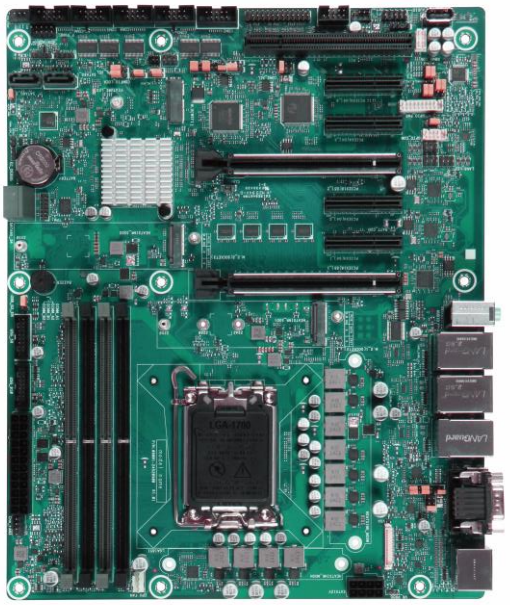
Portwell



RUBY-D814-Q870

Industrial Board

User Manual

Version R1.1

Copyright

Revision History

R1.0	Official release Rev. 1.0
R1.1	Updated Block Diagram

Table of Contents

Chapter 1

Overview

1 Introduction

1. Introduction

The RUBY-D814-Q870 supports Intel® Core™ Ultra Processors (Series 2), LGA1851, utilizes the ATX form factor. It supports four dual channel DDR5 U-DIMMs up to 192GB capacity, one M.2 E key socket, and two M.2 M key sockets. Graphic with Xe LPG architecture, up to 4Xe Graphics Engines, support four independent displays via DisplayPort, HDMI, and VGA. Additionally, it features one 1GbE port, two 2.5GbE ports, one USB3.2 Type-C port and six USB 3.2 Type-A ports.

The RUBY-D814-Q870 series is versatile, compact, powerful, making it ideal for diverse applications such as industrial automation, robotic control systems, automated test equipment, medical equipment, gateways, digital signage, and more.

Chapter 2

Overview

2. Specifications

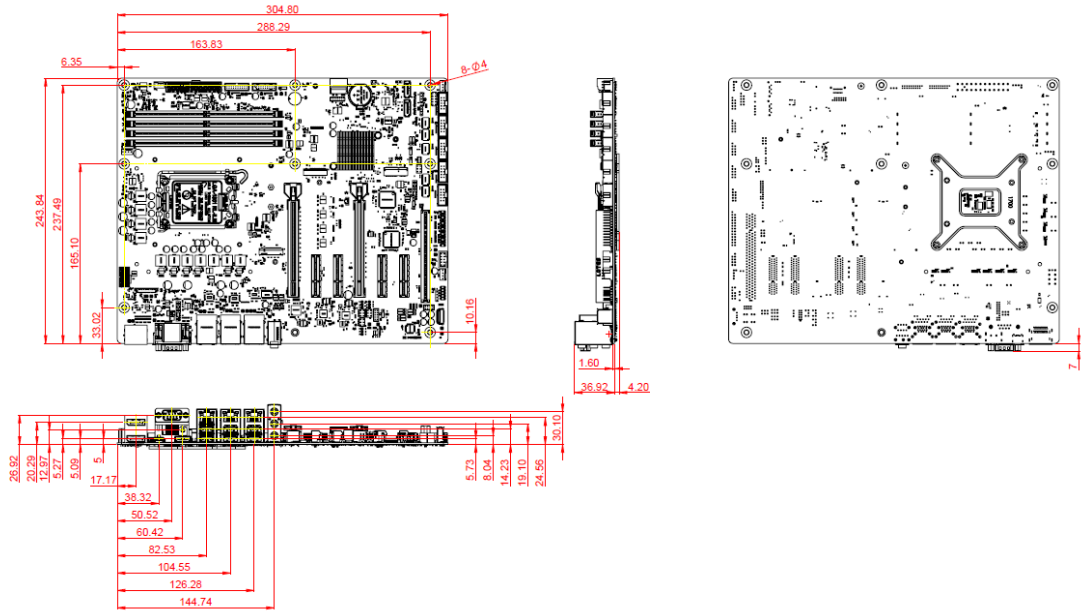
Main Processor	Supports Intel® Core™ Ultra Processors (Series 2), LGA1851 Supports up to 125W TDP
Chipset	Intel® Q870 Chipset
System BIOS	AMI UEFI BIOS
Main Memory	4x non-ECC DDR5 5600MT/s U-DIMM up to 192GB
Graphics	HDMI: 1x HDMI port on rear I/O (HDMI 2.1, 4096 x 2160 @ 60Hz) DP: 2x DP ports on rear I/O (DP 1.4, 3840 x 2160 @ 60Hz) DP: 1x DP port on rear I/O (DP 1.4, 3840 x 2160 @ 60Hz, colay with USB 3.2 Gen 2x2 Type-C®) VGA: 1x VGA output (additional cable required)
Expansion Interface	2 x PCIe 5.0 x16 slot (1 x16 / 2 x8 signal) 2x PCIe 4.0 x4 slot (x4 signal, open slot) 2 x PCIe 4.0 x4 slot (x2 signal, open slot) 1 x PCI slot 1x M.2 E key2230
Storage Interface	4x SATA III port (SATA 6Gb/s) (Supports RAID 0,1,5,10) 1x M.2 2280 M Key (PCIe 4.0 x4) 1x M.2 2242/2260/2280 M Key (PCIe 5.0 x4)
Input/Output	Serial Port: 1x RS-232/422/485 port (selectable via BIOS) on rear I/O, 1x RS232/422/485, 4x RS232 on board header USB Port: 6x USB 3.2 Gen 2 Type-A ports and 1x USB 3.2 Gen 2x2 Type-C® port on rear I/O. 2x USB 3.2 Gen 1 ports (for additional 4x USB 3.2), 1x USB 2.0 vertical connector and 1x USB 2.0 header (for additional 2x USB 2.0) on board. Audio Interface: Audio jack on rear I/O (Line-in, Line-out, Mic-in)
Ethernet	1x Intel® 1GbE Controller 2x Intel® 2.5GbE Controller 3x RJ45 connectors on rear I/O
High Drive GPIO	1x pin-header for GPIO(8bit)
Mechanical and environmental specifications	Board size: 305mm x 244mm (12" x 9.6") Operating temperature: 0 ~ 60° C Storage temperature: -40 ~ 85° C Humidity: 5 ~ 95% non-condensing Power supply voltage: ATX
Certification	CE/FCC

2.1 Supported Operating Systems

The RUBY-D814-Q870 supports the following operating systems.

- Windows® 10 IoT Enterprise LTSC
- Windows® 11 IoT Enterprise LTSC
- Ubuntu 24.04
- RedHat Enterprise

2.2 Mechanical Dimensions



2.3 Power Consumption

Power Supply Test Config

The format of the current is the mean-mean/ max-mean data when running burn in test.

- SKU: Only with CPU, memory and storage
  - CPU: ARROW LAKE S Q2HA/3.7G 125W/QS-38636
  - Memory: MICRON/DDR5 4800 U-DIMM 8GB *4
  - Storage: Intel SSD 128G
  - Oscilloscope:DPO7104
  - OS: Window 10 x64
- BIOS version: V1.00.00
- PSU: 700W

Power Supply Test Result

Source	Voltage	Minimum Load	Max Voltage	MB Capacitive Load	Mean Mean / Max. Mean MB Current
		(A)	Tolerance	(uf)	w/o peripherals(A)
ATX PSU	ATX12V	0.9	±5%	2250	11.517 / 13.668
	+5VSB_ATX	N/A	±5%	50	0.046/ 0.132
	+3V	0.636	±5%	700	0.406/ 0.636
	+5V	1.74	±5%	1200	2.581/ 5.471

2.4 Environmental Specifications

Storage Temperature: -40~85° C

Operation Temperature: 0~60° C

Storage Humidity: 5~95%, non-condensing

Operation Humidity: 5~95%, non-condensing

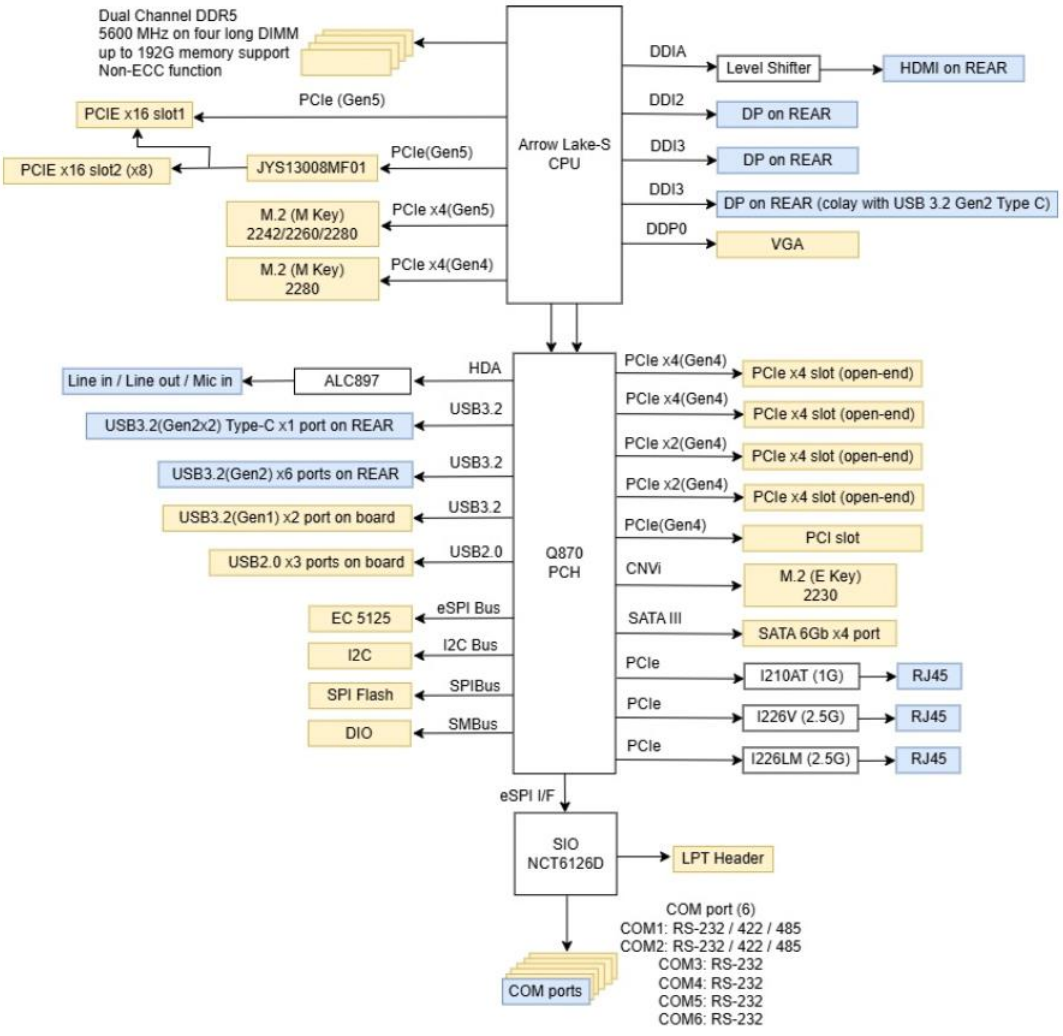
Chapter 3

Overview

3 Block Diagram

3 Block Diagram

On board
Rear I/O



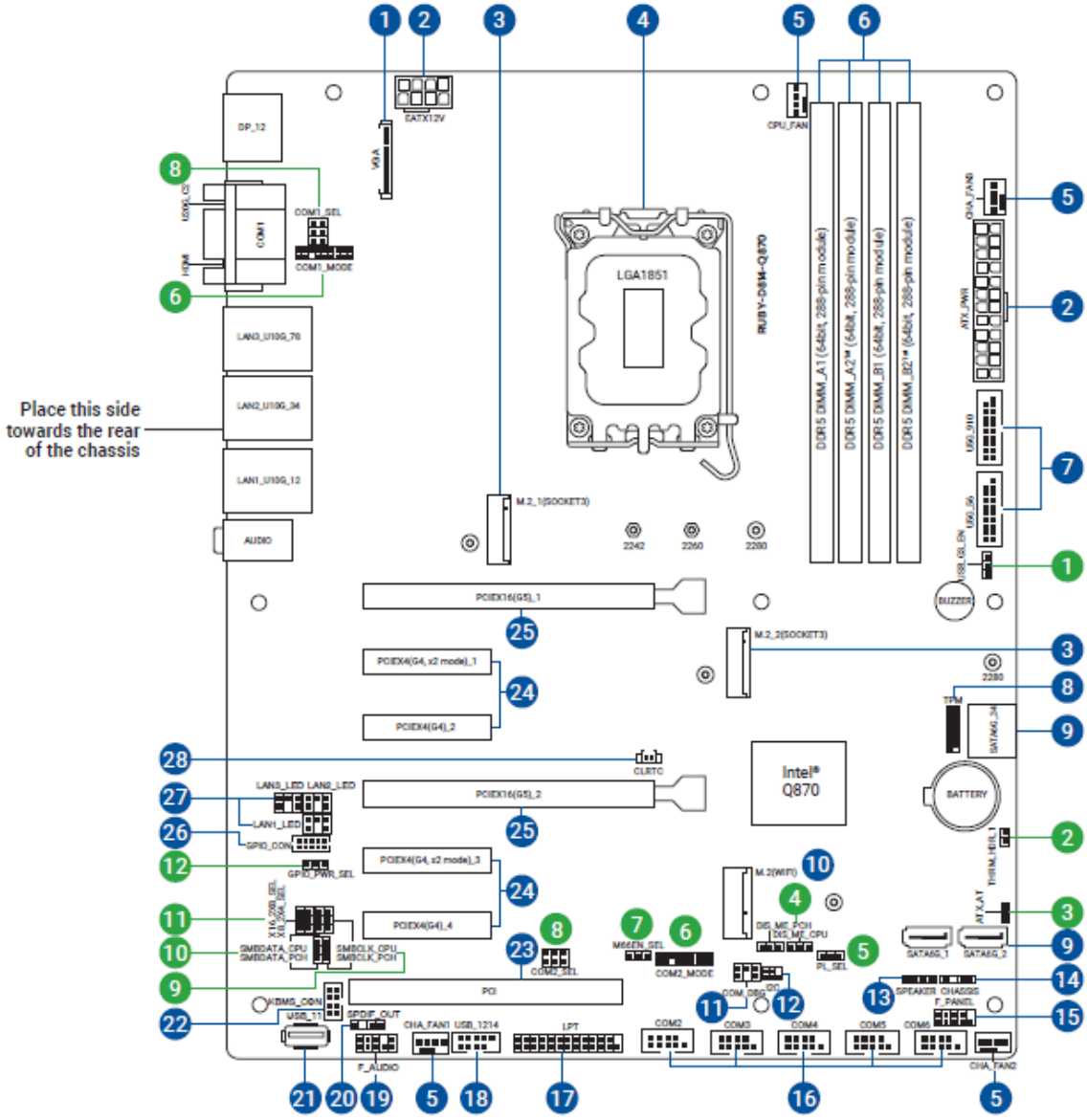
Chapter 4

Overview

4 Hardware Configuration

4.1 Jumpers and Connectors

Figure 1, RUBY-D814-Q870 Top View



4.2 Jumper Settings

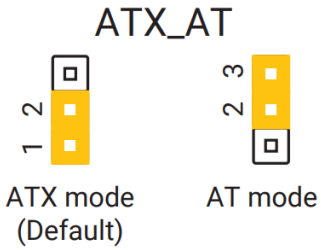
For users to customize RUBY-D814-Q870's features. In the following sections, Short means covering a jumper cap over jumper pins; Open or N/C (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 1 for the Jumper allocations.

Jumper Table
The jumper settings are schematically depicted in this manual as follows:

Jump Function List:

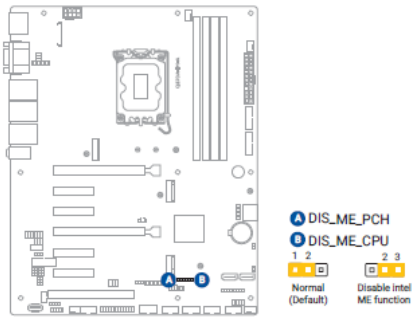
Jump	Function	Remark
1	Extended Temperature Sensor header	2-pin
2	AT/ATX Mode selection jumper	3-pin
3	Disable ME jumpers	3-pin
4	Power Limit selection jumper	3-pin
5	COM mode selection jumper	18-1 pin
6	PCI Clock selection jumper	3-pin
7	COM Ring/+5V/+12V selection jumper	6-pin
8	PCIe SMBus Clock Connection jumpers	3-pin
9	PCIe SMBus Data Connection jumpers	3-pin
10	Expansion slot bandwidth selection jumpers	3-pin
11	General Purpose Input/Output Power selection jumper	3-pin

2: Extended Temperature Sensor header (2-pin THRM_HDR_1)



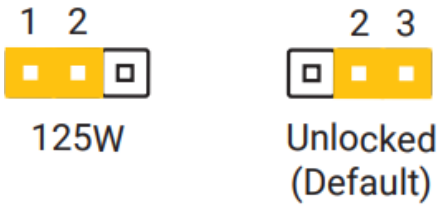
PIN No.	Signal Description
1-2 Short	ATX ★
2-3 Short	AT

3: Disable ME jumpers (3-pin DIS_ME_CPU, DIS_ME_PCH)



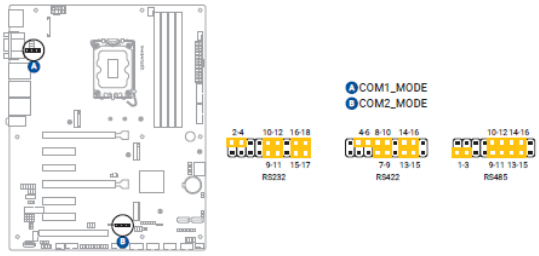
PIN No.	Signal Description
1-2	Normal ★
2-3	Disable Intel ME function

4: Power Limit selection jumpers (3-pin PL_SEL)



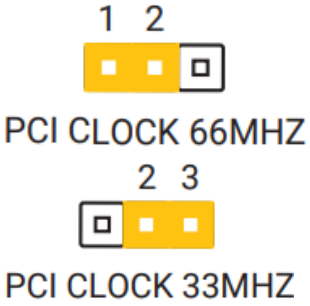
PIN No.	Signal Description
1-2	125W
2-3	Unlocked ★

5: PANEL Voltage Selection



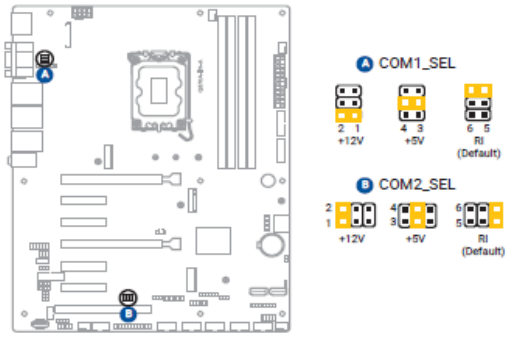
PIN No.	Signal Description
2-4, 9-11, 10-12, 15-17, 16-18	RS-232
4-6, 7-9, 8-10, 13-15, 14-16	RS-422
1-3, 9-11, 10-12, 13-15, 14-16	RS-485

6: PCI Clock selection jumper (3-pin M66EN_SEL)



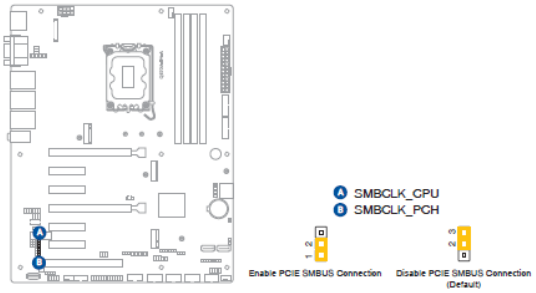
PIN No.	Signal Description
1-2	PCI CLOCK 66MHZ
2-3	PCI CLOCK 33MHZ ★

7: COM Ring/+5V/+12V selection jumpers (6-pin COM1_SEL, COM2_SEL)



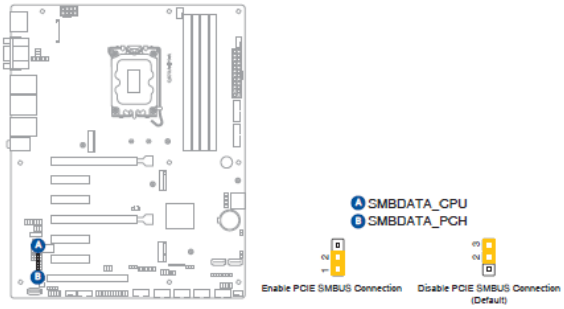
PIN No.	Signal Description
1-2	+12V
3-4	+5V
5-6	Ring ★

8: PCIe SMBus Clock Connection jumpers (3-pin SMBCLK_CPU, SMBCLK_ PCH)



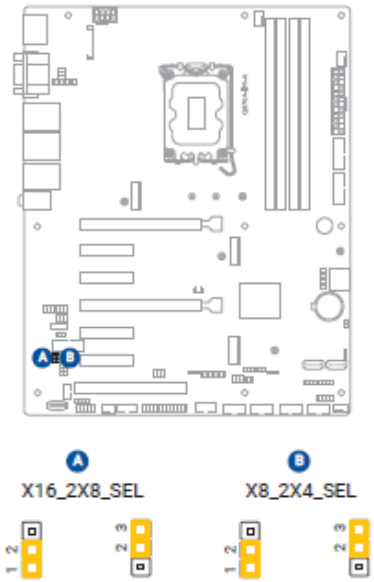
PIN No.	Signal Description
1-2	Enable PCIE SMBUS Connection
3-4	Disable PCIE SMBUS Connection ★

9: PCIe SMBus Data Connection jumpers (3-pin SMBDATA_CPU, SMBDATA_PCH)



PIN No.	Signal Description
1-2	Enable PCIE SMBUS Connection
3-4	Disable PCIE SMBUS Connection ★

10: Expansion slot bandwidth selection jumpers (3-pin X16_2X8_SEL, X8_2X4_SEL)



PIN No.	PCIEX16(G5)_1	PCIEX16(G5)_2
A: 1-2, B: 1-2 (Default)	x16 (if PCIEX16(G5)_2 is empty) x8 (if PCIEX16(G5)_2 is used)	x8
A: 2-3, B: 1-2	x8	x8
A: 2-3, B: 2-3	x8	x4/x4

11: General Purpose Input/Output Power selection jumper (3-pin GPIO_PWR_SEL)

PIN No.	Signal Description
1-2	+3V ★
2-3	+5V

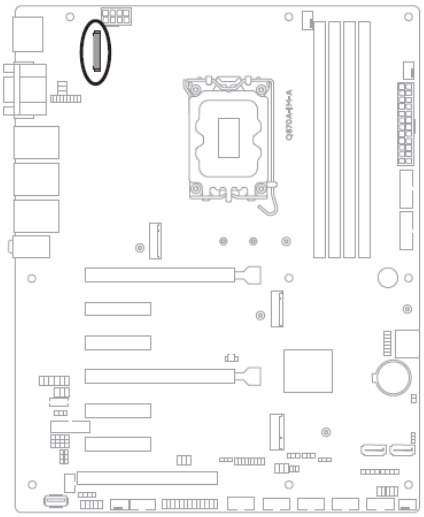
4.3 Connector Settings

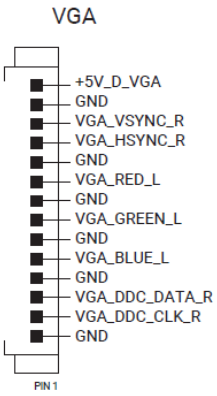
Connector Function List:

Conn	Function	Remark
1	VGA connector	16-pin
2	ATX Power connectors (24-pin ATX_PWR, 8-pin EATX12V)	
3	M.2 socket 3	
4	Intel® LGA1851 CPU socket	
5	CPU and Chassis Fan headers	4-pin
6	DDR5 U-DIMM slots	
7	USB 3.2 Gen 1 connectors	20-1 pin
8	SPI TPM header	14-1 pin
9	SATA 6.0Gb/s ports	7-pin
10	M.2 Wi-Fi (M.2(WIFI))	
11	COM Debug connector	6-1 pin
12	I2C header	6-1 pin
13	Speaker header	4-pin
14	Chassis Intrusion header	4-1 pin
15	System Panel header	10-1 pin
16	Serial Port connectors	10-1 pin
17	LPT header (16-bit GPIO multi-function)	26-1 pin
18	USB 2.0 header	10-1 pin
19	Front Panel Audio header	10-1 pin
20	Digital Audio header	4-1 pin
21	USB 2.0 vertical connector	
22	Keyboard and Mouse Port connector	8-pin
23	PCI slot	
24	PCI Express x4 slots	
25	PCI Express x16 slots	

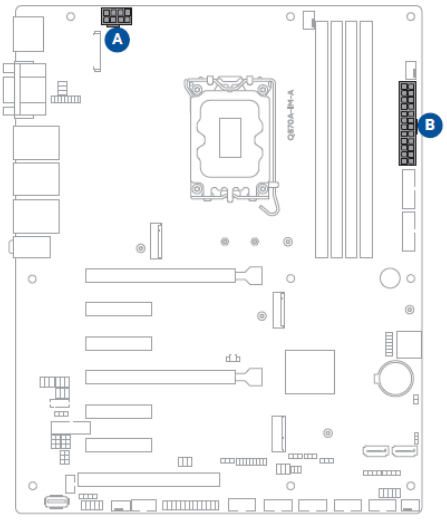
26	General purpose input/output connector	10-pin
27	LAN activity LED connectors	6-1 pin
28	Clear CMOS header	2-pin

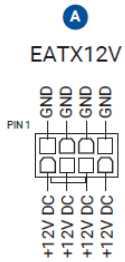
1 VGA connector

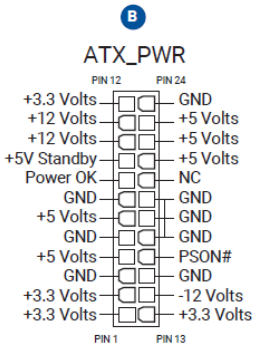




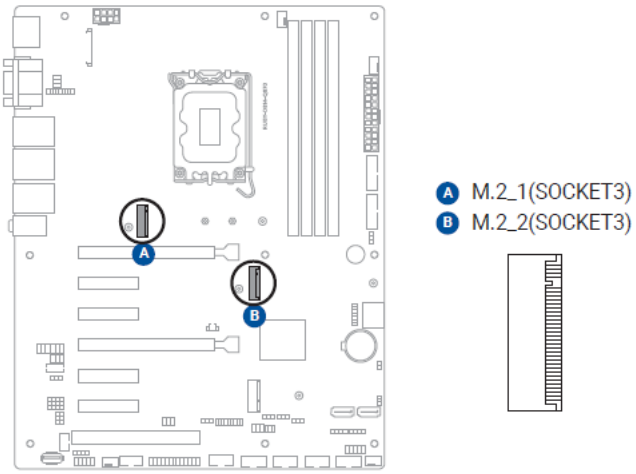
2 ATX Power connectors (24-pin ATX_PWR, 8-pin EATX12V)



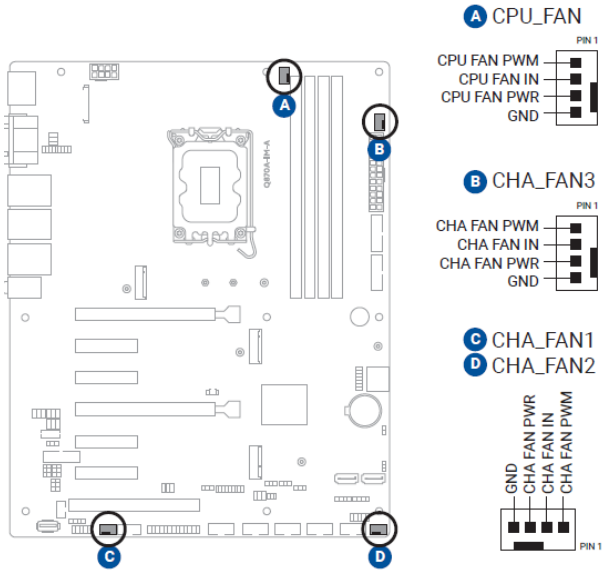




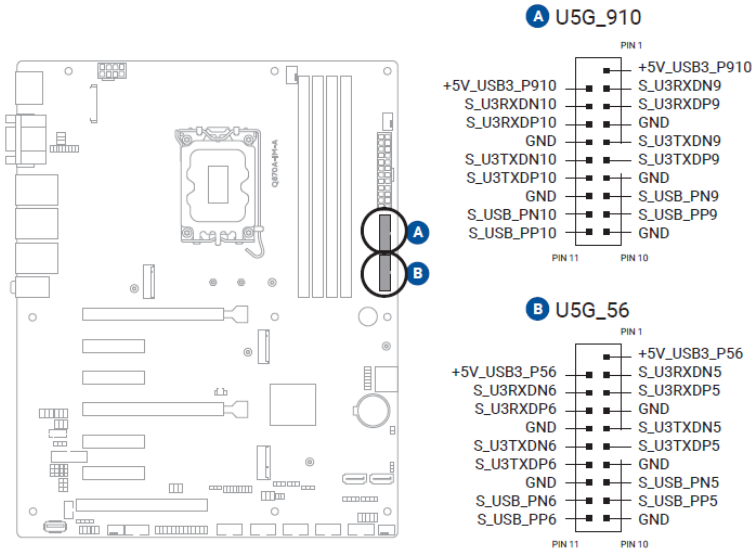
3 M.2 socket 3(M.2(SOCKET3))



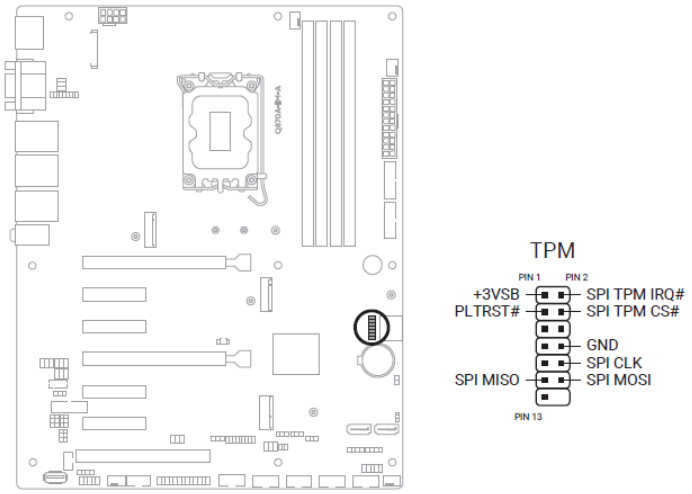
5 CPU and Chassis Fan headers



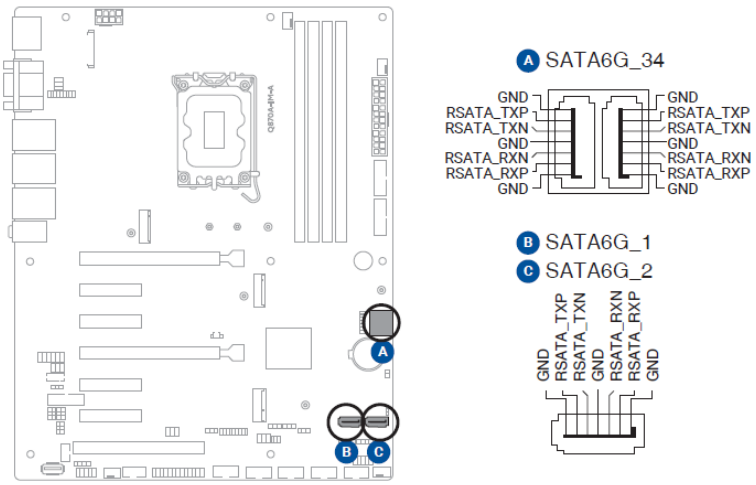
7 USB 3.2 Gen 1 connectors



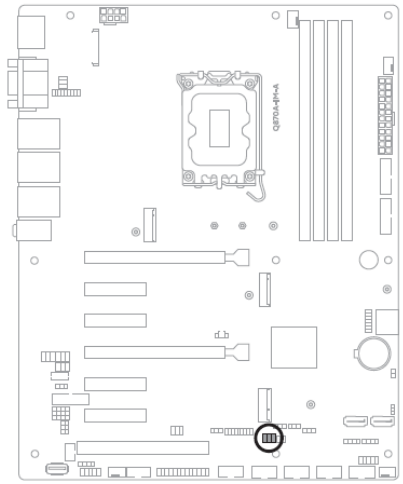
8 SPI TPM header

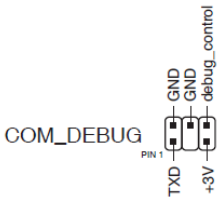


9 SATA 6.0Gb/s ports

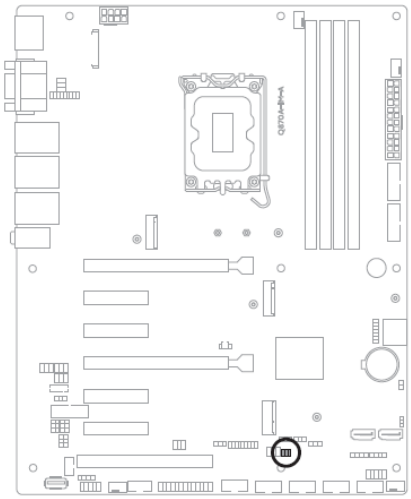


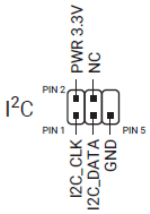
11 COM Debug connector



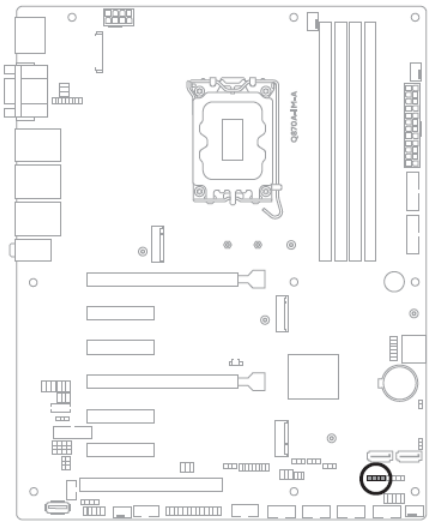


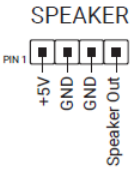
12 I2C header



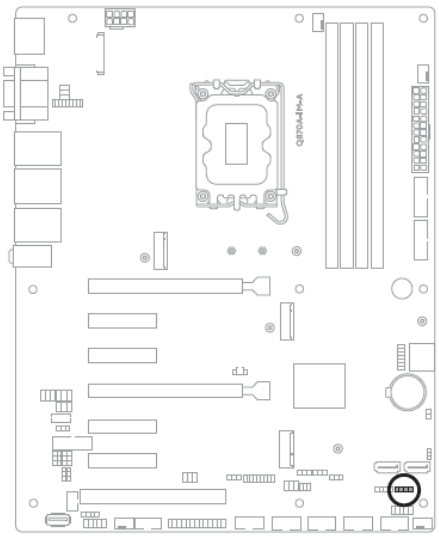


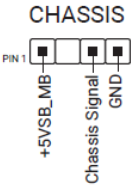
13 Speaker header



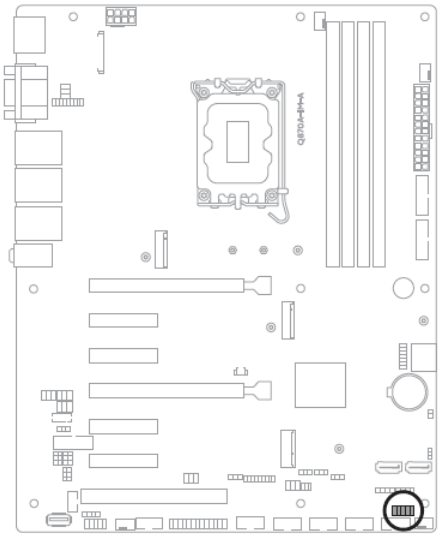


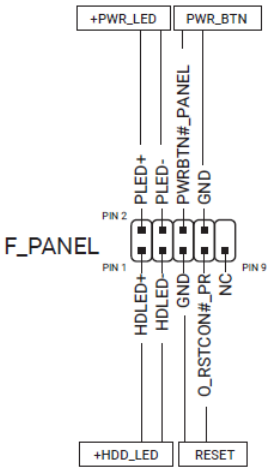
14 Chassis Intrusion header



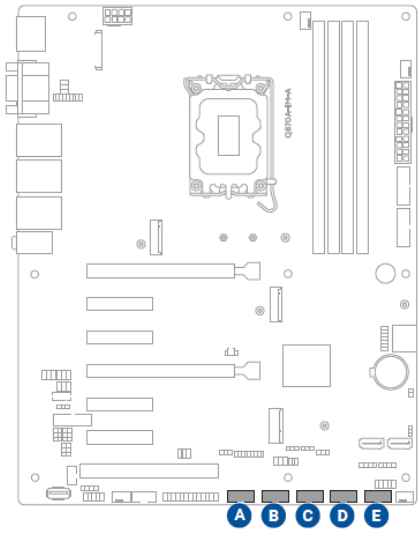


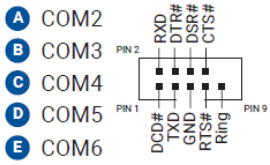
15 System Panel header



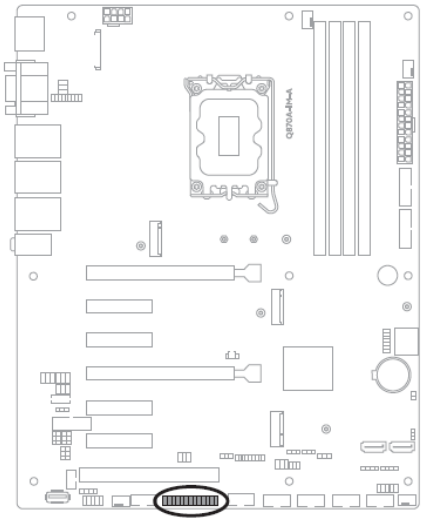


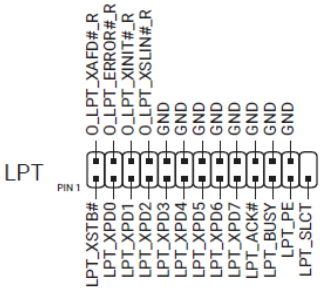
16 Serial Port connectors



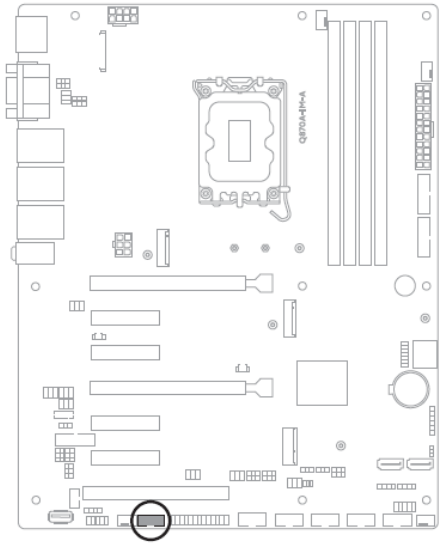


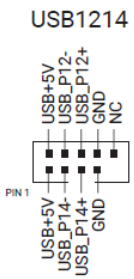
17 LPT header (16-bit GPIO multi-function)



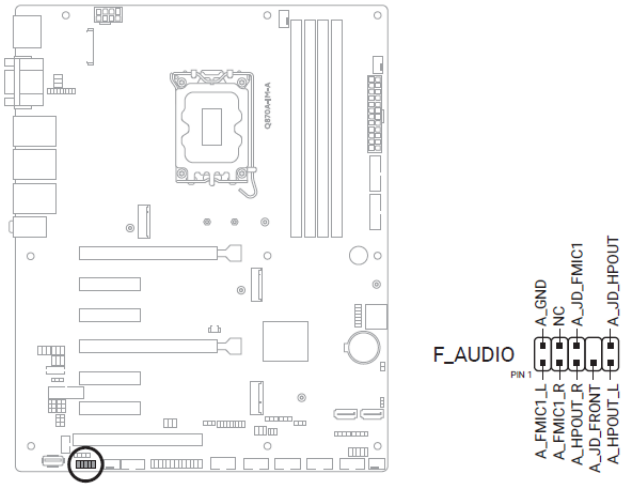


18 USB 2.0 header

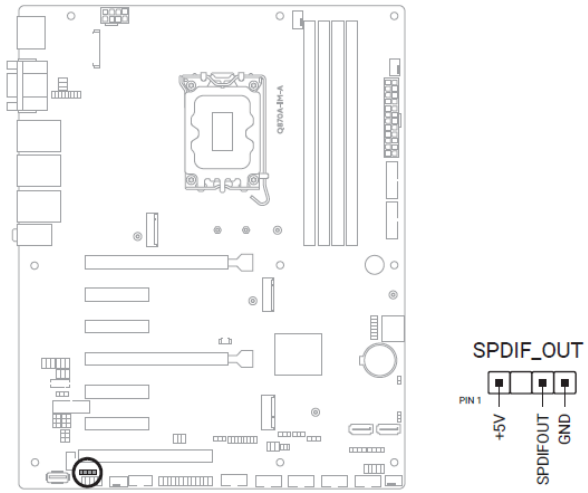




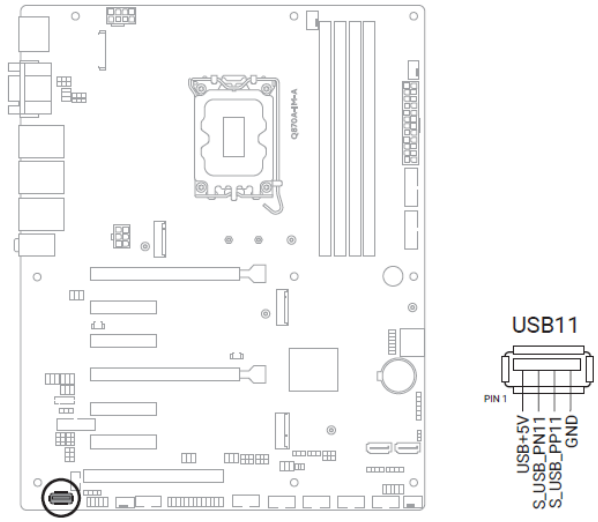
19 Front Panel Audio header



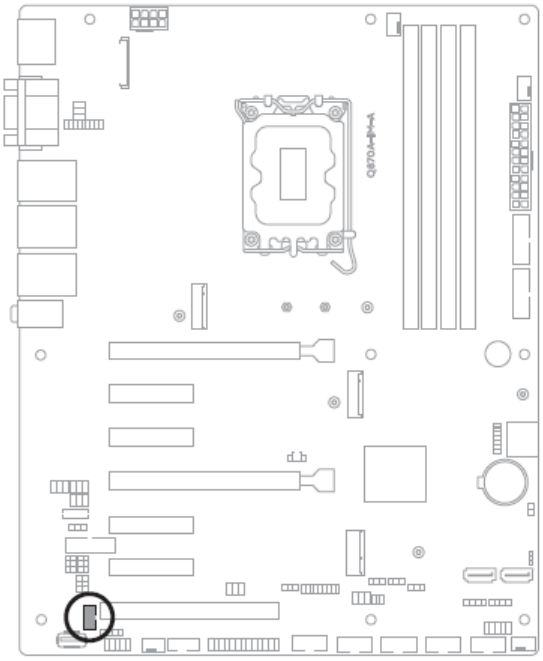
20 Digital Audio header

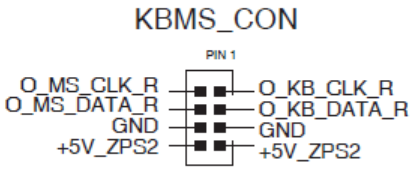


21 USB 2.0 vertical connector

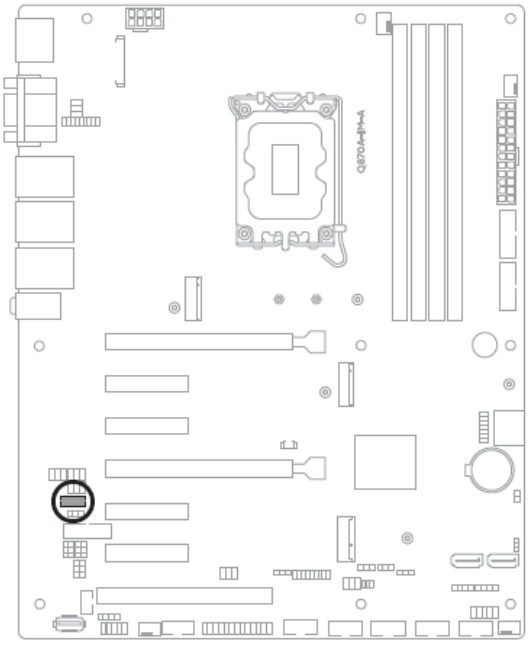


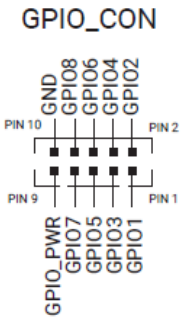
22 Keyboard and Mouse Port connector



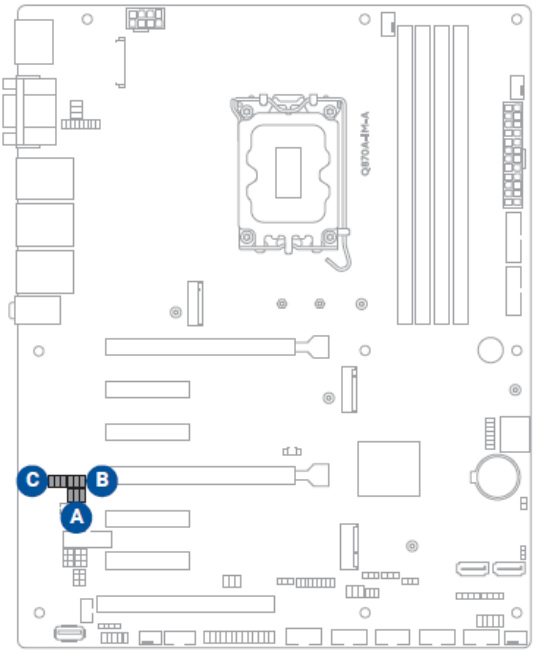


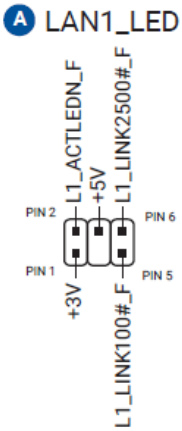
26 General purpose input/output connector

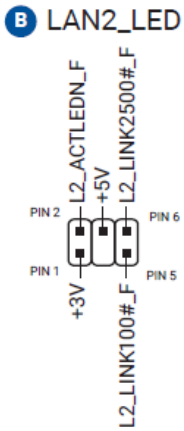


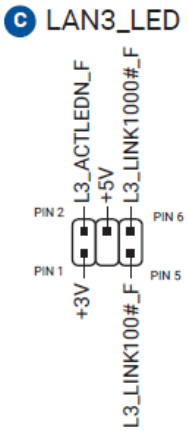


27 LAN activity LED connectors

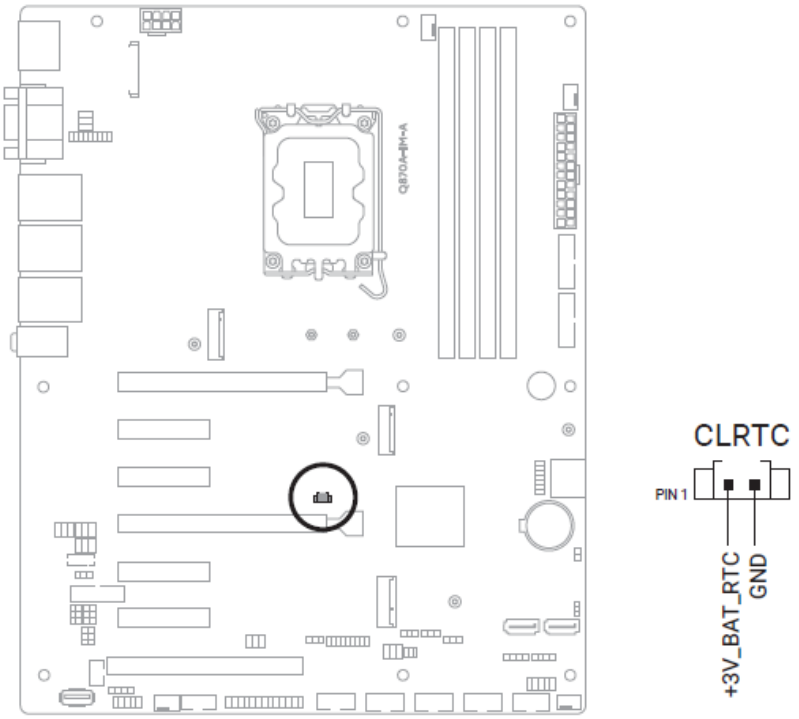








28 Clear CMOS header



Chapter 5

Overview

5 Sample Code

5.1 Watch Dog Timer

[Sample Code]How to Access EC I/O (ex:25C/25D)

```
// EC Function and define
typedef struct _EController_Port{
      UINT8 CMD_Port;
      UINT8 STS_Port;
      UINT8 DATA_Port;
}EControllerPort;

#define EC_PSEUDO_IBF     BIT2
#define EC_STS_IBF          BIT1 // Input buffer full (data ready for
// embedded controller)
#define EC_STS_OBF          BIT0 // Output buffer full (data ready for host)

#ifndef ECIBFTimeoutCount
#define ECIBFTimeoutCount   0x0400
#endif

#define  Port_LIST  {0x66,0x66,0x62},  {0x66,0x66,0x62},  {0x6E,0x6E,0x6A},
{0x66,0x66,0x62},  {0x66,0x66,0x62},  {0x6C,0x6C,0x68},  {0x66,0x66,0x62},
{0x25D,0x25D,0x25C},

EControllerPort Port[] ={ Port_LIST {0xFF,0xFF,0xFF}};

VOID FixDelay()
{
          UINT32 i=30;
          while(i--)
```

```
        {
                IoWrite8(0xeb, 0x55);
                IoWrite8(0xeb, 0xaa);
        }
}

BOOLEAN IsInputBufferFree(
        IN ECTYPE Type)
{
        UINT8         Reg;
        UINTN         i;
        BOOLEAN flag = FALSE;

        for(i=0;i<ECIBFTimeoutCount;i++) {
                Reg = IoRead8(Port[Type].STS_Port); //STS_Port 0x25D
                if(!(Reg & (EC_STS_IBF|EC_PSEUDO_IBF))) {
                        flag = TRUE;
                        break;
                }
                FixDelay();
        }
        return flag;
}

EFI_STATUS    EC_SendCommand (
        IN ECTYPE Type,
        IN UINT8    CMD)
{
        EFI_STATUS        Status = EFI_SUCCESS;

        if(!IsInputBufferFree(Type)) return -1;
        IoWrite8(Port[Type].CMD_Port,CMD);        //CMD_Port 0x25D
        if(!IsInputBufferFree(Type)) return -1;
```

```
        return Status;
}

EFI_STATUS   EC_SendData (
        IN ECTYPE Type,
        IN UINT8 Data)
{
        EFI_STATUS      Status = EFI_SUCCESS;

        if(!IsInputBufferFree(Type)) return -1;
        IoWrite8(Port[Type].DATA_Port,Data);    //DATA_Port 0x25C
        if(!IsInputBufferFree(Type)) return -1;

        return Status;
}
```

Ex: 透過 EC I/O command 設定 Set WDT

```
    EFI_STATUS Status = EFI_SUCCESS;
    Status      =      ECSendCommand(EC_PROPRIETARY_PORT,0xa2);
//EC_PROPRIETARY_PORT = 7
    if(Status != EFI_SUCCESS)    return Status;

    Status = ECSendData(EC_PROPRIETARY_PORT,LSB);      // LSB =
((UINT16)WDT_Timer >> 8)
    if(Status != EFI_SUCCESS)    return Status;

    Status = ECSendData(EC_PROPRIETARY_PORT,MSB);      // MSB =
((UINT16)WDT_Timer & 0xFF)
    if(Status != EFI_SUCCESS)    return Status;
```

5.2 GPIO Signal

[Sample Code] How to Set RUBY-D814-Q870 GPIO

The GPIO of RUBY-D814-Q870 has 2 types, one is SMBUS, the other is SIO. There are 24 GPIO pins on RUBY-D814-Q870. The Mapping table is the bellow:

Table 1. GPIO pin and reg value mapping table

GPIO Type	Pin	Pin Reg Value
SMBUS	0	0
	1	1
	2	2
	3	3
	4	4
	5	5
	6	6
	7	7
SIO	8	7
	9	6
	10	2
	11	5
	12	1
	13	4
	14	0
	15	3
SIO	16	7
	17	6
	18	5
	19	4
	20	3
	21	2
	22	1
	23	0

SMBUS Type (Pin 0 - 7)

1. Get SMBUS_BASE address

```
val = 0x8080fc20;
    Outportd(0xCF8, val);
    val = Inportd(0xCFC);
    SMBUS_BASE = val & 0x0000FFE0;      //0x4000
```

2. Set GPIOn to GPI or GPO

```
//Pin 0-7
    Status = Inportb(SMBUS_BASE + 0x00);
    Outportb(SMBUS_BASE + 0x00, Status); // SMBus Clear Status

    Outportb(SMBUS_BASE + 0x02, 0x08); // Set SMBus CMD to Byte Data
    Outportb(SMBUS_BASE + 0x04, 0x40); // Set SMBus Slave Address to
0x40
// and excute Read flow
    Outportb(SMBUS_BASE + 0x03, 0x00); // Set SMBus Reg
    val = Inportb(SMBUS_BASE + 0x02);
    val = val | 0x40;
    Outportb(SMBUS_BASE + 0x02, val); // Excute SMBus Command

    Status = Inportb(SMBUS_BASE + 0x00); // Get SMBus Status
    while (!(Status & 0x8E)) { // Wait for SMBus finished command
        MicroSecondDelay(10);
        Status = Inportb(SMBUS_BASE + 0x00);
    }

    val = Inportb(SMBUS_BASE + 0x05); // Get SMBus Data
    val = val | (0x01 << GPIOn); // GPI, val = val | ~(0x01 << GPIOn)
// if GPO, GPIOn value is pin reg value which
// refefrence to Table 1. Pin Reg Value Field
    Status = Inportb(SMBUS_BASE + 0x00);
    Outportb(SMBUS_BASE + 0x00, Status); // SMBus Clear Status
```

```
    Outportb(SMBUS_BASE + 0x02, 0x08); // Set SMBus CMD to Byte Data
    Outportb(SMBUS_BASE + 0x04, 0x40); // Set SMBus Slave Address to
0x40
// and excute Write flow
    Outportb(SMBUS_BASE + 0x03, 0x00); // Set SMBus Reg
    Outportb(SMBUS_BASE + 0x05, val); // Set SMBus Data
    val = Inportb(SMBUS_BASE + 0x02);
    val = val | 0x40;
    Outportb(SMBUS_BASE + 0x02, val); // Excute SMBus Command

    Status = Inportb(SMBUS_BASE + 0x00); // Get SMBus Status
    while (!(Status & 0x8E)) { // Wait for SMBus finished command
        MicroSecondDelay(10);
        Status = Inportb(SMBUS_BASE + 0x00);
    }
```

3. Get GPIOn GPI value

```
//Pin 0-7
    Status = Inportb(SMBUS_BASE + 0x00);
    Outportb(SMBUS_BASE + 0x00, Status); // SMBus Clear Status

    Outportb(SMBUS_BASE + 0x02, 0x08); // Set SMBus CMD to Byte Data
    Outportb(SMBUS_BASE + 0x04, 0x41); // Set SMBus Slave Address to
0x40
// and excute Read flow
    Outportb(SMBUS_BASE + 0x03, 0x09); // Set SMBus Reg
    val = Inportb(SMBUS_BASE + 0x02);
    val = val | 0x40;
    Outportb(SMBUS_BASE + 0x02, val); // Excute SMBus Command

    Status = Inportb(SMBUS_BASE + 0x00); // Get SMBus Status
    while (!(Status & 0x8E)) { // Wait for SMBus finished command
```

```
        MicroSecondDelay(10);
        Status = Inportb(SMBUS_BASE + 0x00);
    }

    val = Inportb(SMBUS_BASE + 0x05); // Get SMBus Data
    if (val & (0x01 << GPIOn))    // Determine if GPIOn is High or Low,
// GPIOn value is pin reg value which
// refefrence to Table 1. Pin Reg Value Field

        return HIGH; //GPI High
    else
        return LOW; //GPI Low

4. Set GPIOn GPO value
//Pin 0-7
    Status = Inportb(SMBUS_BASE + 0x00);
    Outportb(SMBUS_BASE + 0x00, Status); // SMBus Clear Status

    Outportb(SMBUS_BASE + 0x02, 0x08); // Set SMBus CMD to Byte Data
    Outportb(SMBUS_BASE + 0x04, 0x41); // Set SMBus Slave Address to
0x40
// and excute Read flow
    Outportb(SMBUS_BASE + 0x03, 0x0A); // Set SMBus Reg
    val = Inportb(SMBUS_BASE + 0x02);
    val = val | 0x40;
    Outportb(SMBUS_BASE + 0x02, val); // Excute SMBus Command

    Status = Inportb(SMBUS_BASE + 0x00); // Get SMBus Status
    while (!(Status & 0x8E)) { // Wait for SMBus finished command
        MicroSecondDelay(10);
        Status = Inportb(SMBUS_BASE + 0x00);
    }
```

```
    val = Inportb(SMBUS_BASE + 0x05); // Get SMBus Data
    val = val | (0x01 << GPIOn); // GPO High, val = val | ~(0x01 << GPIOn)
// if GPO Low, GPIOn value is pin reg value which
// refefrence to Table 1. Pin Reg Value Field

    Status = Inportb(SMBUS_BASE + 0x00);
    Outportb(SMBUS_BASE + 0x00, Status); // SMBus Clear Status

    Outportb(SMBUS_BASE + 0x02, 0x08); // Set SMBus CMD to Byte Data
    Outportb(SMBUS_BASE + 0x04, 0x40); // Set SMBus Slave Address to
0x40
// and excute Write flow
    Outportb(SMBUS_BASE + 0x03, 0x0A); // Set SMBus Reg
    Outportb(SMBUS_BASE + 0x05, val); // Set SMBus Data
    val = Inportb(SMBUS_BASE + 0x02);
    val = val | 0x40;
    Outportb(SMBUS_BASE + 0x02, val); // Excute SMBus Command

    Status = Inportb(SMBUS_BASE + 0x00); // Get SMBus Status
    while (!(Status & 0x8E)) { // Wait for SMBus finished command
        MicroSecondDelay(10);
        Status = Inportb(SMBUS_BASE + 0x00);
    }
```

SIO Type (Pin 8 - 23)

1. Define SIO Port

SIO_INDEX_PORT is 0x2E

SIO_DATA_PORT is 0x2F

2. Set GPIOn to GPI or GPO

```
//Pin 8-15
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO
```

```
    Outportb(SIO_INDEX_PORT, 0x07);
    Outportb(SIO_DATA_PORT,   0x07);

    Outportb(SIO_INDEX_PORT, 0x30);
    val = Inportb(SIO_DATA_PORT)
    val = val | 0x10;          // Pin 8 – 15 using 0x10
    Outportb(SIO_INDEX_PORT, 0x30);
    Outportb(SIO_DATA_PORT,   val); // Active GPIO

    Outportb(SIO_INDEX_PORT, 0xF0);
    val = Inportb(SIO_DATA_PORT) // Read current value
    val = val | (0x01 << GPIOn); // GPO, val = val & ~(0x01 << GPIOn);
// if GPO, GPIOn value is pin reg value which
// refefrence to Table 1. Pin Reg Value Field

    Outportb(SIO_INDEX_PORT, 0xF0);
    Outportb(SIO_DATA_PORT,   val);

    Outportb(SIO_INDEX_PORT, 0xAA); // Lock SIO

//Pin 16-23
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO

    Outportb(SIO_INDEX_PORT, 0x07);
    Outportb(SIO_DATA_PORT,   0x07);

    Outportb(SIO_INDEX_PORT, 0x30);
    val = Inportb(SIO_DATA_PORT)
    val = val | 0x08;          // Pin 16 – 23 using 0x08
    Outportb(SIO_INDEX_PORT, 0x30);
    Outportb(SIO_DATA_PORT,   val); // Active GPIO
```

```
    Outportb(SIO_INDEX_PORT, 0xF0);
    val = Inportb(SIO_DATA_PORT) // Read current value
    val = val | (0x01 << GPIOn); // GPO, val = val & ~(0x01 << GPIOn);
// if GPO, GPIOn value is pin reg value which
// refefrence to Table 1. Pin Reg Value Field
    Outportb(SIO_INDEX_PORT, 0xF0);
    Outportb(SIO_DATA_PORT,   val);

    Outportb(SIO_INDEX_PORT, 0xAA); // Lock SIO
```

3. Get GPIOn GPI value

```
//Pin 8-15
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO

    Outportb(SIO_INDEX_PORT, 0x07);
    Outportb(SIO_DATA_PORT,   0x07);

    Outportb(SIO_INDEX_PORT, 0x30);
    val = Inportb(SIO_DATA_PORT)
    val = val | 0x10;          // Pin 8 – 15 using 0x10
    Outportb(SIO_INDEX_PORT, 0x30);
    Outportb(SIO_DATA_PORT,   val); // Active GPIO

    Outportb(SIO_INDEX_PORT, 0xF1);
    val = Inportb(SIO_DATA_PORT) // Read current value

    Outportb(SIO_INDEX_PORT, 0xAA); // Lock SIO

    if (val & (0x01 << GPIOn))   // Determine if GPIOn is High or Low;
// GPIOn value is pin reg value which
// refefrence to Table 1. Pin Reg Value Field
```

```
        return HIGH; //GPI High
    else
        return LOW; //GPI Low

//Pin 16-23
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO

    Outportb(SIO_INDEX_PORT, 0x07);
    Outportb(SIO_DATA_PORT,   0x07);

    Outportb(SIO_INDEX_PORT, 0x30);
    val = Inportb(SIO_DATA_PORT)
    val = val | 0x08;          // Pin 16 – 23 using 0x08
    Outportb(SIO_INDEX_PORT, 0x30);
    Outportb(SIO_DATA_PORT,   val); // Active GPIO

    Outportb(SIO_INDEX_PORT, 0xF1);
    val = Inportb(SIO_DATA_PORT) // Read current value

    Outportb(SIO_INDEX_PORT, 0xAA); // Lock SIO

    if (val & (0x01 << GPIOn))   // Determine if GPIOn is High or Low;
// GPIOn value is pin reg value which
// refefrence to Table 1. Pin Reg Value Field.

        return HIGH; //GPI High
    else
        return LOW; //GPI Low
```

4. Set GPIOn GPO value

```
//Pin 8-15
```

```
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO

    Outportb(SIO_INDEX_PORT, 0x07);
    Outportb(SIO_DATA_PORT,   0x07);

    Outportb(SIO_INDEX_PORT, 0x30);
    val = Inportb(SIO_DATA_PORT)
    val = val | 0x10;          // Pin 8 – 15 using 0x10
    Outportb(SIO_INDEX_PORT, 0x30);
    Outportb(SIO_DATA_PORT,   val); // Active GPIO

    Outportb(SIO_INDEX_PORT, 0xF1);
    val = Inportb(SIO_DATA_PORT) // Read current value
    val = val | (0x01 << GPIOn); // GPO LOW, val = val & ~(0x01 << GPIOn);
// if GPO High, GPIOn value is pin reg value which
// refefrence to Table 1. Pin Reg Value Field

    Outportb(SIO_INDEX_PORT, 0xF1);
    Outportb(SIO_DATA_PORT,   val);

    Outportb(SIO_INDEX_PORT, 0xAA); // Lock SIO

//Pin 16-23
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO
    Outportb(SIO_INDEX_PORT, 0x87); // Unlock SIO

    Outportb(SIO_INDEX_PORT, 0x07);
    Outportb(SIO_DATA_PORT,   0x07);

    Outportb(SIO_INDEX_PORT, 0x30);
    val = Inportb(SIO_DATA_PORT)
    val = val | 0x08;          // Pin 16 – 23 using 0x08
```

```
    Outportb(SIO_INDEX_PORT, 0x30);
    Outportb(SIO_DATA_PORT,   val); // Active GPIO

    Outportb(SIO_INDEX_PORT, 0xF1);
    val = Inportb(SIO_DATA_PORT) // Read current value
    val = val | (0x01 << GPIOn); // GPO LOW, val = val & ~(0x01 << GPIOn);
// if GPO High, GPIOn value is pin reg value which
// refefrence to Table 1. Pin Reg Value Field

    Outportb(SIO_INDEX_PORT, 0xF1);
    Outportb(SIO_DATA_PORT,   val);

    Outportb(SIO_INDEX_PORT, 0xAA); // Lock SIO
```

Chapter 6

Overview

6 BIOS Setup Items

RUBY-D814-Q870 is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in SPI Flash so that it is retained during power-off periods. When the system is turned on, RUBY-D814-Q870 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

6.1 Entering Setup -- Launch System Setup

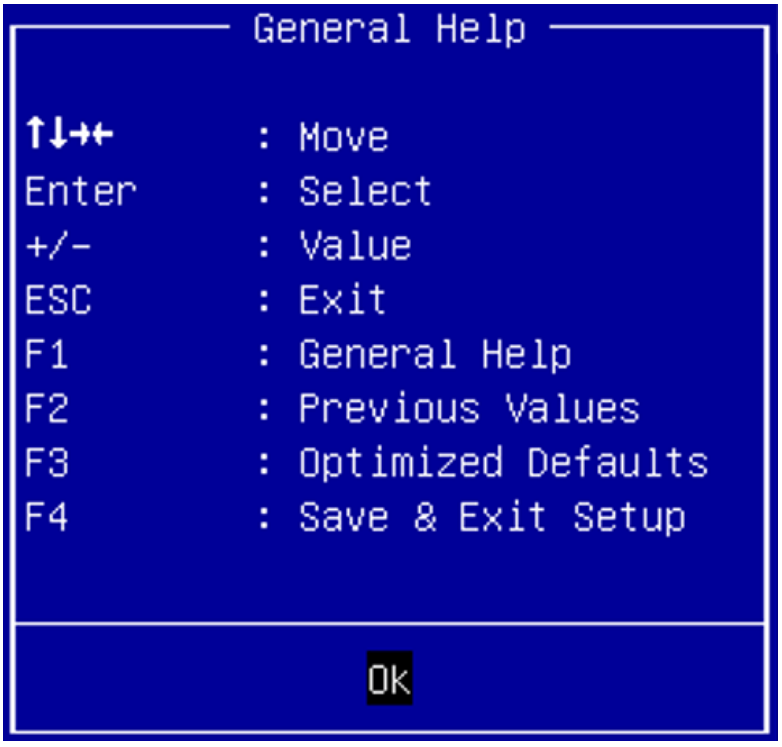
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

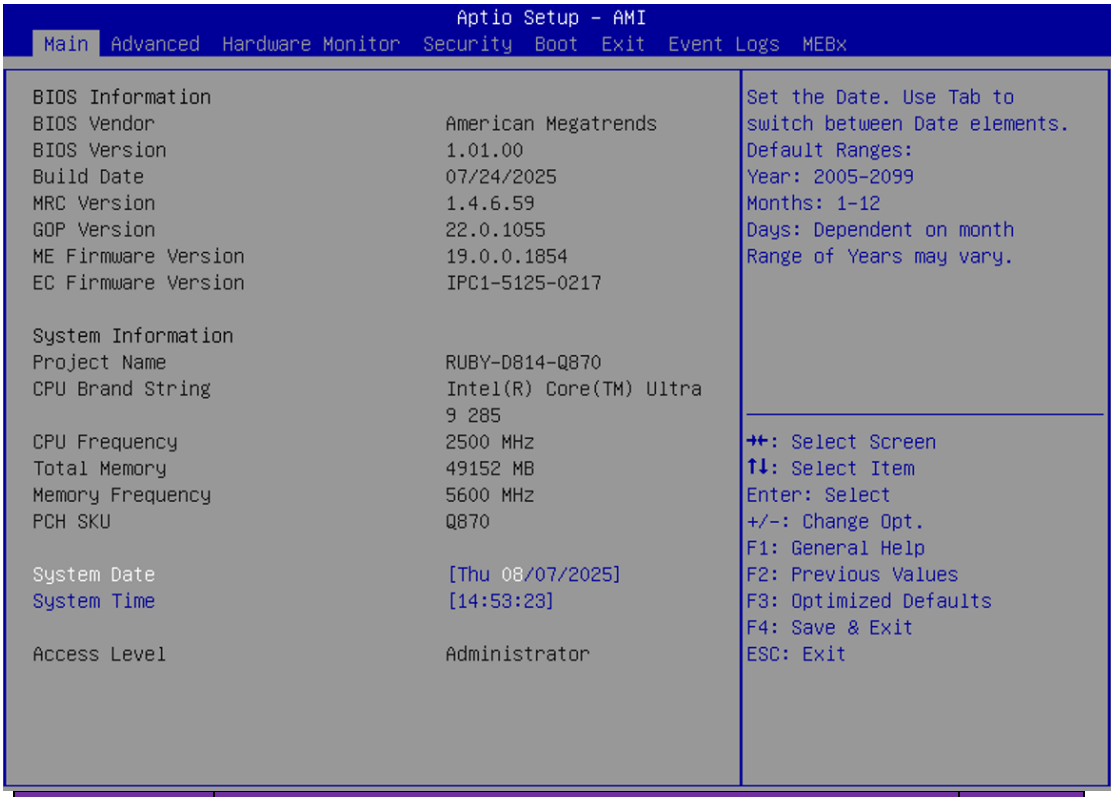
If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.

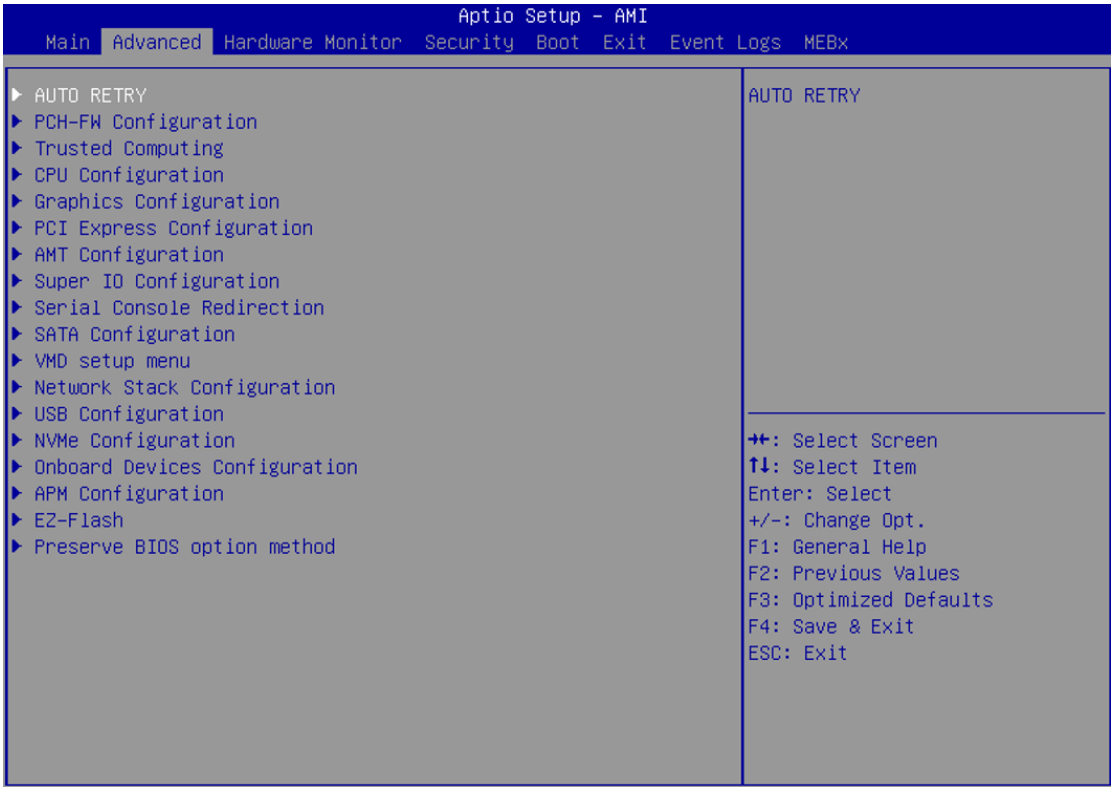


6.2 Main



Feature	Description	Options
System Date	Set the Date. Use Tab to switch between Date elements. Default Ranges: Year: 2005 – 2099 Months: 1 – 12 Days: Dependent on month Range of Years may vary.	
System Time	Set the Time. Use Tab to switch between Time elements.	

6.3 Advanced


Aptio Setup – AMI
Main
Advanced
Hardware Monitor
Security
Boot
Exit
Event Logs
MEBx
AUTO RETRY
PCH-FW Configuration
Trusted Computing
CPU Configuration
Graphics Configuration
PCI Express Configuration
AMT Configuration
Super IO Configuration
Serial Console Redirection
SATA Configuration
VMD setup menu
Network Stack Configuration
USB Configuration
NVMe Configuration
Onboard Devices Configuration
APM Configuration
EZ-Flash
Preserve BIOS option method
AUTO RETRY
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

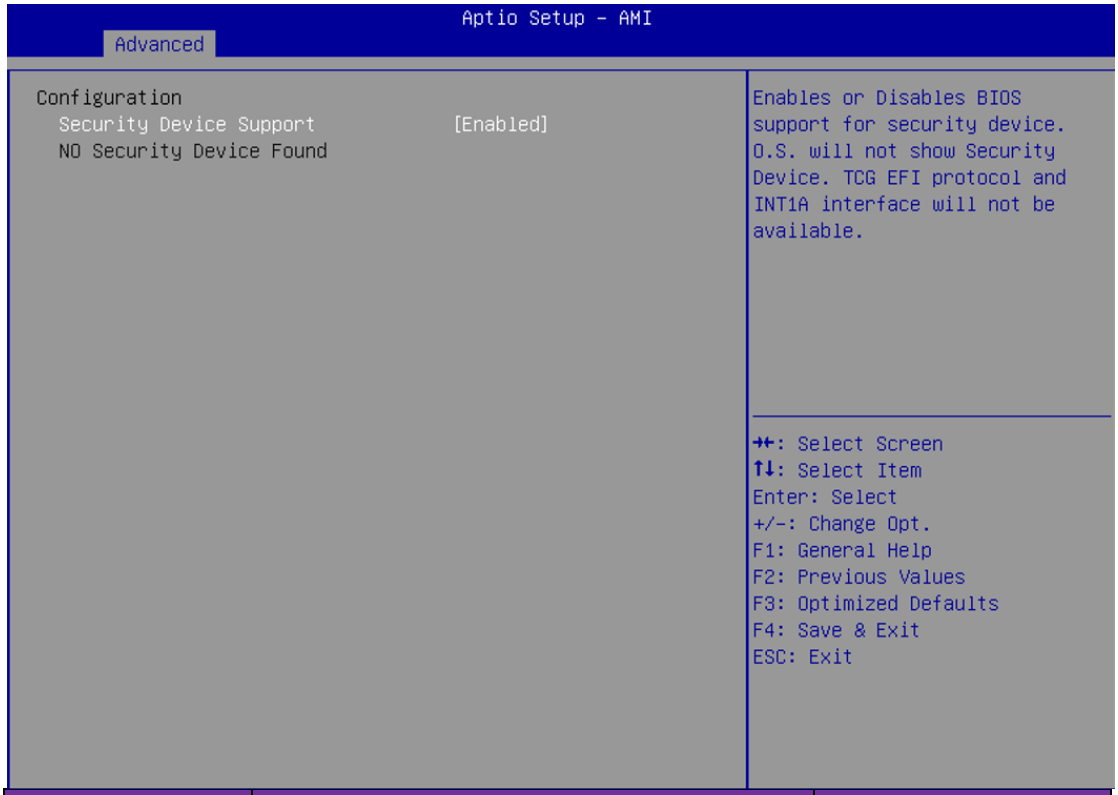
6.3.1 AUTO RETRY

Feature	Description	Options
Auto Retry	Watchdog /Disabled ALL item selection	★EC Watchdog, Disabled
Watchdog Count Mode	Select Watchdog Timer count mode	★Second Mode, Minute Mode
Watchdog Timer	Watchdog Timer time-out value. Range: 30 ~ 255	★180

6.3.2 PCH-FW Configuration

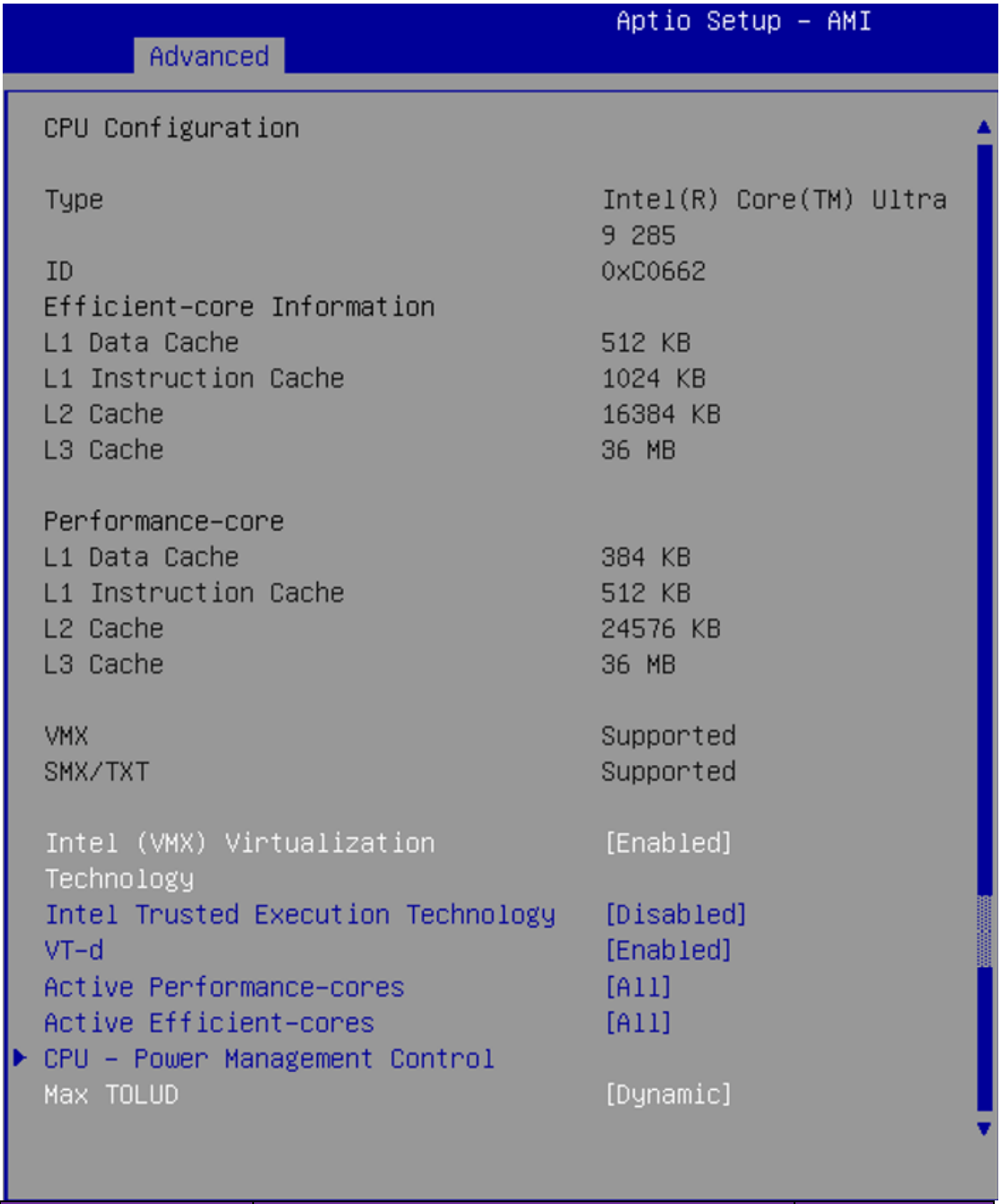
Feature	Description	Options
TPM Device Selection	Selects TPM device: PTT or dTPM. PTT - Enables PTT in SkuMgr dTPM 1.2 – Disables PTT in SkuMgr Warning ! PTT/ dTPM will be disabled and all data saved on it will be lost.	★dTPM, PTT

6.3.3 Trusted Computing



Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.	★Enabled, Disabled

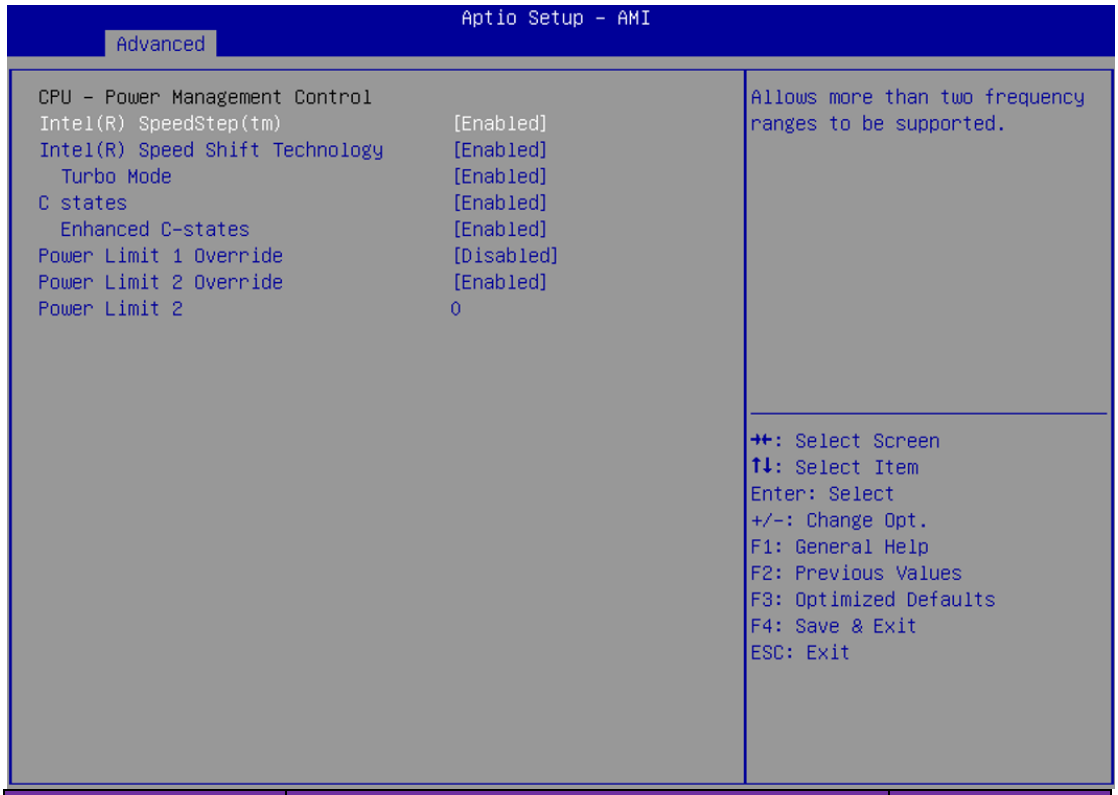
6.3.4 CPU Configuration



Feature	Description	Options
Intel (VMX)Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.	★Enabled, Disabled
Intel Trusted Execution Technology	Enables utilization of additional hardware capabilities provided by Intel(R) Trusted Execution Technology. Changes require a full power cycle to take effect.	Enabled, ★Disabled
VT-d	VT-d capability	★Enabled, Disabled

Active Performance-cores	Number of P-cores to enable in each processor package. Note: Number of Cores and E-Cores are looked at together. When both are {0,0}, Pcode will enable all cores.	★All, 7, 6, 5, 4, 3, 2, 1
Active Efficient-cores	Number of E-cores to enable in each processor package. Note: Number of Cores and E-Cores are looked at together. When both are {0,0}, Pcode will enable all cores.	★All, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0
CPU – Power Management Control	CPU – Power Management Control Options	
Max TOLUD	Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller	★Dynamic, 0.75 GB, 1 GB, 1.25 GB, 1.5 GB, 1.75 GB, 2 GB, 2.25 GB, 2.5 GB

CPU – Power Management Control



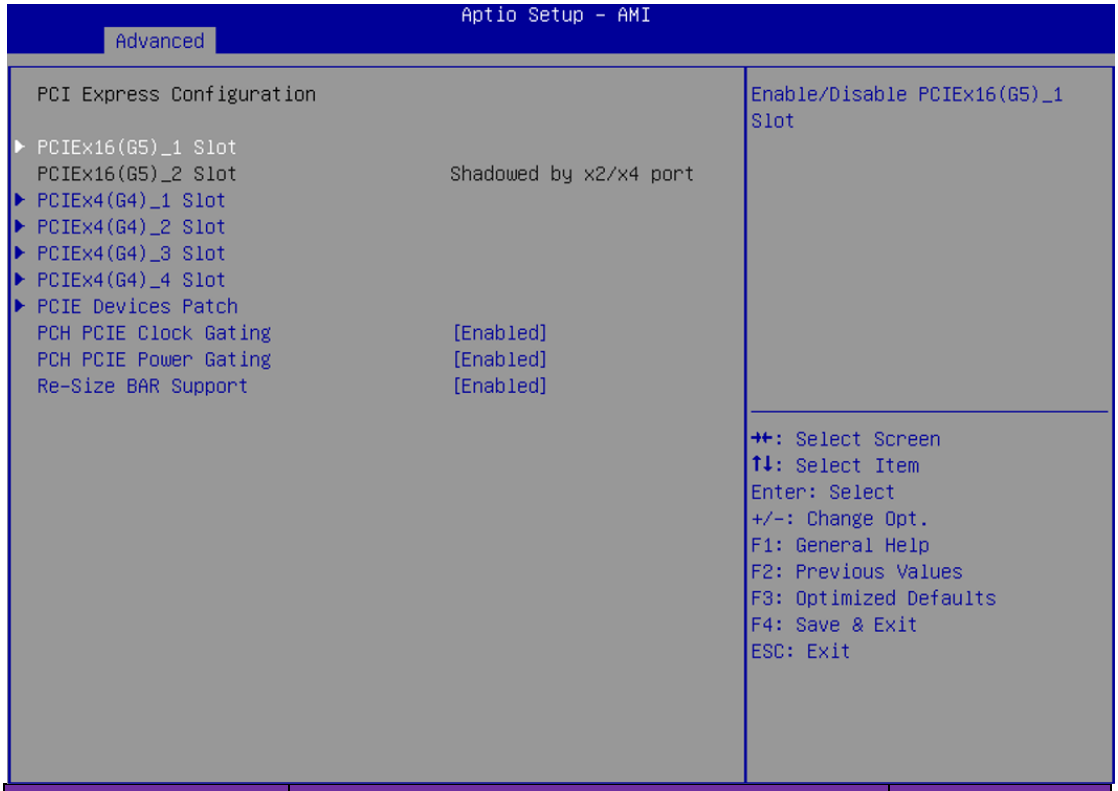
Feature	Description	Options
Intel(R) SpeedStep(tm)	Allows more than two frequency ranges to be supported.	★Enabled, Disabled
Intel(R) Speed Shift Technology	Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.	★Enabled, Disabled
Turbo Mode	Enable/Disable processor Turbo Mode.	★Enabled, Disabled
C states	Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.	★Enabled, Disabled
Enhanced C-states	Enable/Disable C1E. When enabled, CPU will switch to minimum speed when all cores enter C-State.	★Enabled, Disabled
Power Limit 1 Override	Enable/Disable Power Limit 1 override. If this option is disabled, BIOS will program the default values for power Limit 1 and Power Limit 1 Time Window.	Enabled, ★Disabled
Power Limit 1 Override [Enabled]		
Power Limit 1	Power Limit 1 in Milli Wattts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits. Other SKUs: This value must be between Min Power Limit and Processor Base Power (TDP) Limit.	

Power Limit 2 Override	Enable/Disable Power Limit 2 override. If this option is disabled, BIOS will program the default values for Power Limit 2.	★Enabled, Disabled
Power Limit 2	Power Limit 2 value in Milli Watts. BIOS will round to the nearest 1/8W when programming. If the value is 0, BIOS will program this value as 1.25*Processor Base Power (TDP). For 12.50w, enter 12500. Processor applies control policies such that the package power does not exceed this limit.	

6.3.5 Graphics Configuration

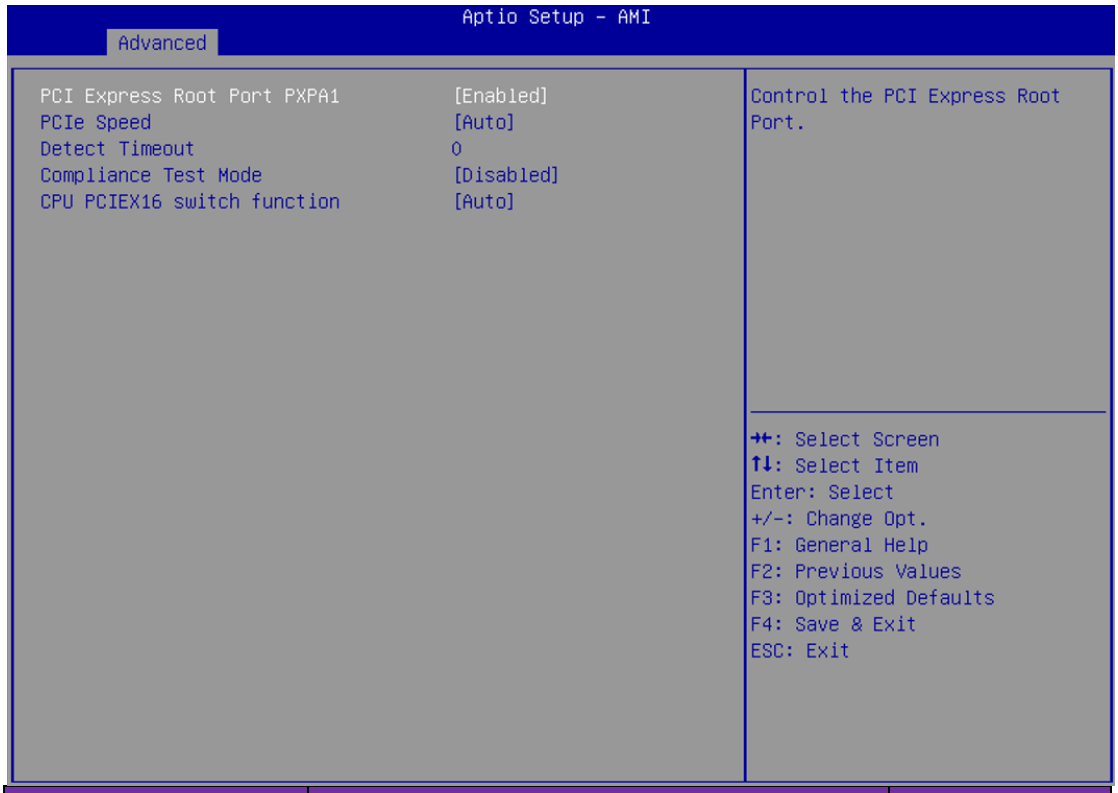
Feature	Description	Options
Primary Display	Select AUTO set IGD to be Primary Display if no external Graphics Device connected otherwise external Graphics Device detected on first PCIe port will be Primary Display or Select IGFX for IGD to be Primary Display or select FORCE for dual display.	★FORCE, Auto, IGFX
Internal Graphics	Keep IGFX enabled based on the setup options.	★Enabled, Disabled
RC6(Render Standby)	Check to enable render standby support.	★Enabled, Disabled

6.3.6 PCI Express Configuration



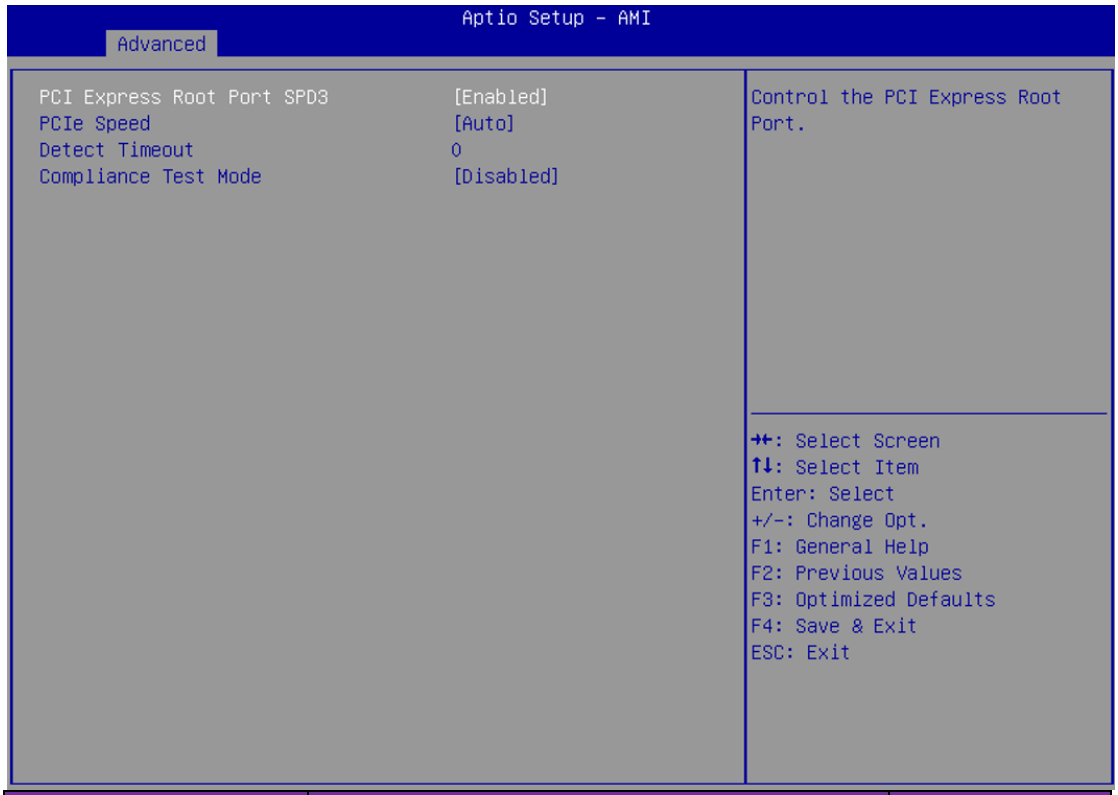
Feature	Description	Options
PCIEx16(G5)_1 Slot	Enable/Disable PCIEx16(G5)_1 Slot	
PCIEx4(G4)_1 Slot	Enable/Disable PCIEx4(G4)_1 Slot	
PCIEx4(G4)_2 Slot	Enable/Disable PCIEx4(G4)_2 Slot	
PCIEx4(G4)_3 Slot	Enable/Disable PCIEx4(G4)_3 Slot	
PCIEx4(G4)_4 Slot	Enable/Disable PCIEx4(G4)_4 Slot	
PCIE Devices Patch	PCIE Devices Patch	
PCH PCIE Clock Gating	PCH PCI Express Clock Gating Enable/Disable for all port	★Enabled, Disabled
PCH PCIE Power Gating	PCH PCI Express Power Gating Enable/Disable for all port	★Enabled, Disabled
Re-Size BAR Support	If system has Resizable BAR capable PCIe Devices, this option Enables or Disables Resizable BAR Support.	★Enabled, Disabled

PCIEx16(G5)_1 Slot



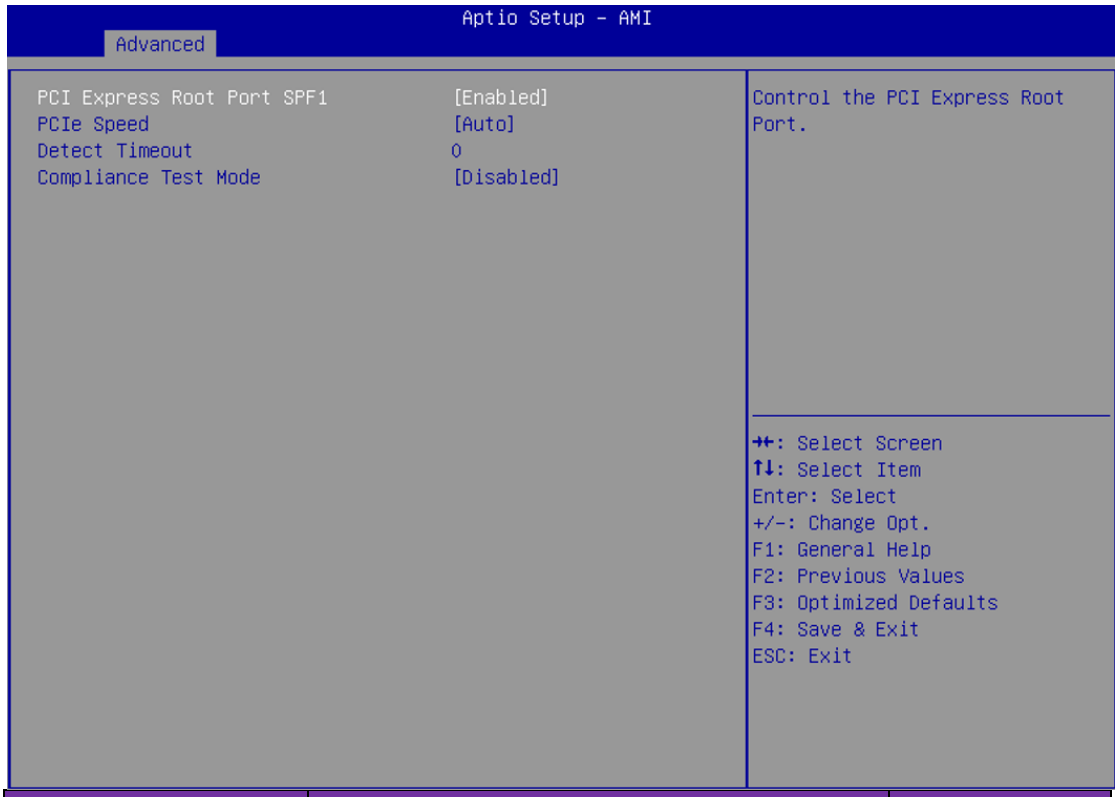
Feature	Description	Options
PCI Express Root Port PXPA1	Control the PCI Express Root Port.	★Enabled, Disabled
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3, Gen4, Gen5
Detect Timeout	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.	
Compliance Test Mode	Enable when using Compliance Load Board	Enabled, ★Disabled
CPU PCIEX16 switch function	CPU PCIEX16 switch function Auto/2x8/1x8+2x4	★Auto, 2x8, 1x8+2x4

PCIEx4(G4)_1 Slot



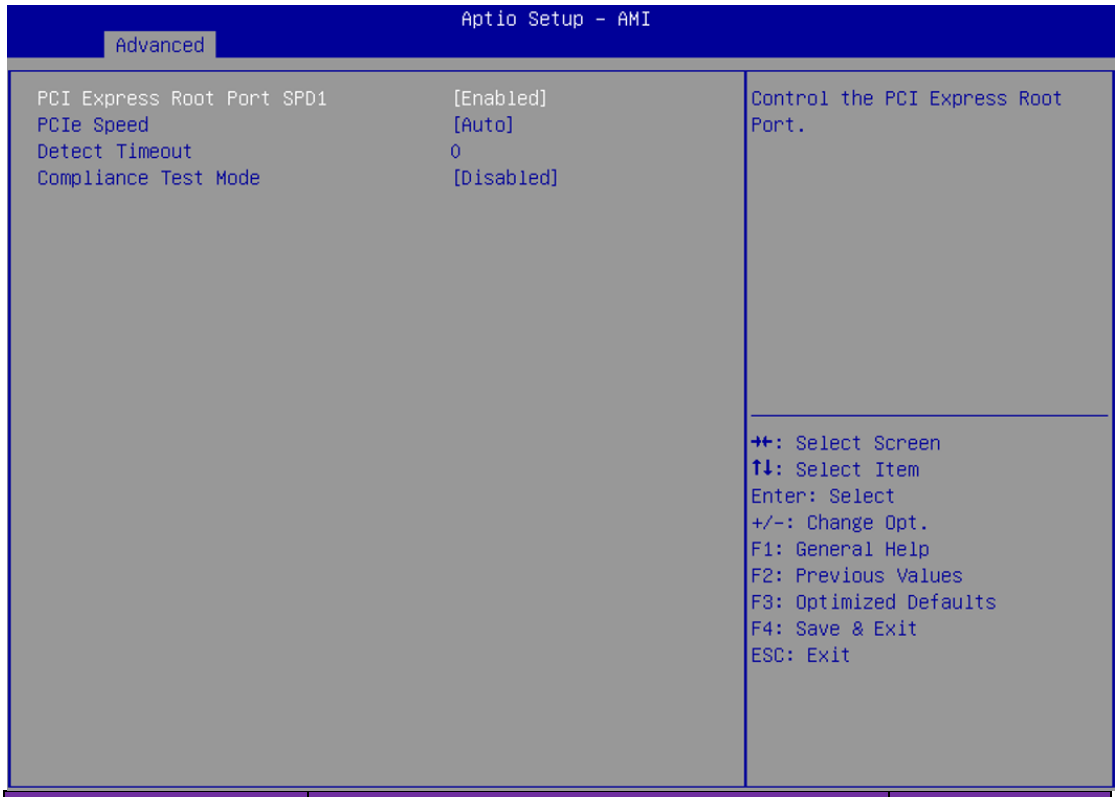
Feature	Description	Options
PCI Express Root Port SPD3	Control the PCI Express Root Port.	★Enabled, Disabled
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3, Gen4
Detect Timeout	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.	
Compliance Test Mode	Enable when using Compliance Load Board	Enabled, ★Disabled

PCIEx4(G4)_2 Slot



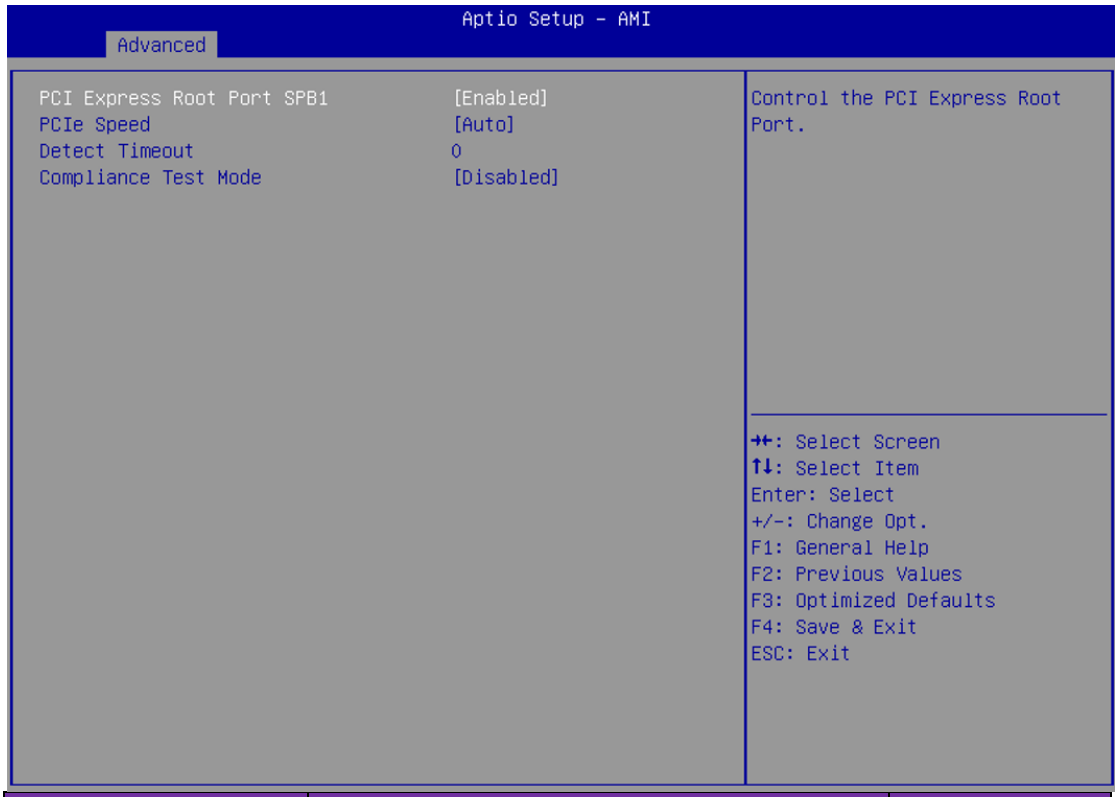
Feature	Description	Options
PCI Express Root Port SPF1	Control the PCI Express Root Port.	★Enabled, Disabled
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3, Gen4
Detect Timeout	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.	
Compliance Test Mode	Enable when using Compliance Load Board	Enabled, ★Disabled

PCIEx4(G4)_3 Slot



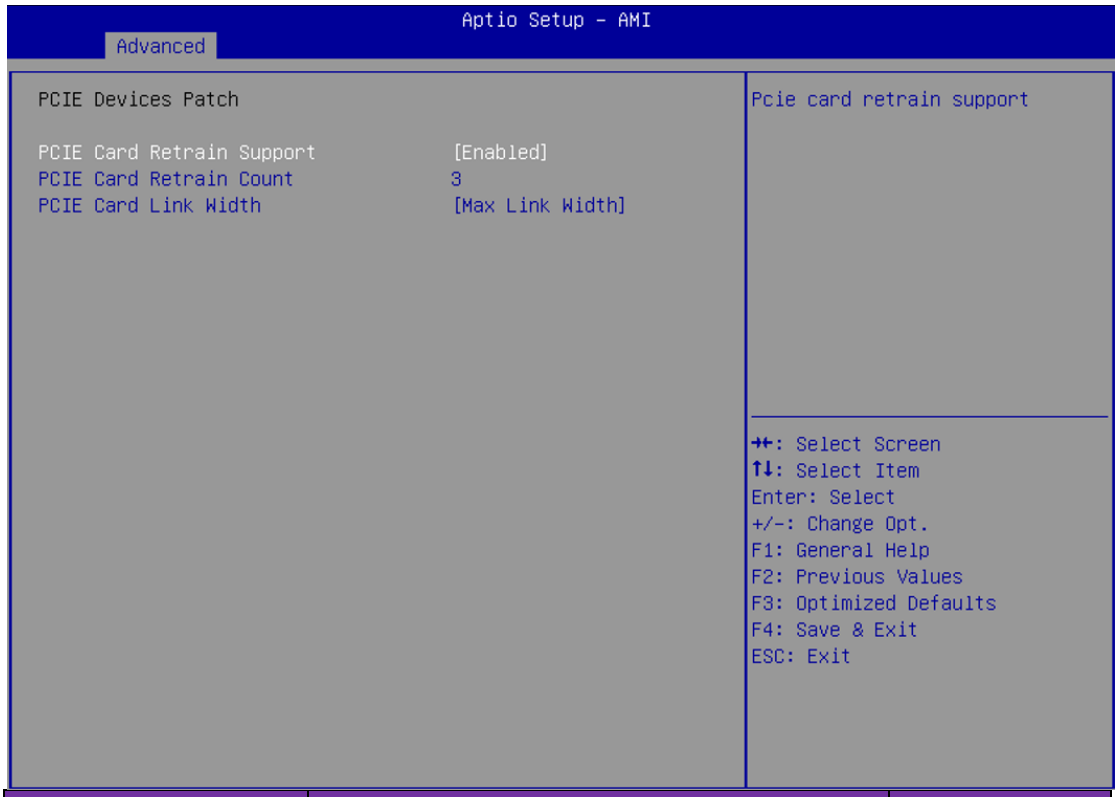
Feature	Description	Options
PCI Express Root Port SPD1	Control the PCI Express Root Port.	★Enabled, Disabled
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3, Gen4
Detect Timeout	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.	
Compliance Test Mode	Enable when using Compliance Load Board	Enabled, ★Disabled

PCIEx4(G4)_4 Slot



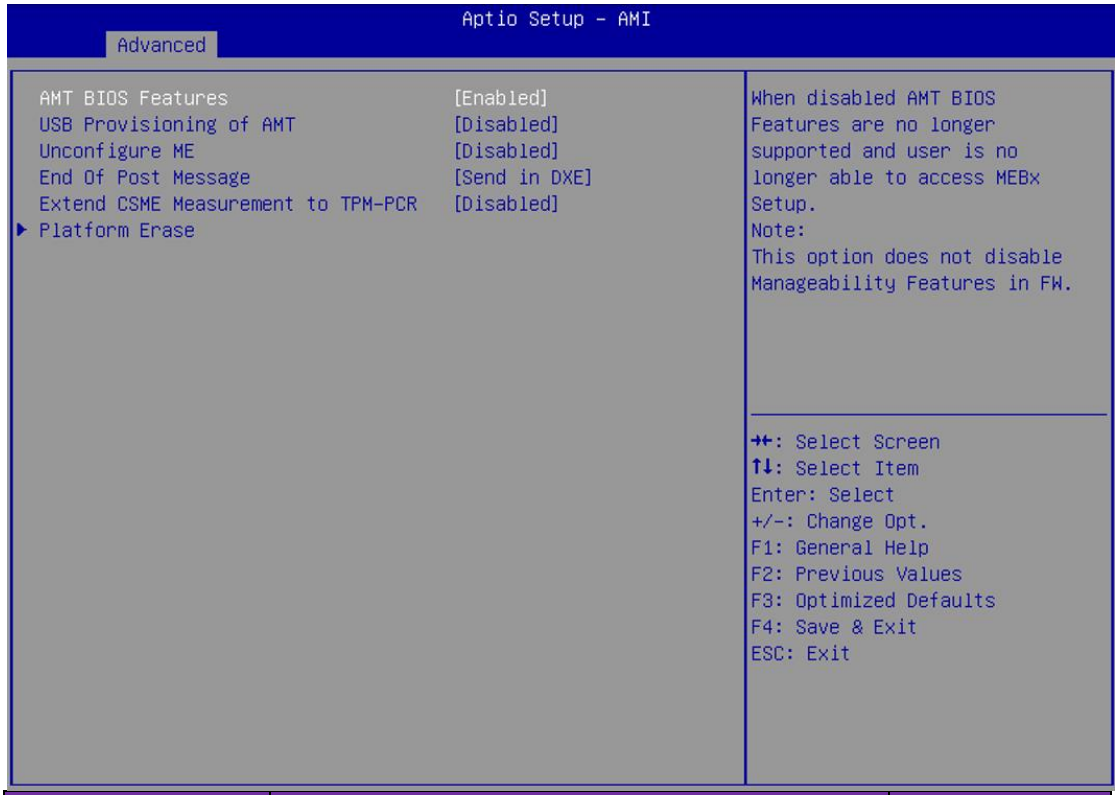
Feature	Description	Options
PCI Express Root Port SPB1	Control the PCI Express Root Port.	★Enabled, Disabled
PCIe Speed	Configure PCIe Speed	★Auto, Gen1, Gen2, Gen3, Gen4
Detect Timeout	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.	
Compliance Test Mode	Enable when using Compliance Load Board	Enabled, ★Disabled

PCIE Devices Patch



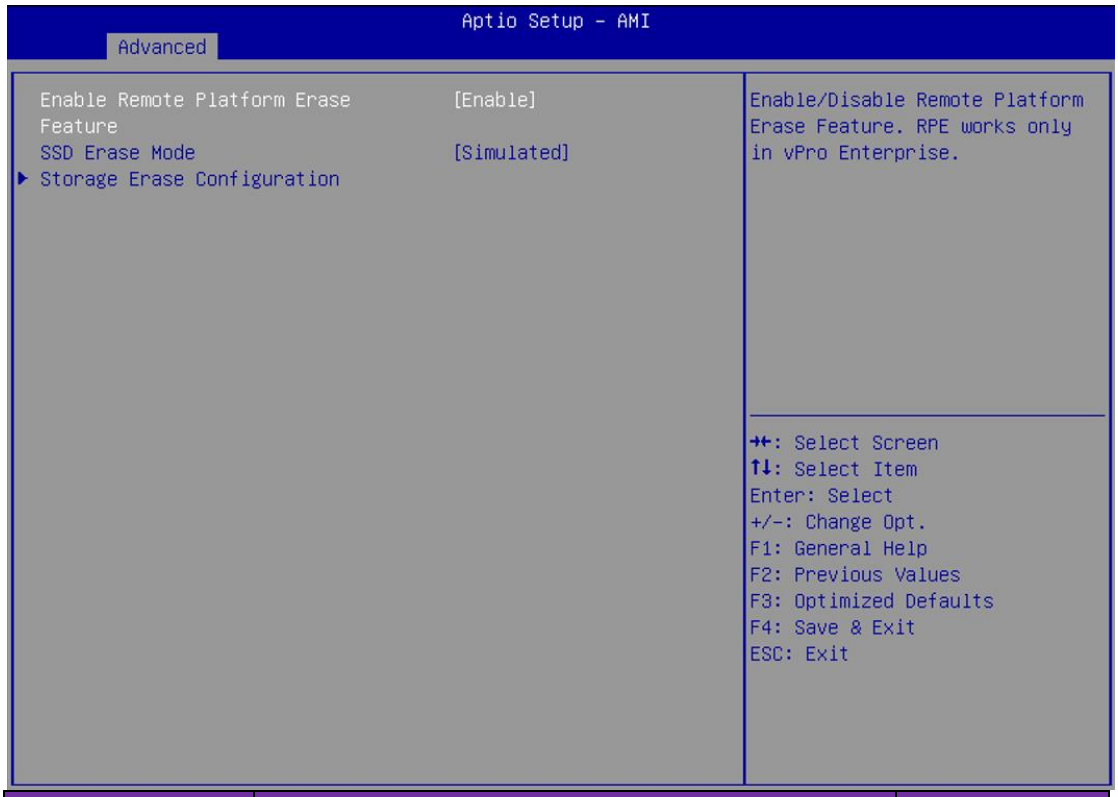
Feature	Description	Options
PCIE Card Retrain Support	Pcie card retrain support	Enabled, ★Disabled
PCIE Card Retrain Support [Enabled]		
PCIE Card Retrain Count	The Count of pcie card retrain	★3
PCIE Card Link Width	Set PCIE card link width	★Max Link Width, X1, X2, X4, X8, X16

6.3.7 AMT Configuration



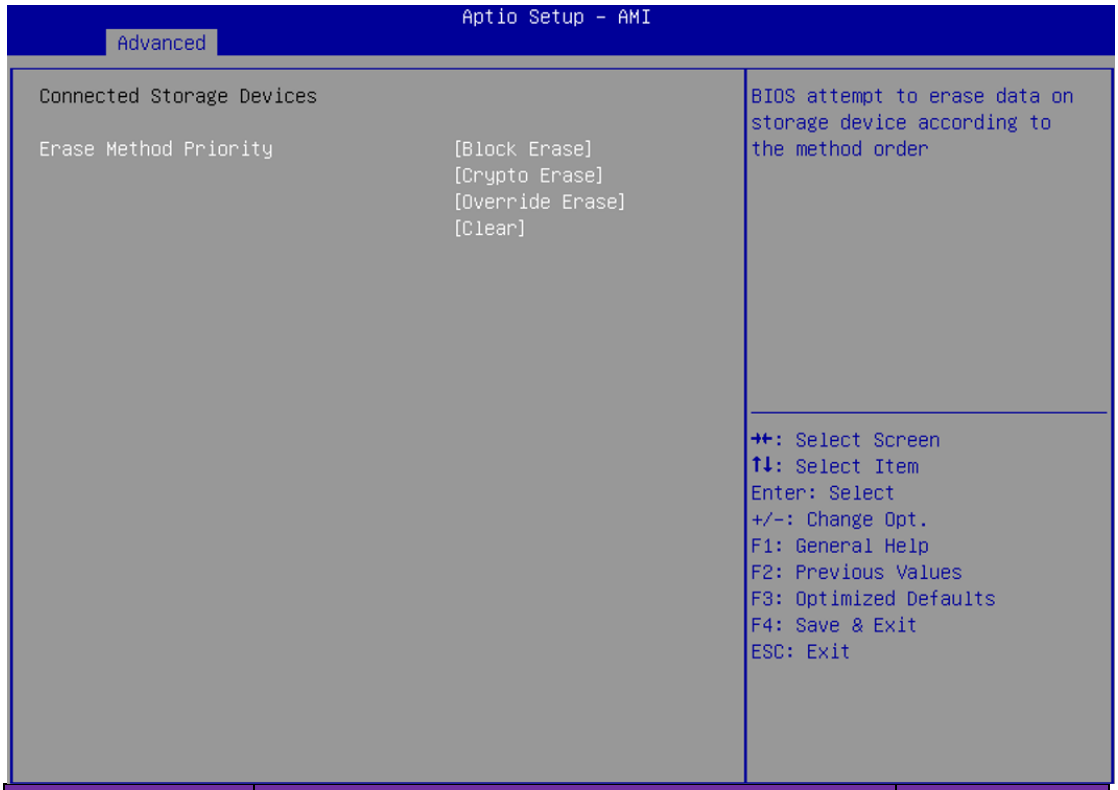
Feature	Description	Options
AMT BIOS Features	When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup. Note: This option does not disable Manageability Features in FW.	★Enabled, Disabled
USB Provisioning of AMT	Enable/Disable of AMT USB Provisioning.	Enabled, ★Disabled
Unconfigure ME	Unconfigure ME with resetting MEBx password to default on next boot.	Enabled, ★Disabled
End Of Post Message	Enable/Disable End of Post message sent to ME	★Send in DXE, Disabled
Extend CSME Measurement to TPM-PCR	Enable/Disable Extend CSME Measurement to TPM-PCR[0] and AMT Config to TPM-PCR[1]	Enabled, ★Disabled
Platform Erase	Platform Erase settings	

Platform Erase



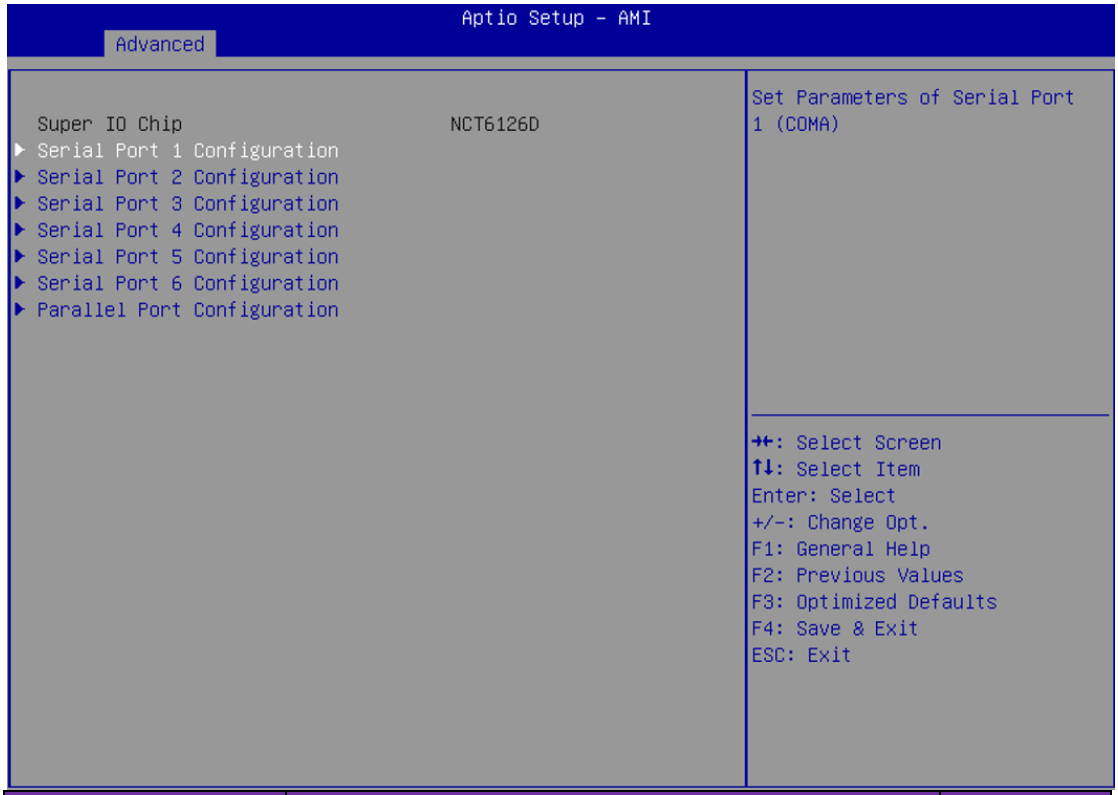
Feature	Description	Options
Enable Remote Platform Erase Feature	Enable/Disable Remote Platform Erase Feature. RPE works only in vPro Enterprise.	★Enable, Disable
SSD Erase Mode	Change RPE SSD Erase Action behavior: Simulated: Performs RPE SSD Erase flow without erasing SSD Real: Erase SSD.	★Simulated, Real
Storage Erase Configuration	Storage Erase Configuration menu	

Storage Erase Configuration



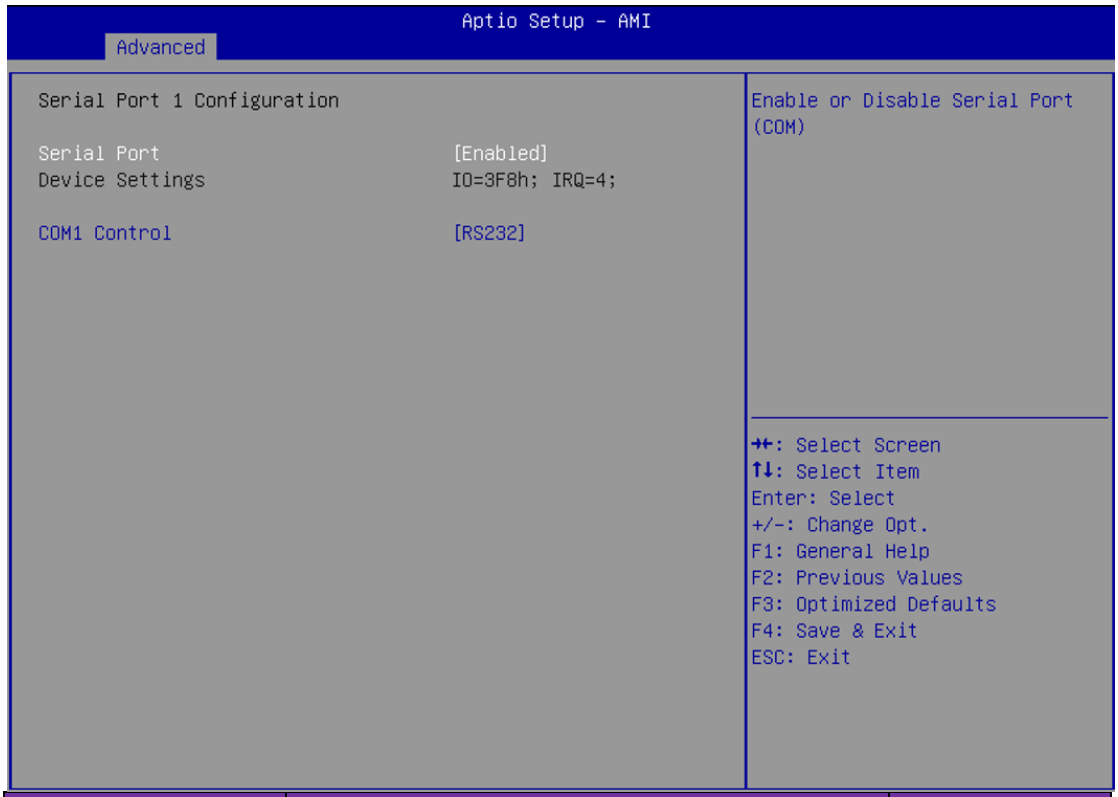
Feature	Description	Options
Erase Method Priority	BIOS attempt to erase data on storage device according to the method order	Block Erase Crypto Erase Override Erase Clear

6.3.9 Super IO Configuration



Feature	Description	Options
Serial Port 1 Configuration	Set Parameters of Serial Port1(COMA)	
Serial Port 2 Configuration	Set Parameters of Serial Port2(COMB)	
Serial Port 3 Configuration	Set Parameters of Serial Port3(COMC)	
Serial Port 4 Configuration	Set Parameters of Serial Port4(COMD)	
Serial Port 5 Configuration	Set Parameters of Serial Port5(COME)	
Serial Port 6 Configuration	Set Parameters of Serial Port6(COMF)	
Parallel Port Configuration	Set Parameters of Parallel Port(LPT/LPTE)	

Serial Port 1 Configuration

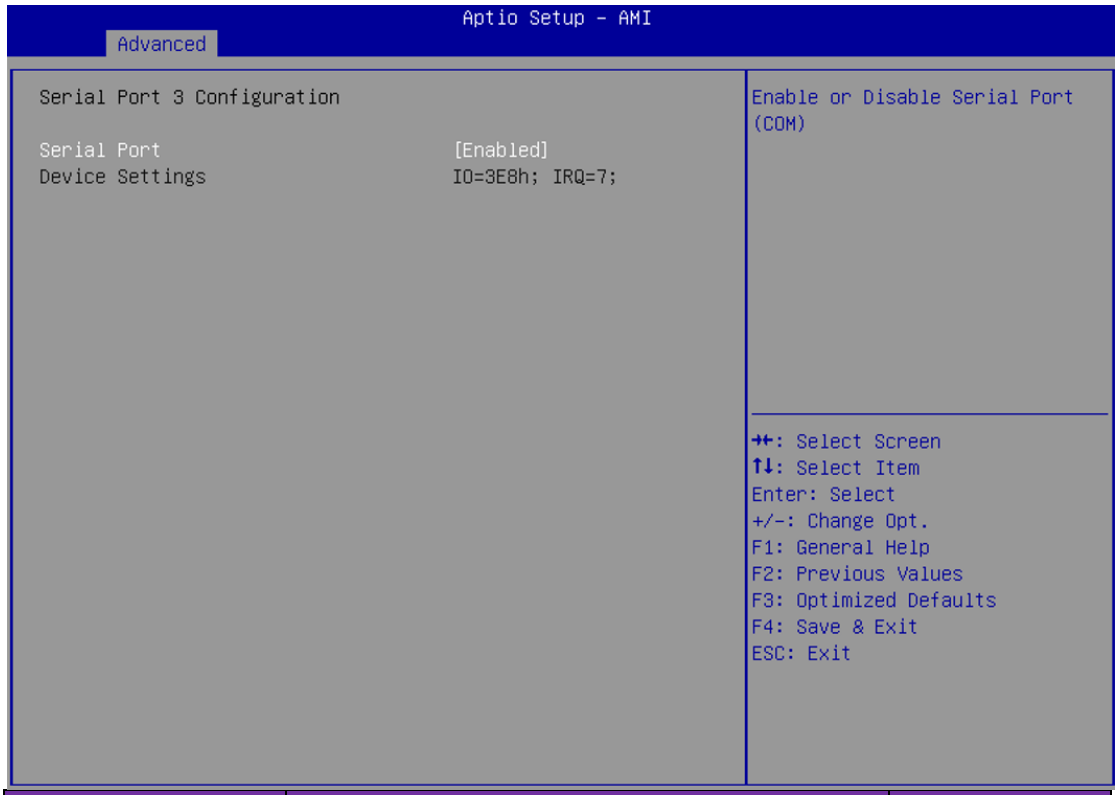


Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	★Enabled, Disabled
COM1 Control	Select COM1 mode. RS232, RS422 or RS485	★RS232, RS422, RS485

Serial Port 2 Configuration

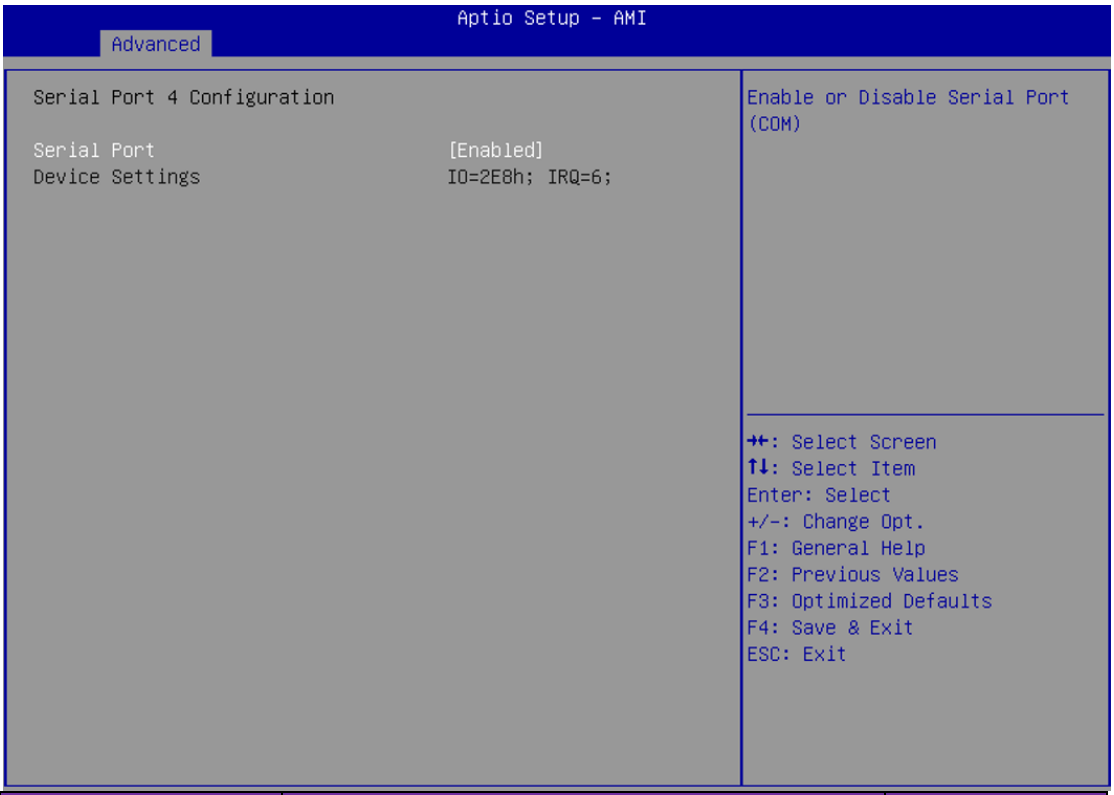
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	★Enabled, Disabled
COM2 Control	Select COM2 mode. RS232, RS422 or RS485	★RS232, RS422, RS485

Serial Port 3 Configuration



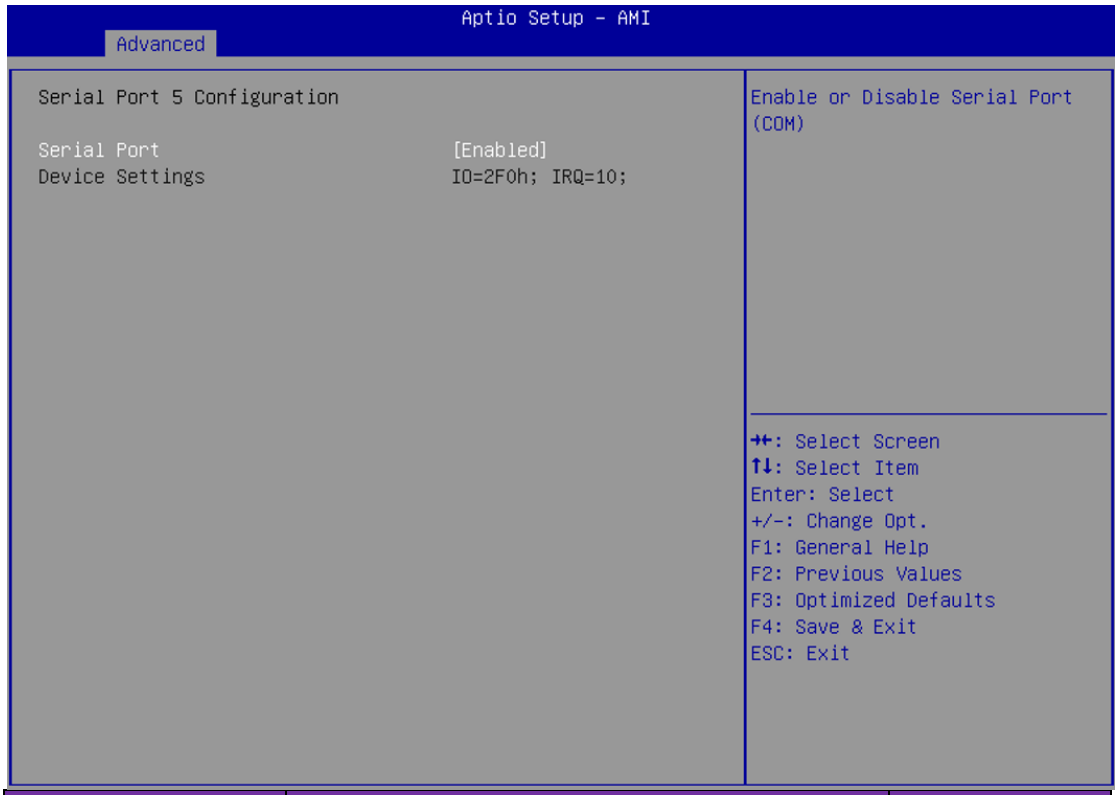
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	★Enabled, Disabled

Serial Port 4 Configuration



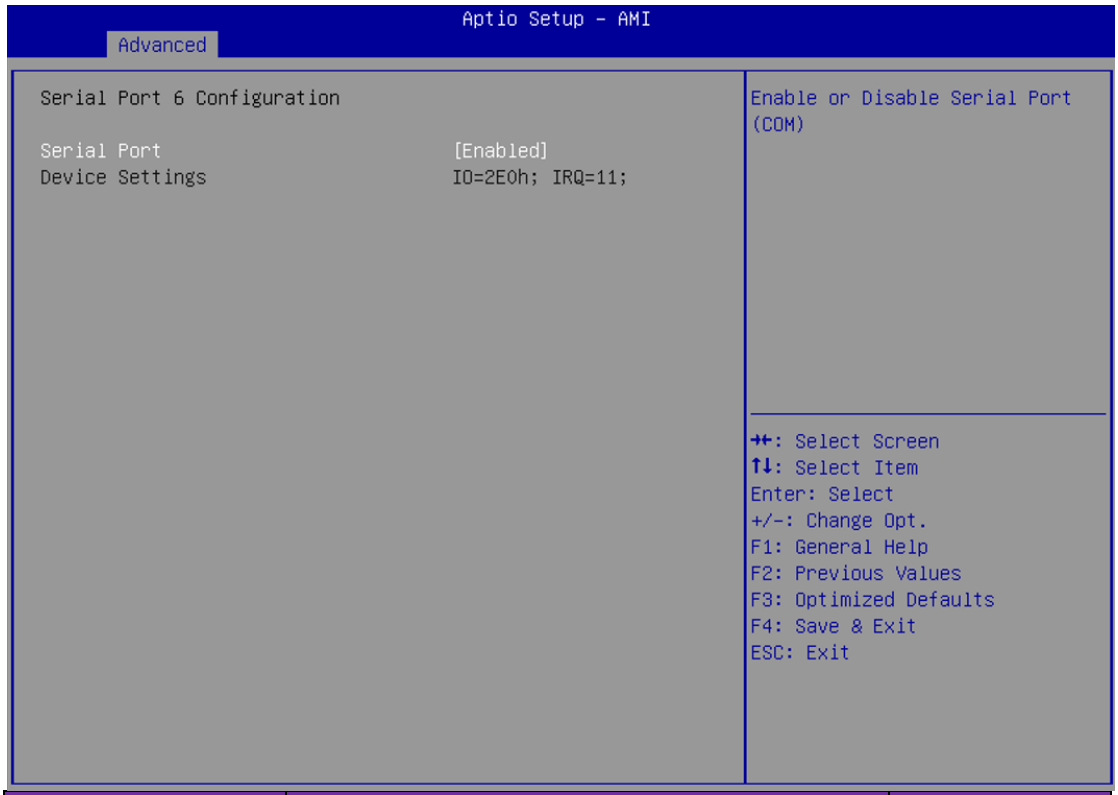
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	★Enabled, Disabled

Serial Port 5 Configuration



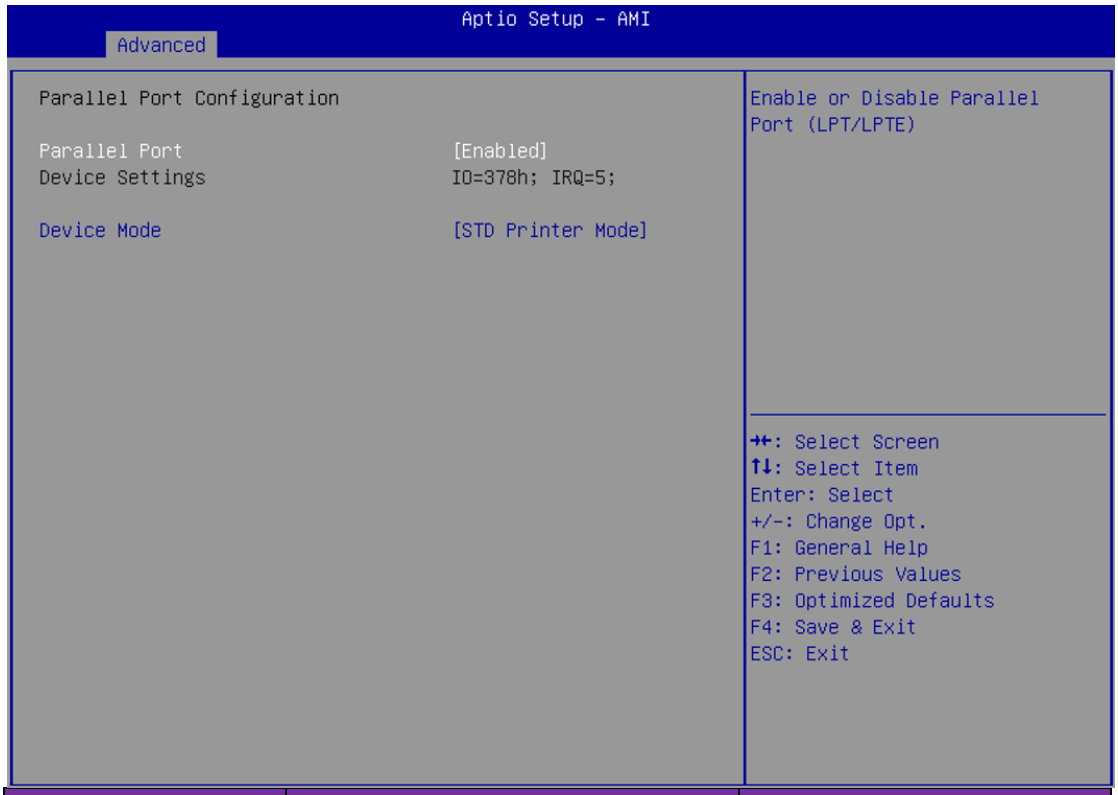
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	★Enabled, Disabled

Serial Port 6 Configuration



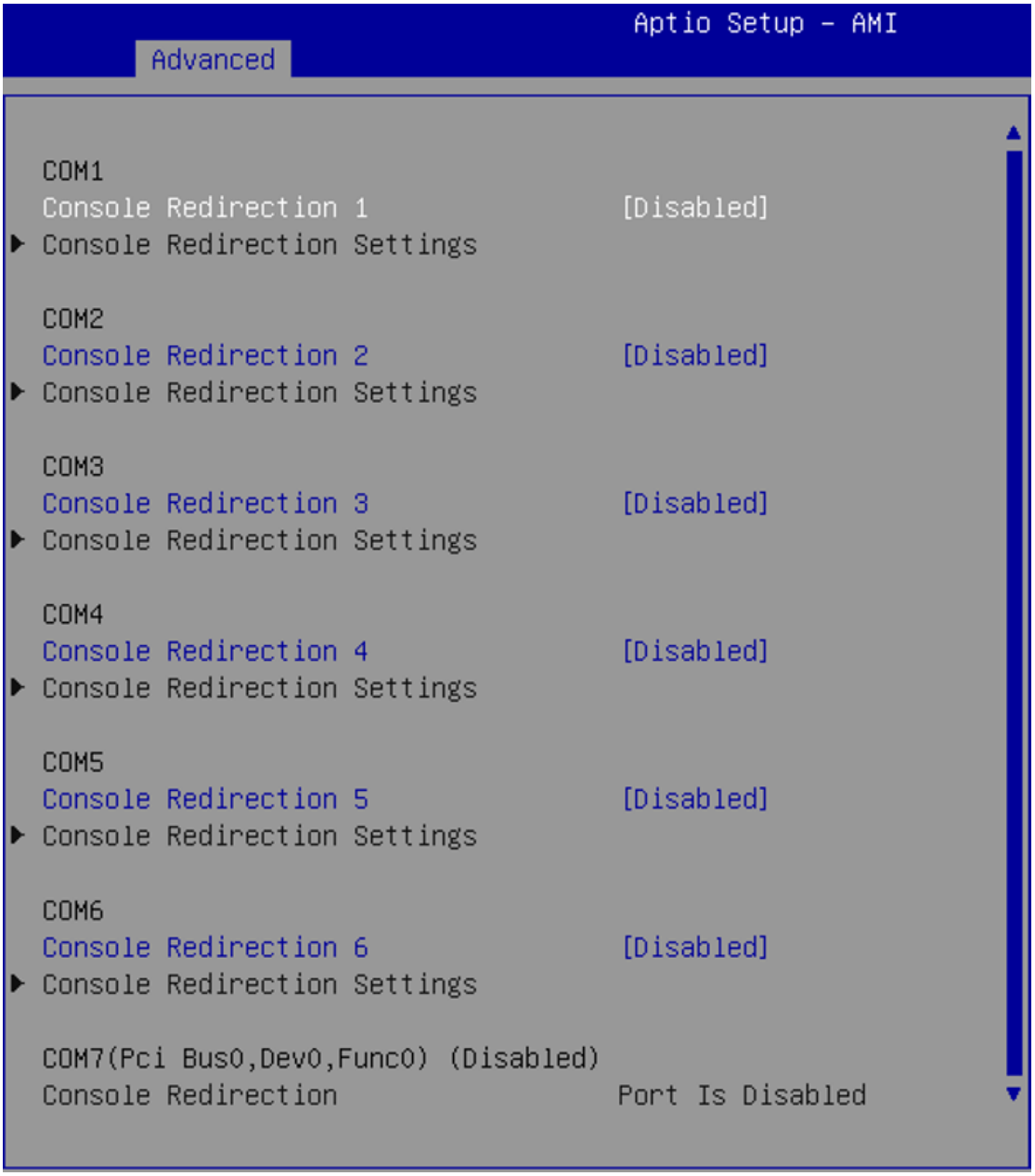
Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	★Enabled, Disabled

Parallel Port Configuration



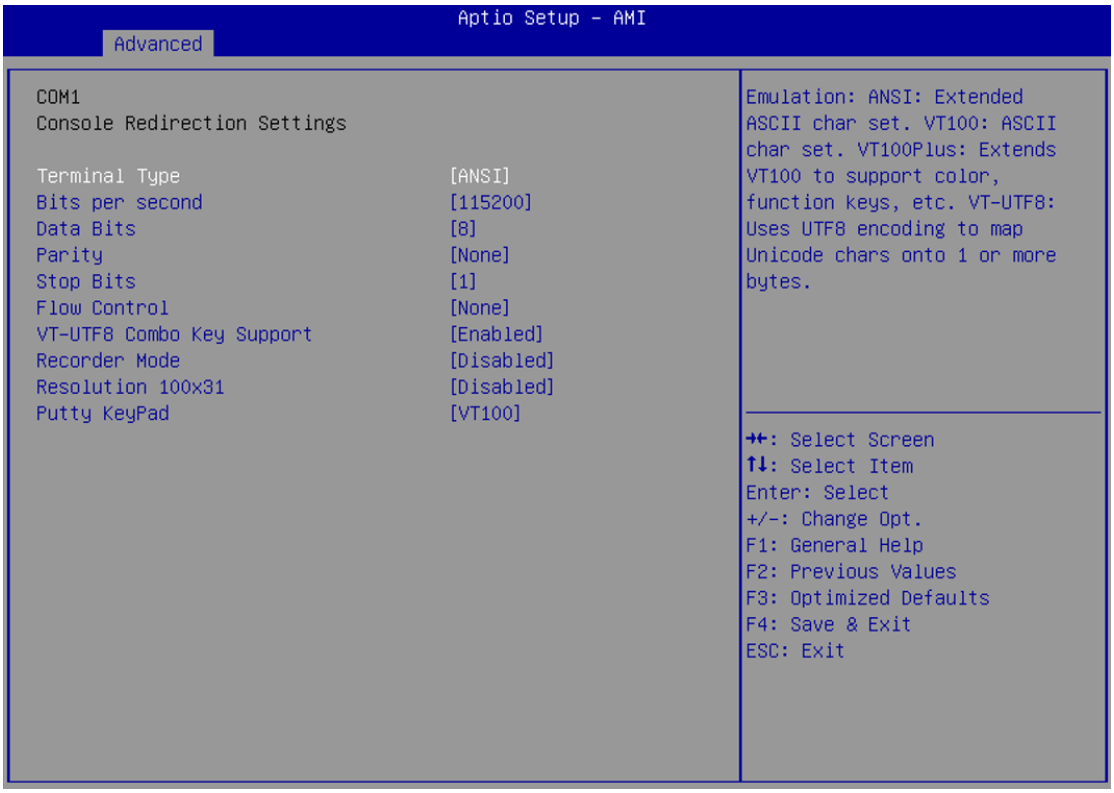
Feature	Description	Options
Parallel Port	Enable or Disable Parallel Port (LPT/LPTE)	★Enabled, Disabled
Device Mode	Change the Printer Port mode.	★STD Printer Mode, SPP Mode, EPP-1.9 and SPP Mode, EPP-1.7 and SPP Mode, ECP Mode, ECP and EPP 1.9 Mode, ECP and EPP 1.7 Mode

6.3.10 Serial Console Redirection



Feature	Description	Options
Console Redirection	Console Redirection Enable or Disable.	Enabled, ★Disabled
Console Redirection Settings	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.	

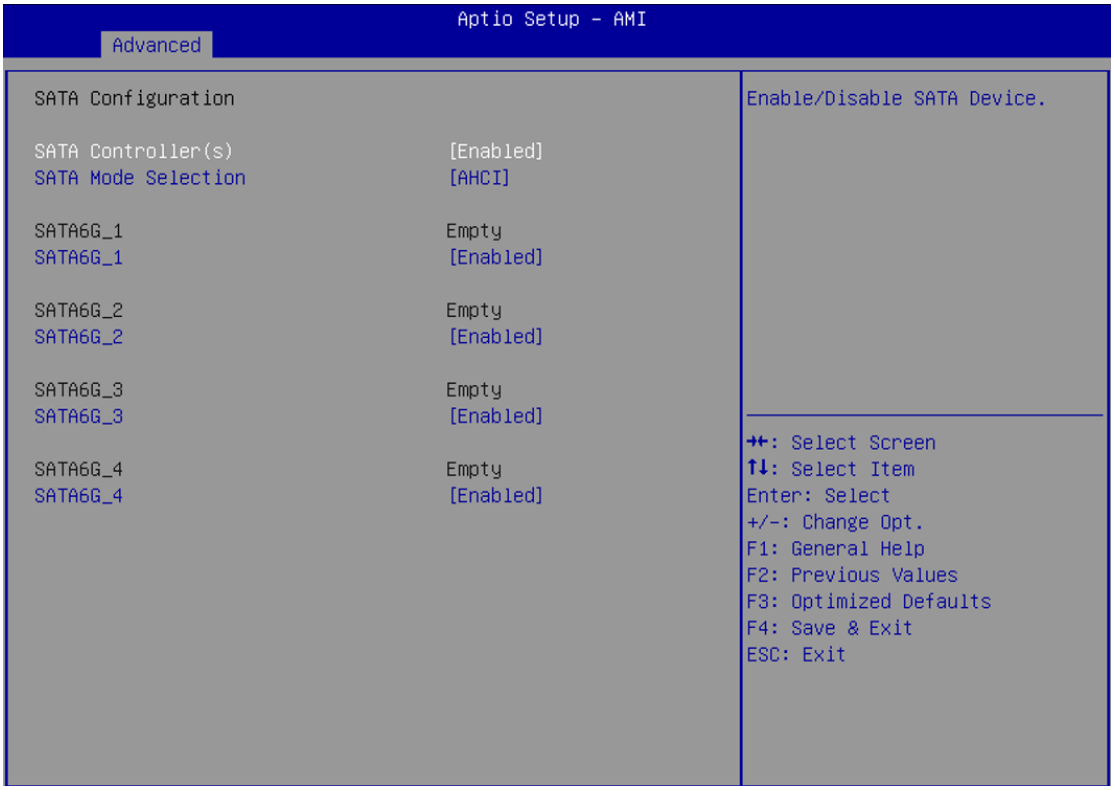
Console Redirection Settings



Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★ANSI, VT100, VT100Plus, VT-UTF8
Bits per second	Selects Serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.	★115200, 9600, 19200, 38400, 57600, 230400, 460800, 921600
Data bits	Data bits	★8, 7
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★None, Even, Odd, Mark, Space
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1, 2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	★None, Hardware RTS/CTS

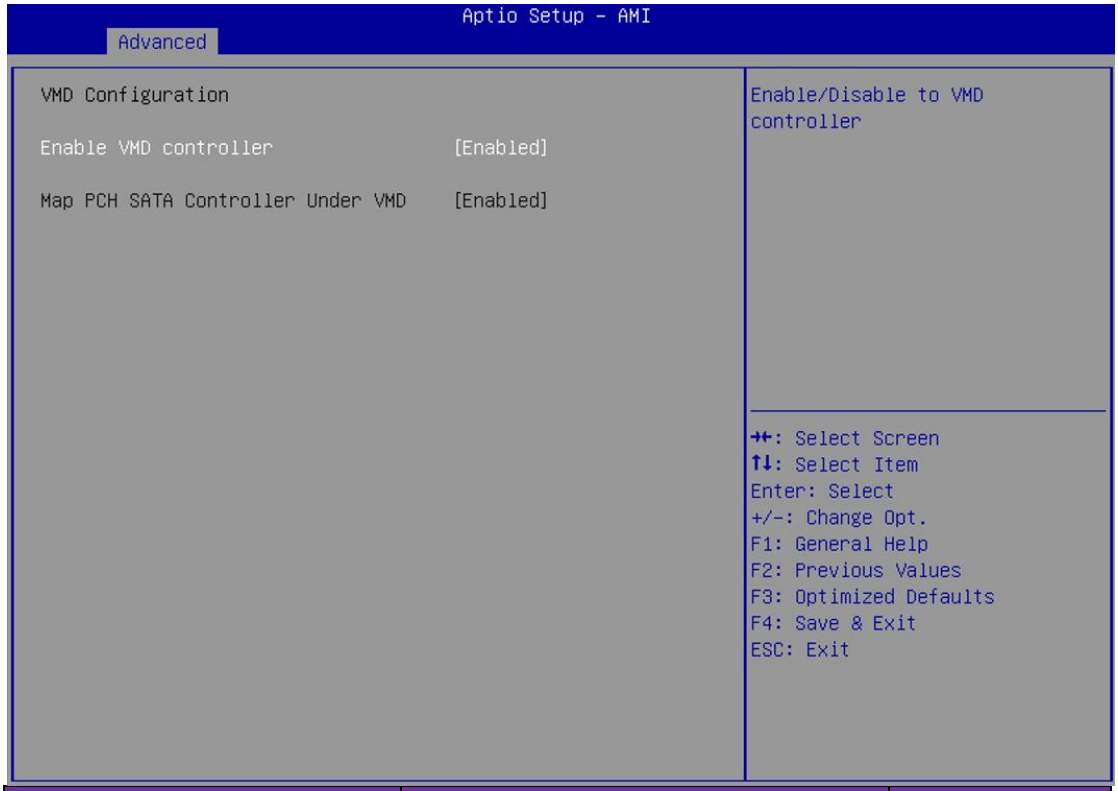
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	★Enabled, Disabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★Disabled, Enabled
Putty KeyPad	Select FunctionKey and KeyPad on Putty.	★VT100, LINUX, XTERMR6, SCO, ESCN, VT400

6.3.11 SATA Configuration



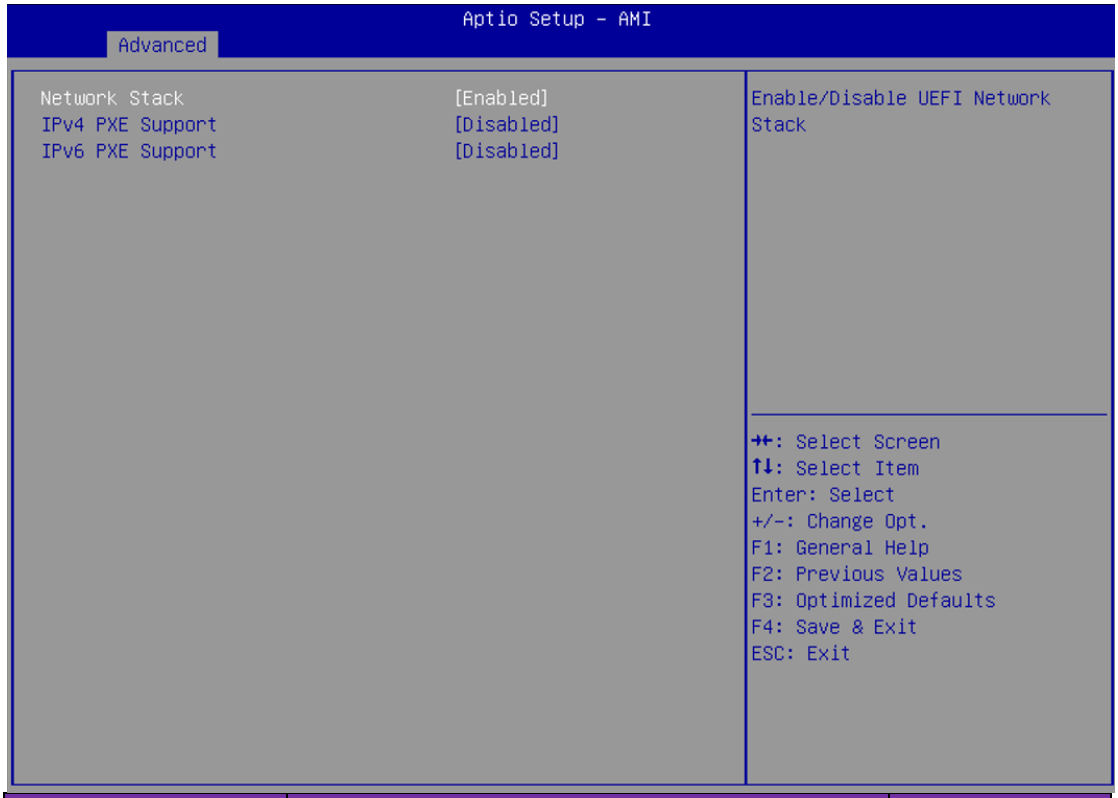
Feature	Description	Options
SATA Controller(s)	Enable/Disable SATA Device.	★Enabled, Disabled
SATA Mode Selection	Determines how SATA controller(s) operate.	★AHCI
SATA6G_1	Enable or Disable SATA Port	★Enabled, Disabled
SATA6G_2	Enable or Disable SATA Port	★Enabled, Disabled
SATA6G_3	Enable or Disable SATA Port	★Enabled, Disabled
SATA6G_4	Enable or Disable SATA Port	★Enabled, Disabled

6.3.12 VMD setup menu



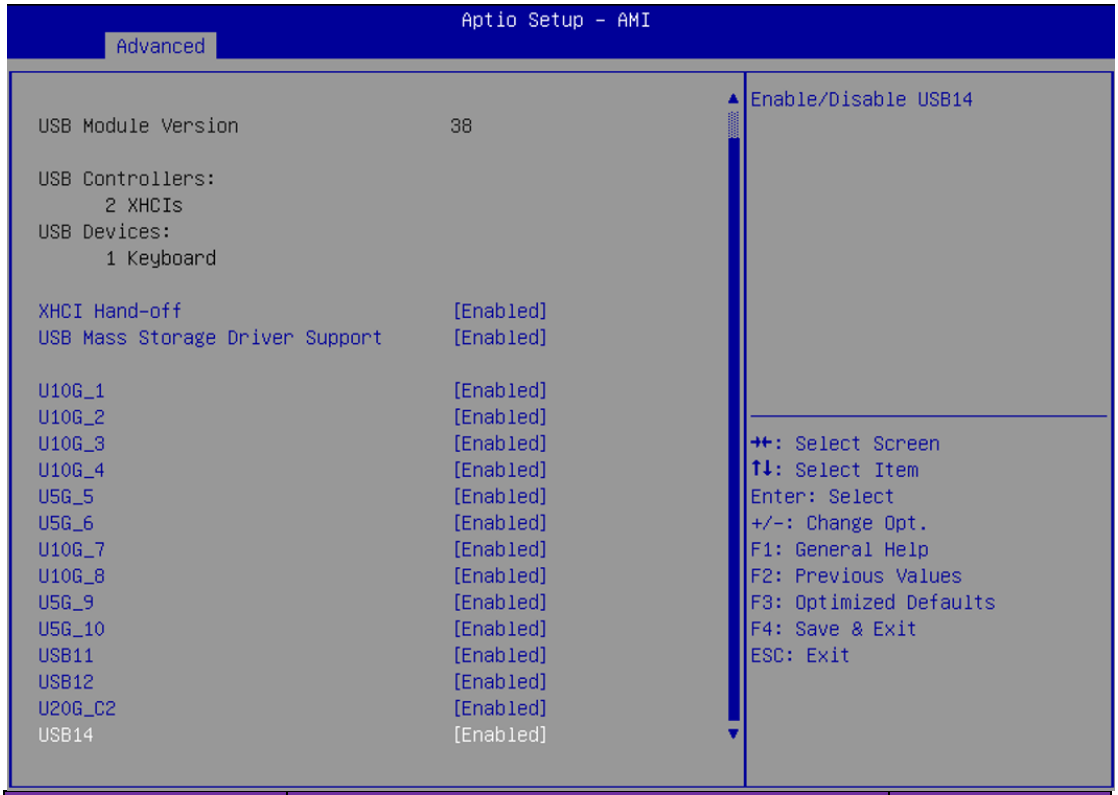
Feature	Description	Options
Enable VMD controller	Enable/Disable to VMD controller	★Disabled, Enabled
Enable VMD controller [Enabled]		
Map PCH SATA Controller Under VMD		★Enabled

6.3.13 Network Stack Configuration



Feature	Description	Options
Network Stack	Enable/Disable UEFI Network Stack	★Disabled, Enabled
Network Stack [Enabled]		
IPv4 PXE Support	Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.	★Disabled, Enabled
IPv6 PXE Support	Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.	★Disabled, Enabled

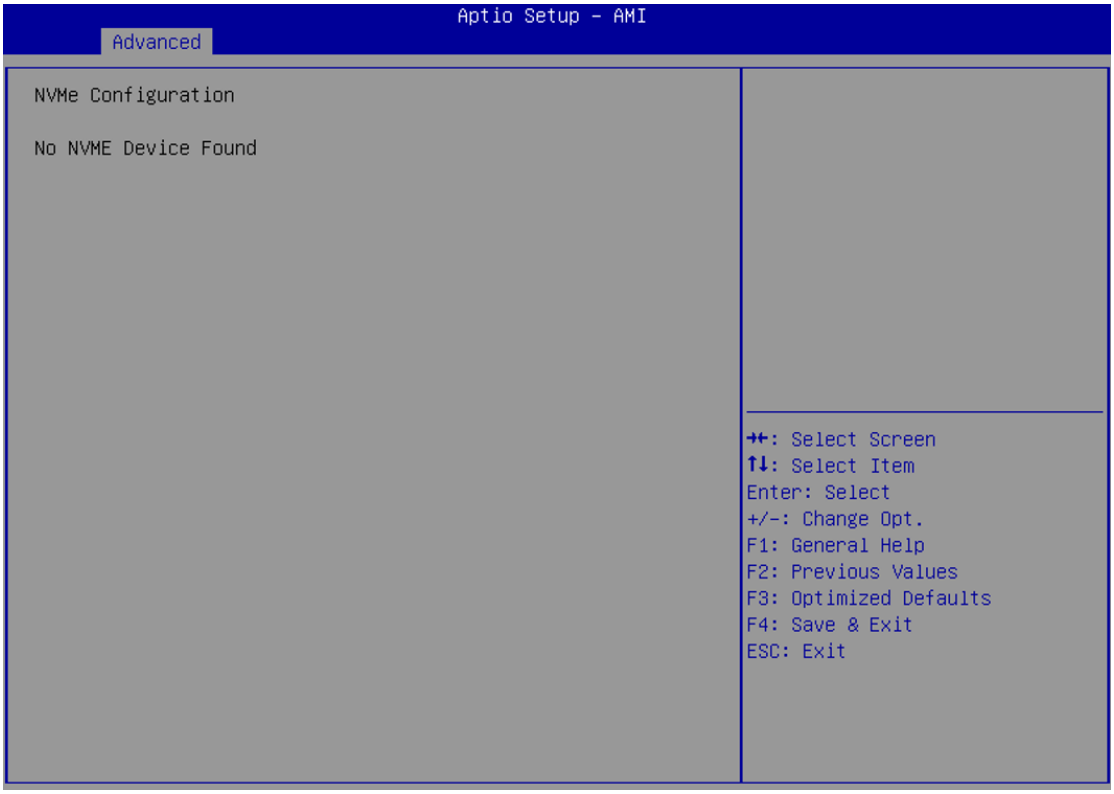
6.3.14 USB Configuration



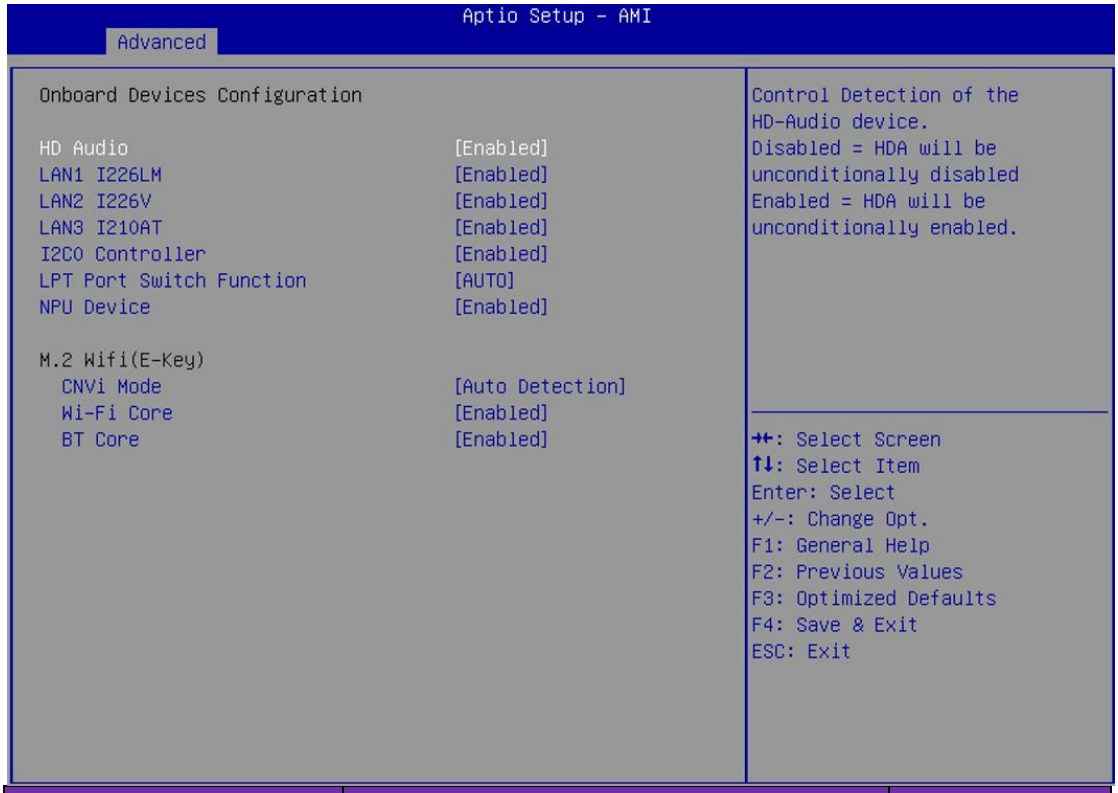
Feature	Description	Options
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.	★Enabled, Disabled
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support.	★Enabled, Disabled
U10G_1	Enable/Disable U10G_1	★Enabled, Disabled
U10G_2	Enable/Disable U10G_2	★Enabled, Disabled
U10G_3	Enable/Disable U10G_3	★Enabled, Disabled
U10G_4	Enable/Disable U10G_4	★Enabled, Disabled
U5G_5	Enable/Disable U5G_5	★Enabled, Disabled
U5G_6	Enable/Disable U5G_6	★Enabled, Disabled
U10G_7	Enable/Disable U10G_7	★Enabled, Disabled
U10G_8	Enable/Disable U10G_8	★Enabled, Disabled
U5G_9	Enable/Disable U5G_9	★Enabled, Disabled
U5G_10	Enable/Disable U5G_10	★Enabled, Disabled

USB11	Enable/Disable USB11	★Enabled, Disabled
USB12	Enable/Disable USB12	★Enabled, Disabled
U20G_C2	Enable/Disable U20G_C2	★Enabled, Disabled
USB14	Enable/Disable USB14	★Enabled, Disabled

6.3.15 NVMe Configuration



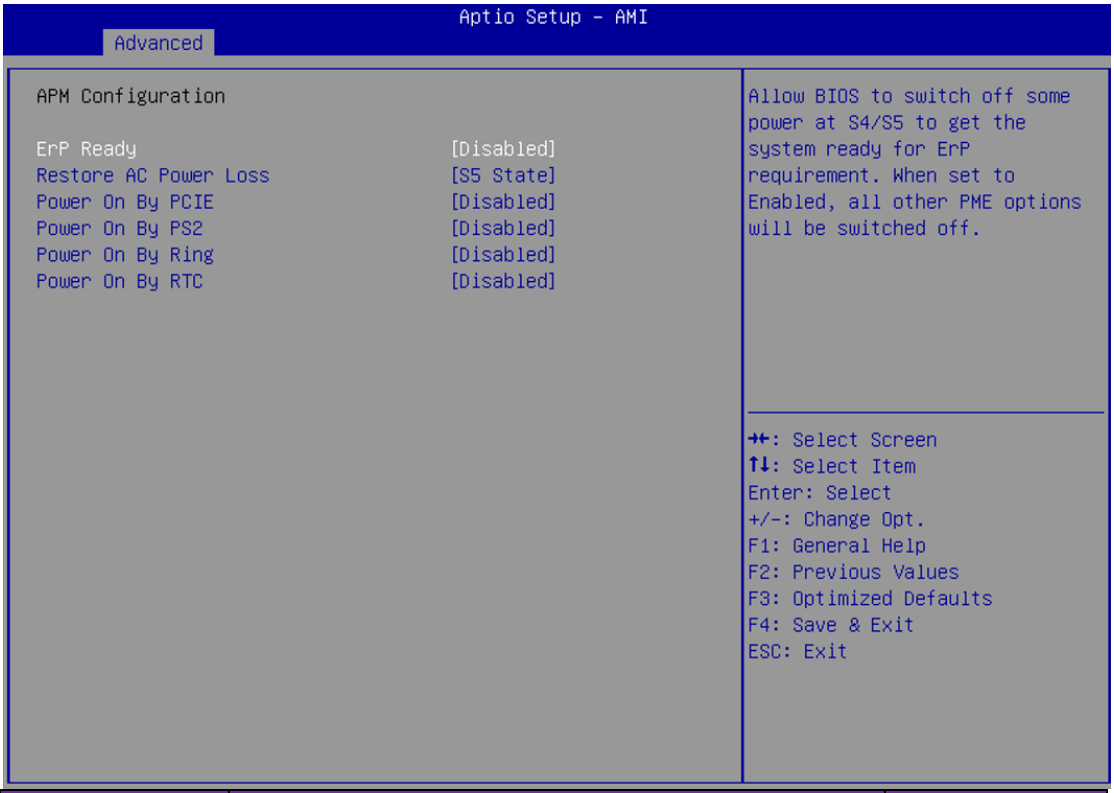
6.3.16 Onboard Device Configuration



Feature	Description	Options
HD Audio	Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally enabled.	★Enabled, Disabled
LAN1 I226LM	Enable/Disable LAN1 I226LM	★Enabled, Disabled
LAN2 I226V	Enable/Disable LAN2 I226V	★Enabled, Disabled
LAN3 I210AT	Enable/Disable LAN3 I210AT	★Enabled, Disabled
I2C0 Controller	Enables/Disables Seriallo Controller If given device is Function 0 PSF disabling is skipped. PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.	★Enabled, Disabled
LPT Port Switch Function	LPT Port Switch Function AUTO/LPT/GPIO	★AUTO, LPT, GPIO
NPU Device	Enable/Disable NPU (Neural Processing Unit) Device.	★Enabled, Disabled
CNVi Mode	This option configures Connectivity. [Auto Detection] means that if Discrete solution is discovered it will be enabled by default. Otherwise Integrated solution (CNVi) will be enabled; [Disable Integrated] disables Integrated Solution.	★Auto Detection, Disable Integrated
Wi-Fi Core	This is an option intended to Enable/Disable Wi-Fi Core in CNVi	★Enabled, Disabled

BT Core	This is an option intended to Enable/Disable BT Core in CNVi	★Enabled, Disabled

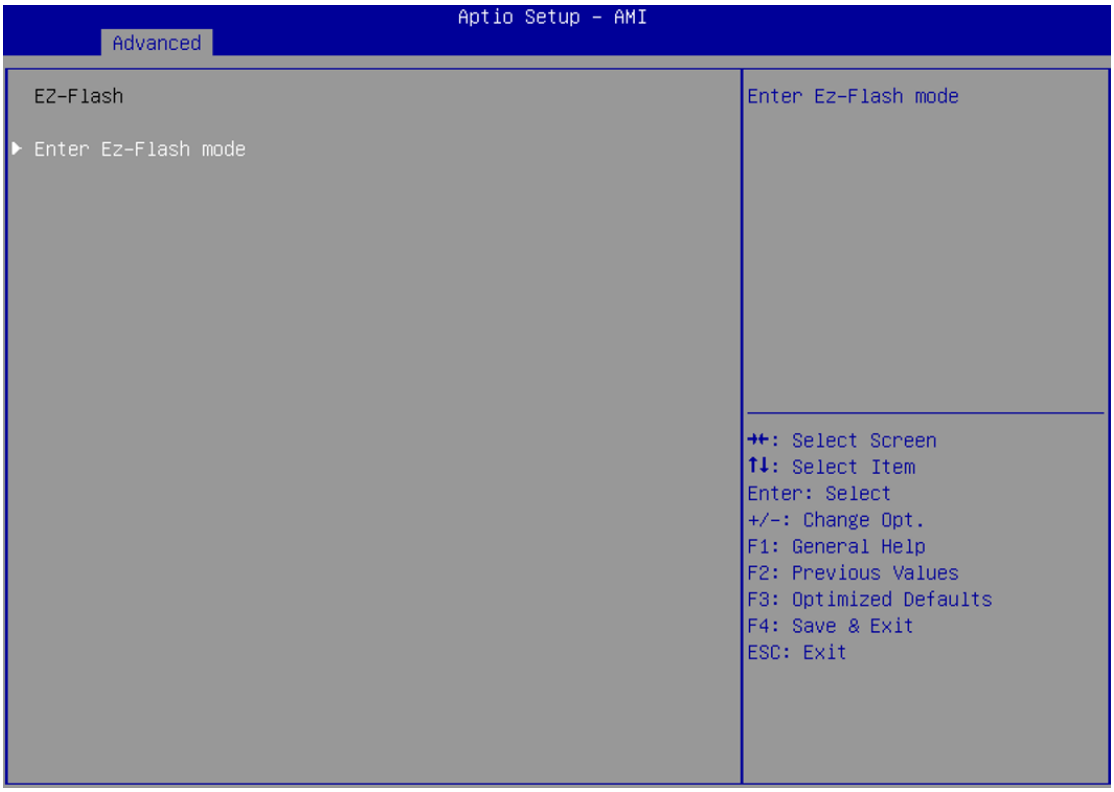
6.3.17 APM Configuration



Feature	Description	Options
ErP Ready	Allow BIOS to switch off some power at S4/S5 to get the system ready for ErP requirement. When set to Enabled, all other PME options will be switched off.	★Disabled, Enabled
Restore AC Power Loss	Select AC power state when power is re-applied after a power failure.	★S5 State, S0 State
Power On By PCIE	Enable or disable the Wake-on-LAN function of the onboard LAN controller or other installed PCIE LAN devices.	★Disabled, Enabled
Power On By PS2	Enable/disable resume from S5 via PS2	★Disabled, Enabled
Power On By Ring	Power On By Ring	★Disabled, Enabled
Power On By RTC	Select whether to enable Wake Up on Alarm, to turn on your system on a special day of the month, special day of the week or daily. NOTE: Values in these fields may be overwritten by the operating system.	★Disabled, Single event, Daily event, Weekly event, Monthly event
Power On By RTC [Single event]		
Wake up hour	Select 0-23 For example enter 3 for 3am and 15 for 3pm	
Wake up minute	Select 0-59 for Minute	

Wake up second	Select 0-59 for Second	
Power On By RTC [Daily event]		
Wake up hour	Select 0-23 For example enter 3 for 3am and 15 for 3pm	
Wake up minute	Select 0-59 for Minute	
Wake up second	Select 0-59 for Second	
Power On By RTC [Weekly event]		
Alarm day of Week	Select the day of the week when the system is to wake up.	★Sunday, Monday, Tuesday, Wednesday, Thursday, Friday, Saturday
Wake up hour	Select 0-23 For example enter 3 for 3am and 15 for 3pm	
Wake up minute	Select 0-59 for Minute	
Wake up second	Select 0-59 for Second	
Power On By RTC [Monthly event]		
Day of the Month	RTC Alarm Date (Days)	★15
Wake up hour	Select 0-23 For example enter 3 for 3am and 15 for 3pm	
Wake up minute	Select 0-59 for Minute	
Wake up second	Select 0-59 for Second	

6.3.18 EZ-Flash

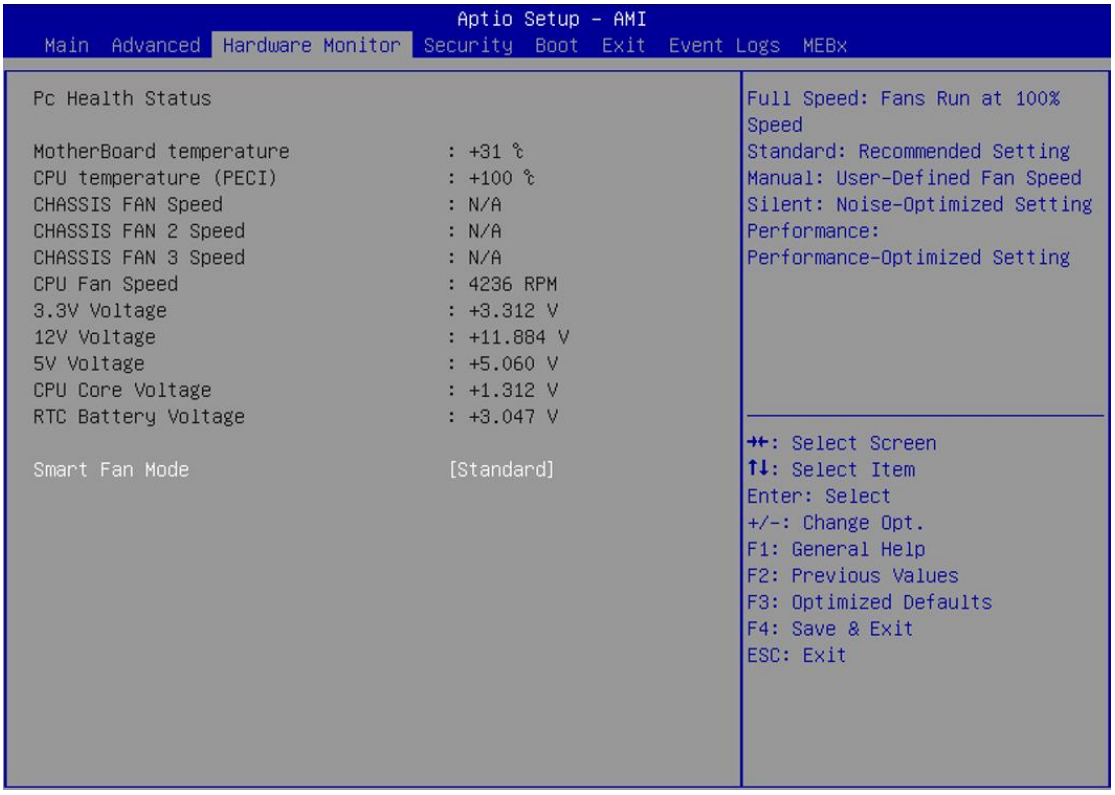


Feature	Description	Options
Enter Ez-Flash mode	In this mode, select a BIOS update file from your drive to update	

6.3.19 Preserve BIOS option method

Feature	Description	Options
Preserve BIOS option	Enabled/Disabled preserve BIOS option after flash BIOS	★Disabled, Enabled

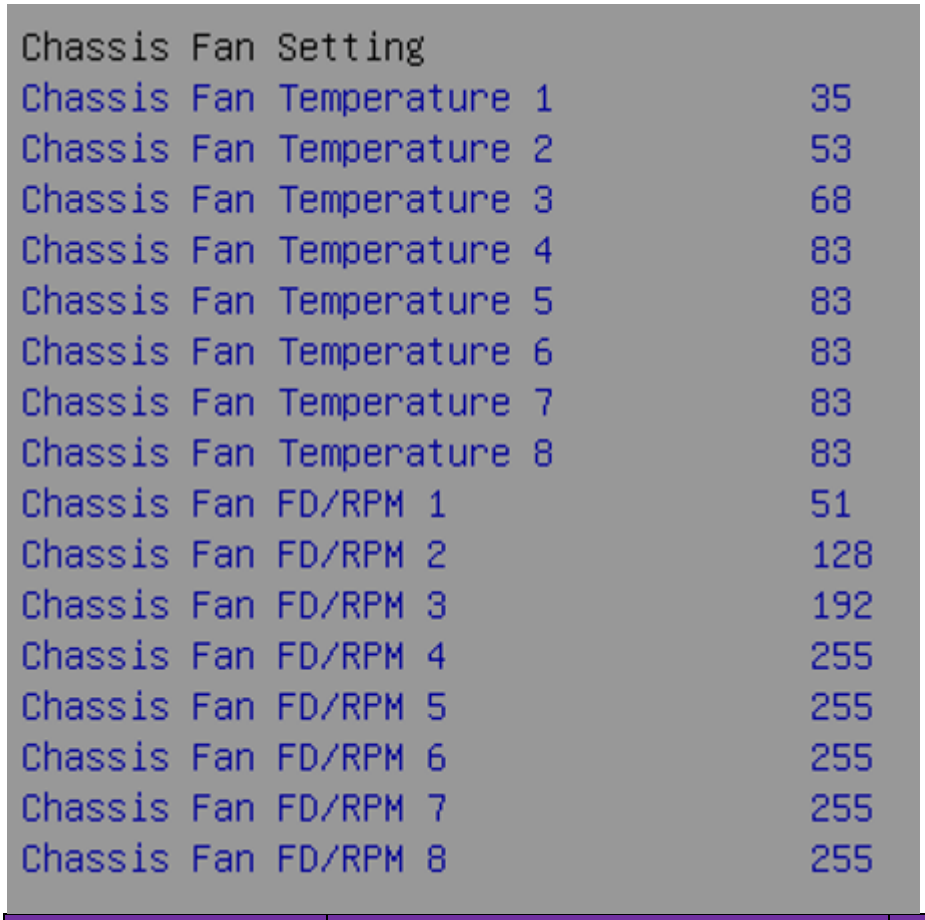
6.4 Hardware Monitor



Feature	Description	Options
Smart Fan Mode	Full Speed: Fans Run at 100% Speed Standard: Recommended Setting Manual: User-Defined Fan Speed Silent: Noise-Optimized Setting Performance: Performance-Optimized Setting	★Standard, Full Speed, Manual, Silent, Performance
Smart Fan Mode [Manual]		
Smart Fan Function	Smart Fan Function Setting	

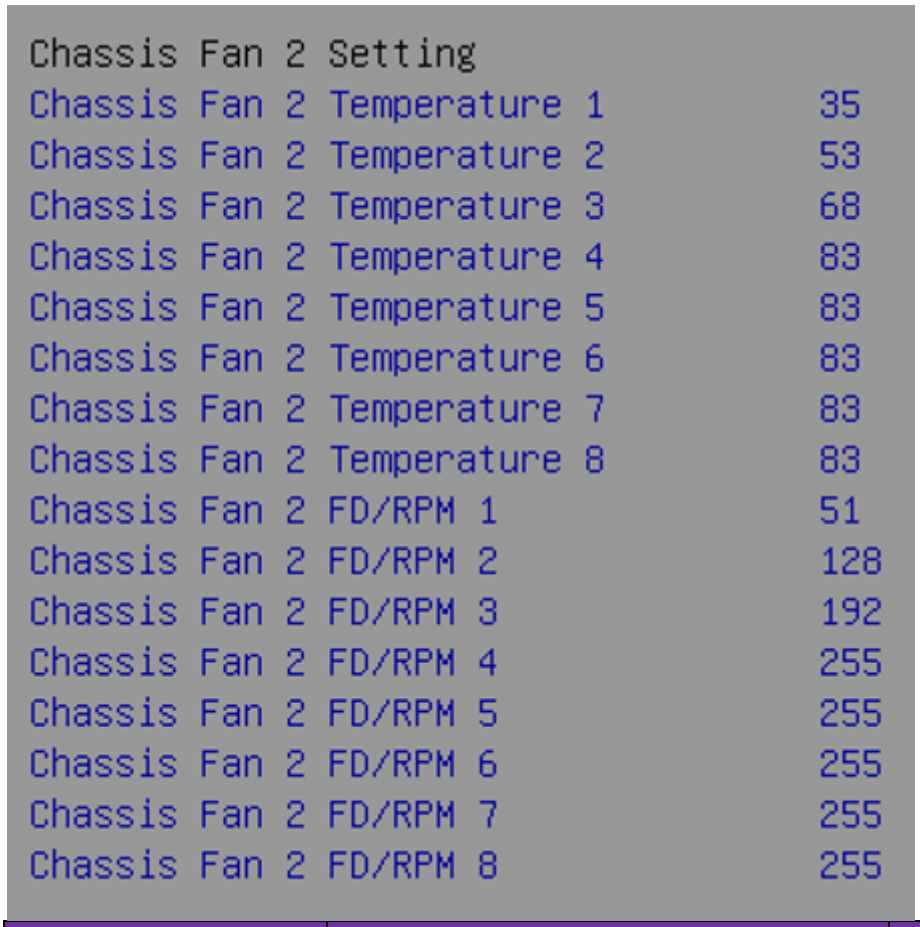
Smart Fan Function

Chassis Fan Setting



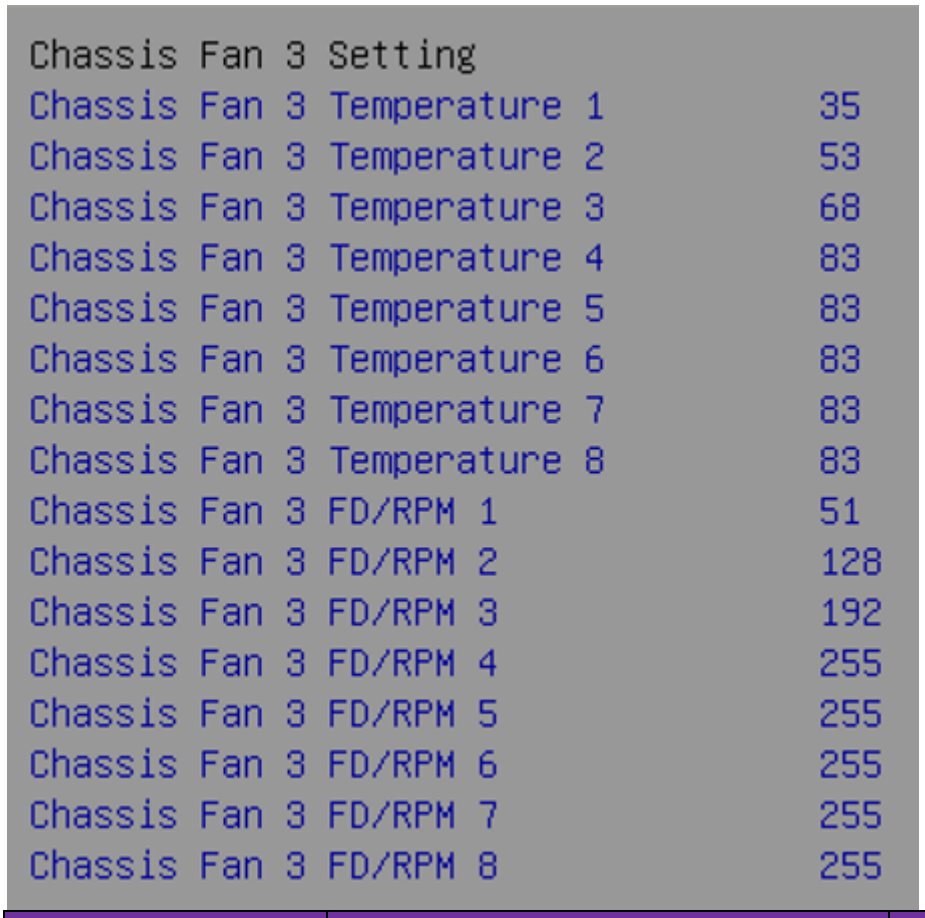
Feature	Description	Options
Chassis Fan Temperature 1~8	Allow you to set the value of temperature	
Chassis Fan FD/RPM 1~8	The value of Fan Duty/RPM when temperature is T1~T8 Range: 0~255	

Chassis Fan 2 Setting



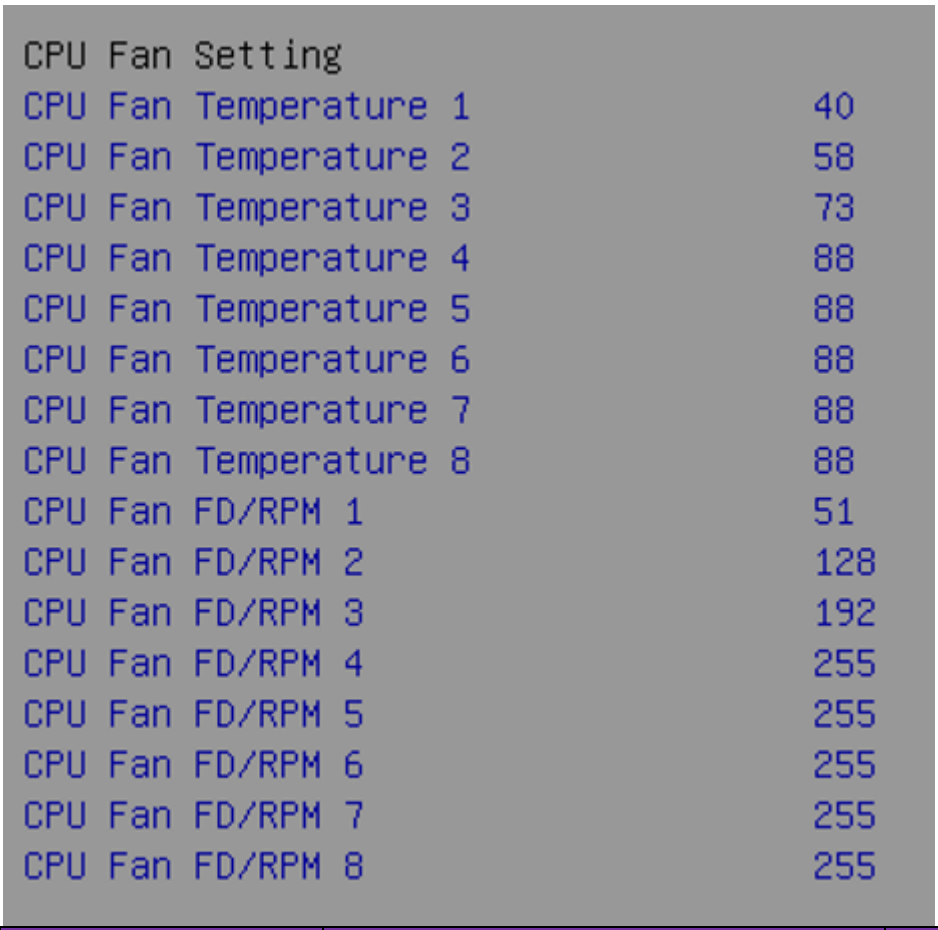
Feature	Description	Options
Chassis Fan 2 Temperature 1~8	Allow you to set the value of temperature	
Chassis Fan 2 FD/RPM 1~8	The value of Fan Duty/RPM when temperature is T1~T8 Range: 0~255	

Chassis Fan 3 Setting



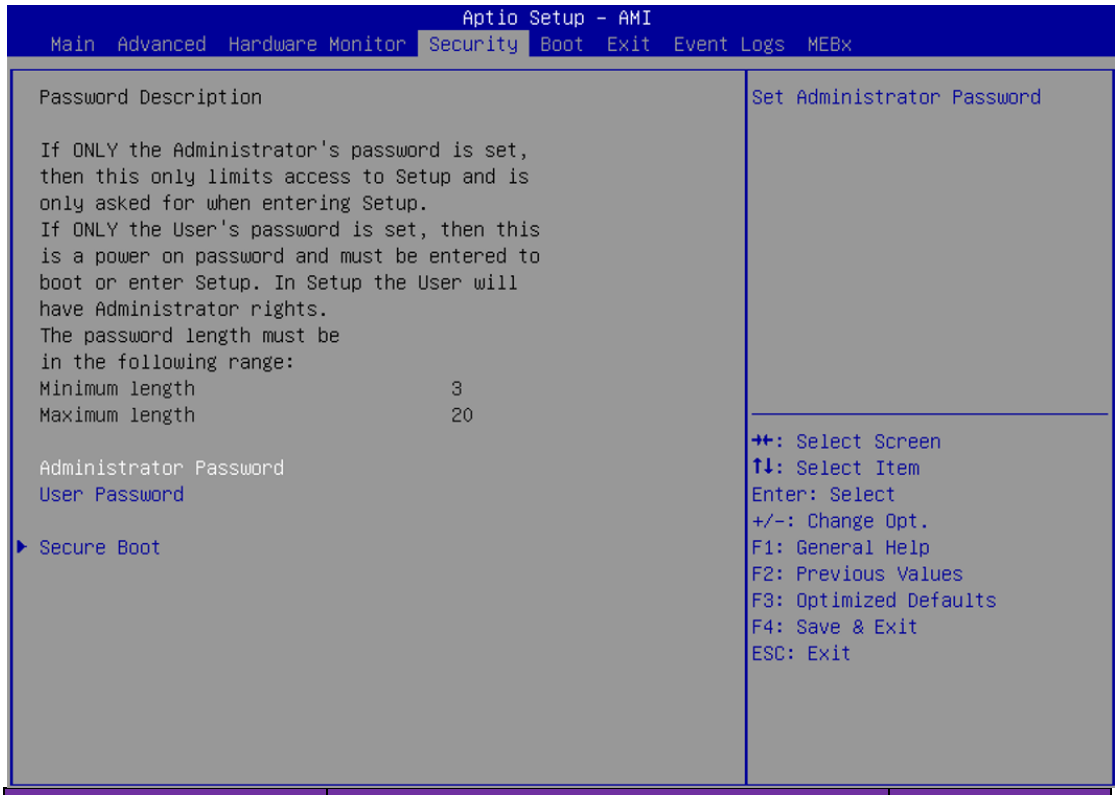
Feature	Description	Options
Chassis Fan 3 Temperature 1~8	Allow you to set the value of temperature	
Chassis Fan 3 FD/RPM 1~8	The value of Fan Duty/RPM when temperature is T1~T8 Range: 0~255	

CPU Fan Setting



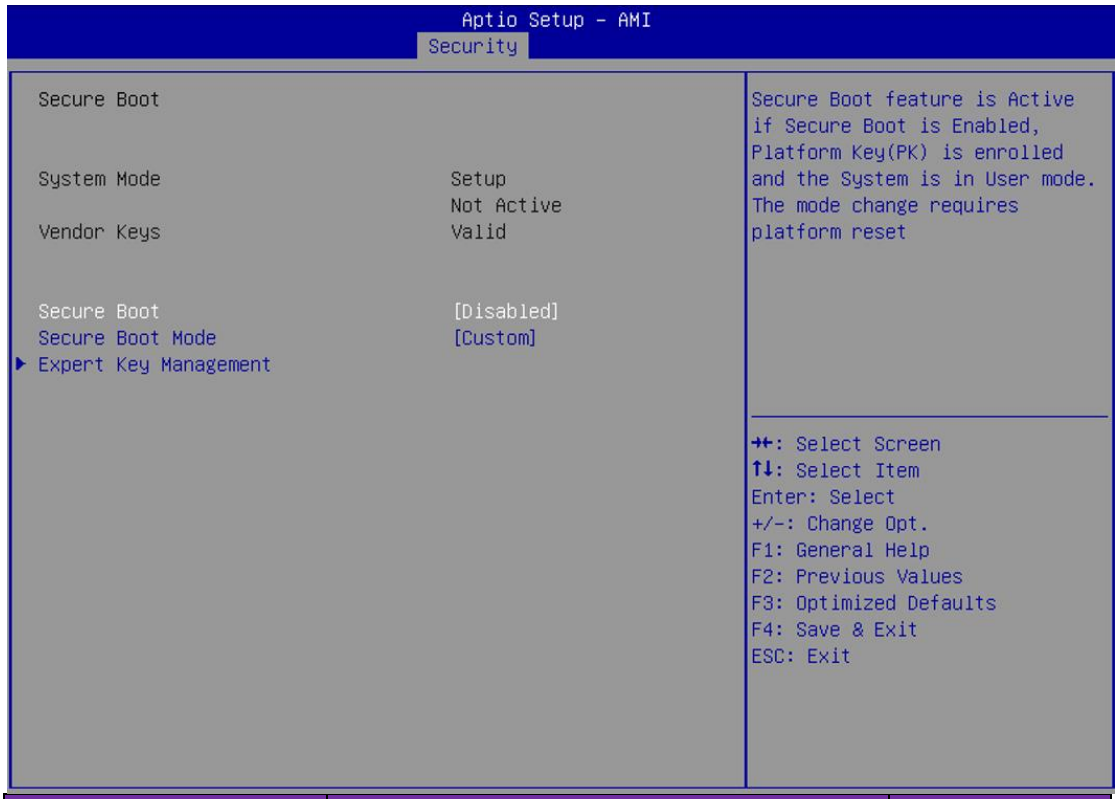
Feature	Description	Options
CPU Fan Temperature 1~8	Allow you to set the value of temperature	
CPU Fan FD/RPM 1~8	The value of Fan Duty/RPM when temperature is T1~T8 Range: 0~255	

6.5 Security



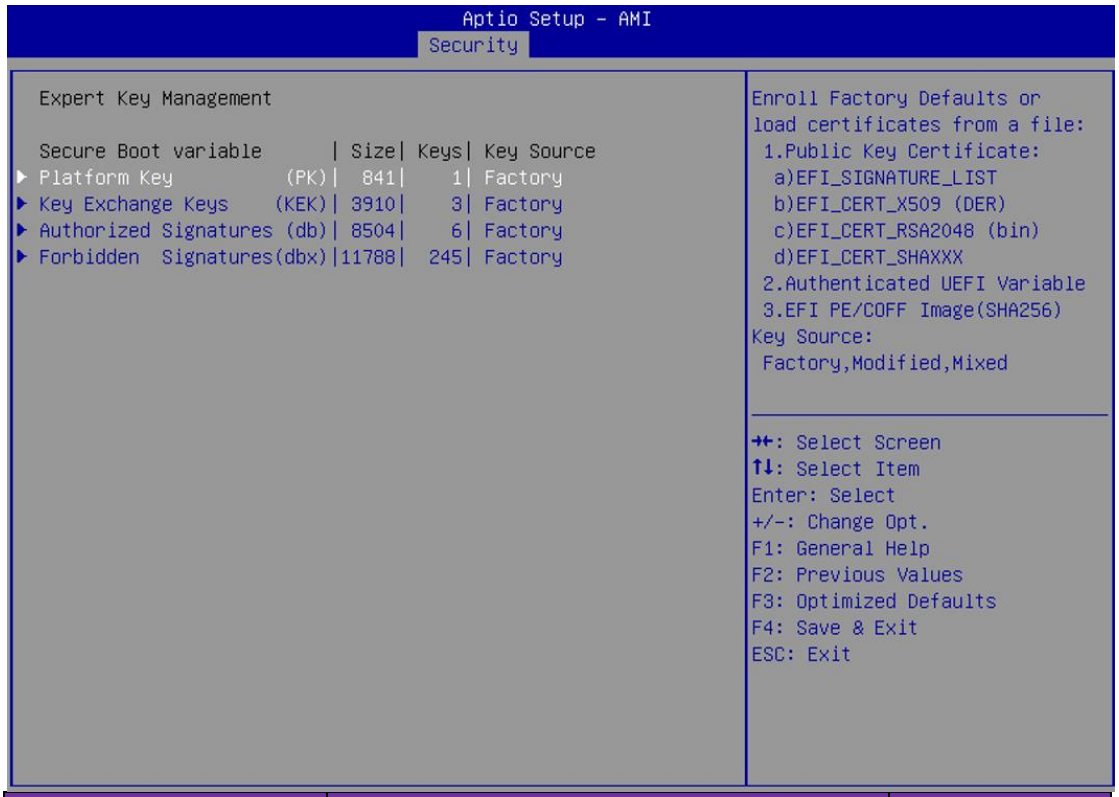
Feature	Description	Options
Administrator Password	Set Administrator password	
User Password	Set User Password	
Secure Boot	Secure Boot configuration	

Secure Boot



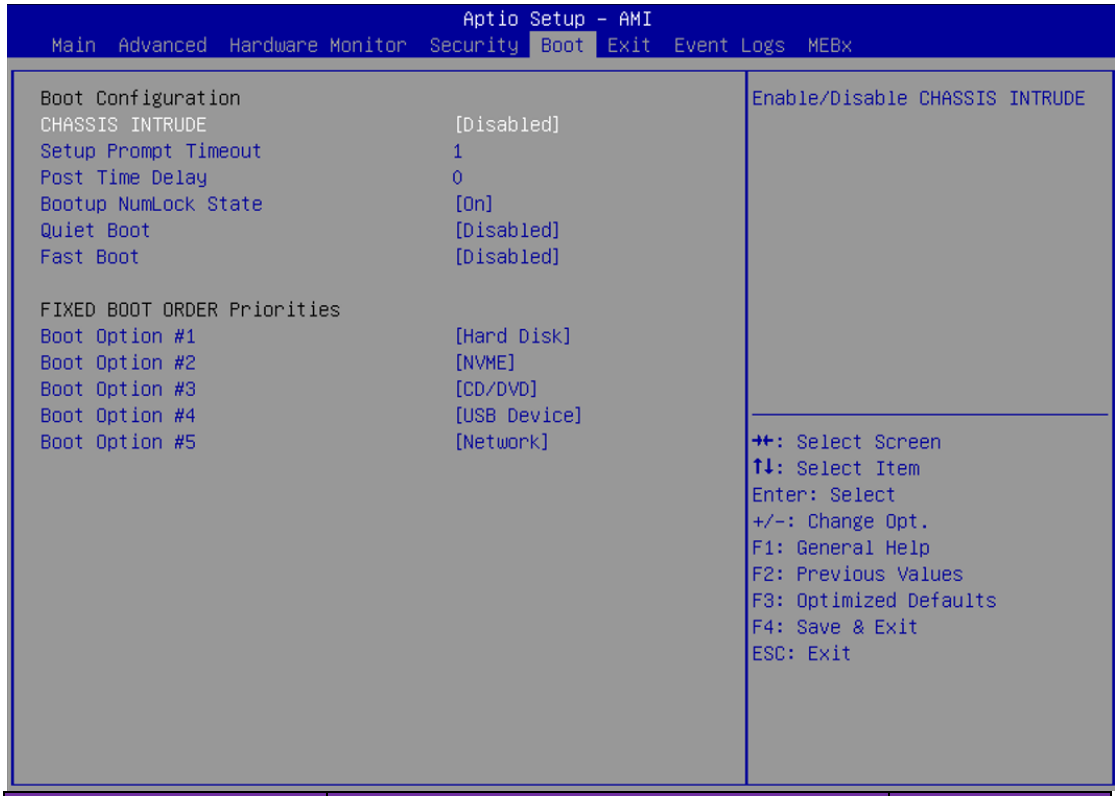
Feature	Description	Options
Secure Boot	Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset	★Disabled, Enabled
Secure Boot Mode	Secure Boot Mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication	Standard, ★Custom
Expert Key Management	Enables expert users to modify Secure Boot Policy variables without variable authentication	

Expert Key Management



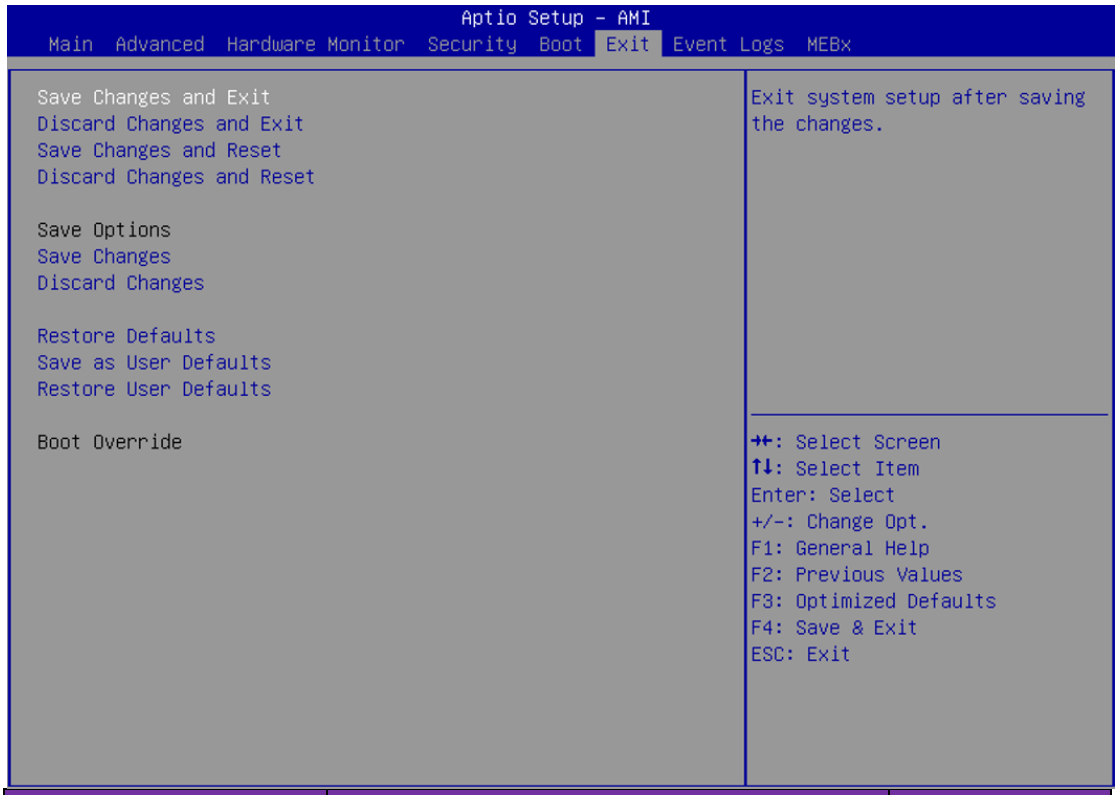
Feature	Description	Options
Platform Key(PK)	Enroll Factory Defaults or load certificates from a file: 1.Publuc Key Certificate: a)EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, Modified, Mixed	Details, Export, Update, Delete
Key Exchange Keys(KEK)		Details, Export, Update, Append, Delete
Authorized Signatures(db)		Details, Export, Update, Append, Delete
Forbidden Signatures(dbx)		Details, Export, Update, Append, Delete

6.6 Boot



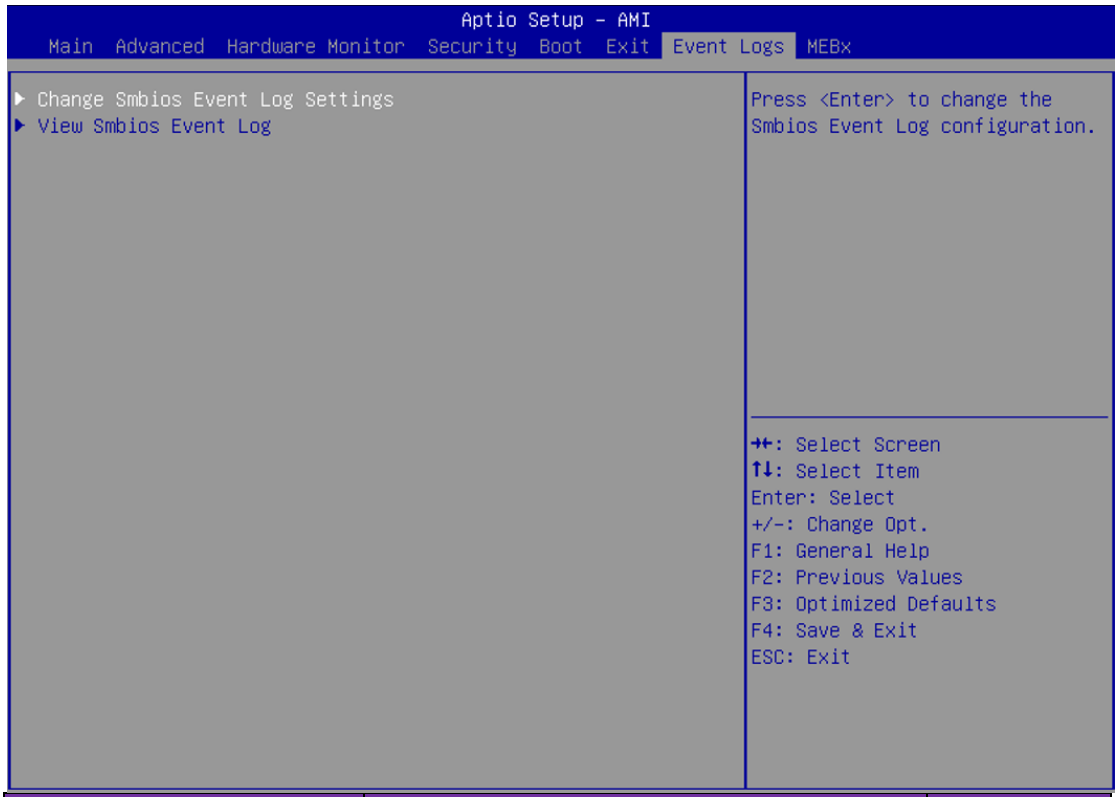
Feature	Description	Options
CHASSIS INTRUDE	Enable/Disable CHASSIS INTRUDE	★Disabled, Enabled
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★1
Post Time Delay	Delay for specific situation needs. For example, HDD spin up time (Delay time = value * 500ms)	★0
Bootup NumLock State	Select the keyboard NumLock state	★On, Off
Quiet Boot	Enables or disables Quiet Boot option	★Disabled, Enabled
Fast Boot	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.	★Disabled, Enabled
Boot Option #1 ~ #5	Sets the system boot order	★Hard Disk, NVME, CD/DVD, USB Device, Network, Disabled

6.7 Exit



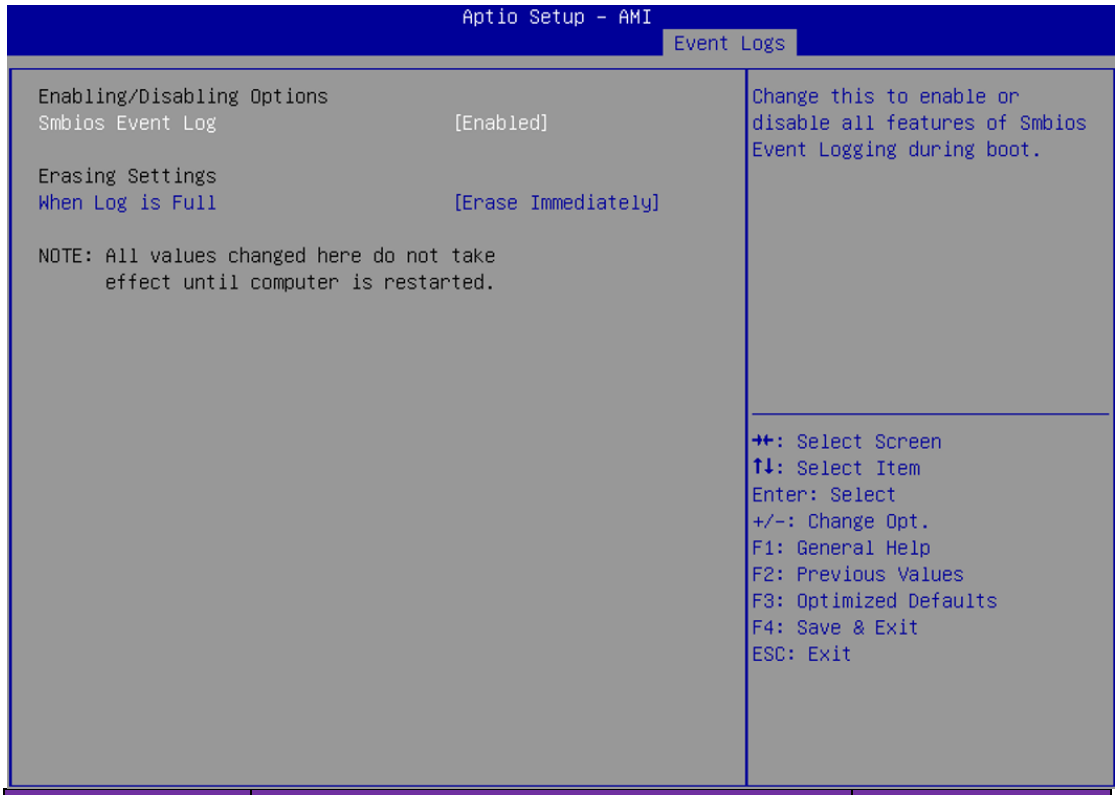
Feature	Description	Options
Save Changes and Exit	Exit system setup after saving the changes.	
Discard Changes and Exit	Exit system setup without saving any changes.	
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Rest system setup without saving any changes.	
Save Changes	Save Changes done so far to any of the setup options.	
Discard Changes	Discard Changes done so far to any of the setup options.	
Restore Defaults	Restore/Load Default values for all the setup options.	
Save as User Defaults	Save the changes done so far as User Defaults.	
Restore User Defaults	Restore the User Defaults to all the setup options.	

6.8 Event Logs



Feature	Description	Options
Change Smbios Event Log Settings	Press <Enter> to change the Smbios Event Log configuration.	
View Smbios Event Log	Press <Enter> to view the Smbios Event Log records.	

Change Smbios Event Log Settings



Feature	Description	Options
Smbios Event Log	Change this to enable or disable all features of Smbios Event Logging during boot.	★Enabled, Disabled
When Log is Full	Choose options for reactions to a full Smbios Event Log.	★Erase Immediately, Do Nothing

6.9 MEBx

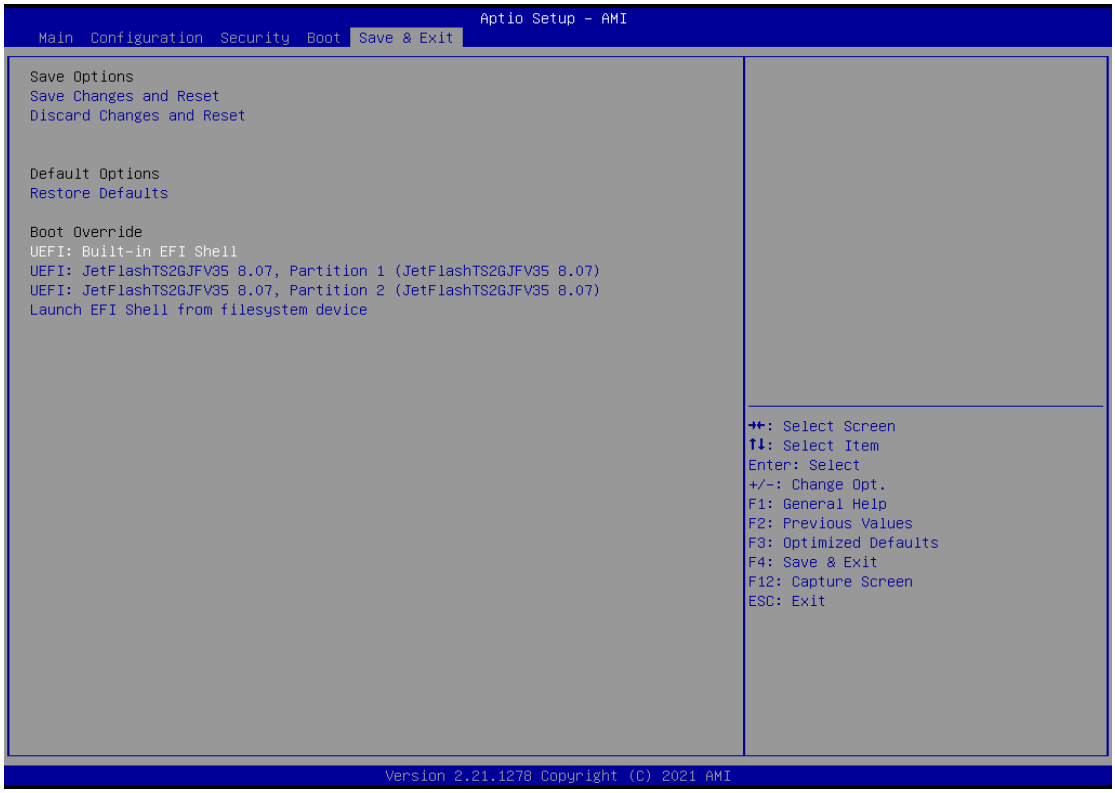

Aptio Setup – AMI
Main Advanced Hardware Monitor Security Boot Exit Event Logs MEBx
Intel(R) ME Password
MEBx Login
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

NANO-6064 **BIOS / EC UEFI Update SOP process under UEFI Shell**

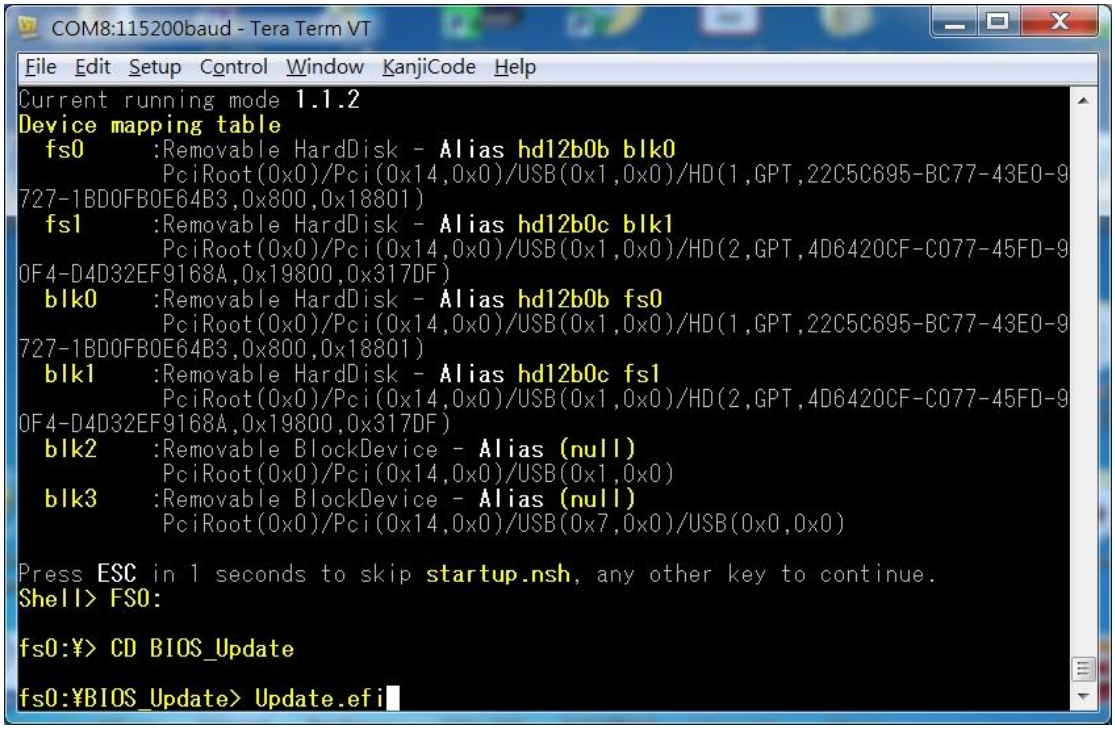
Step 1. Prepare a USB DOK.

Step 2. Unzip BIOS update file to the USB DOK.

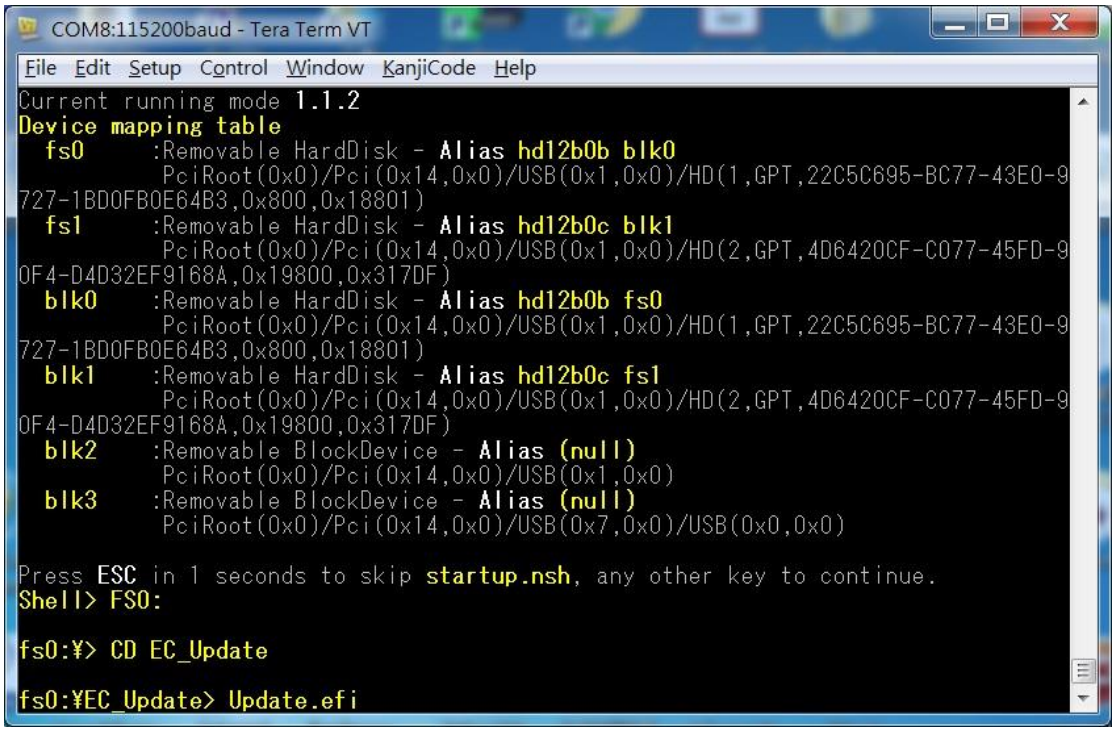
Step 3. Plug the USB DOK into the target system and then boot in UEFI Shell by selecting UEFI: Built-in EFI Shell in the BIOS Save & Exit page.



Step 4. Under the UEFI shell, direct to your USB DOK, below picture is an example using fs0. Then direct to the folder with BIOS / EC updated file and then enter command: "Update.efi" to start updating BIOS / EC.



(BIOS File Update)

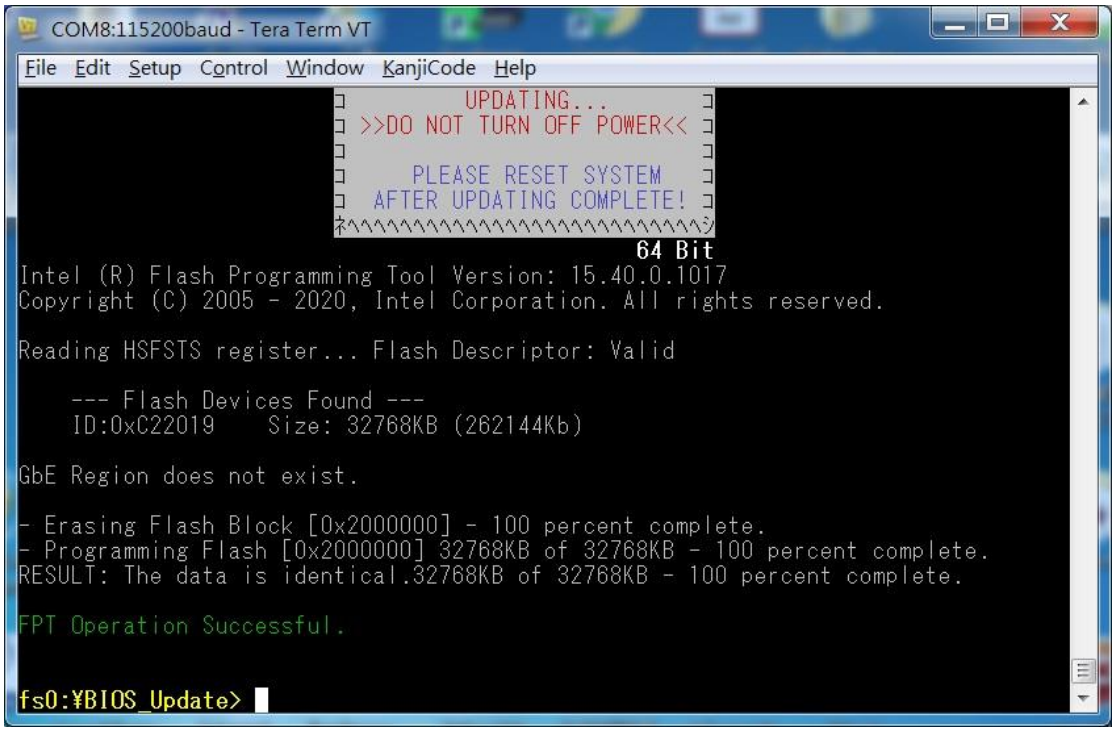


(EC File Update)

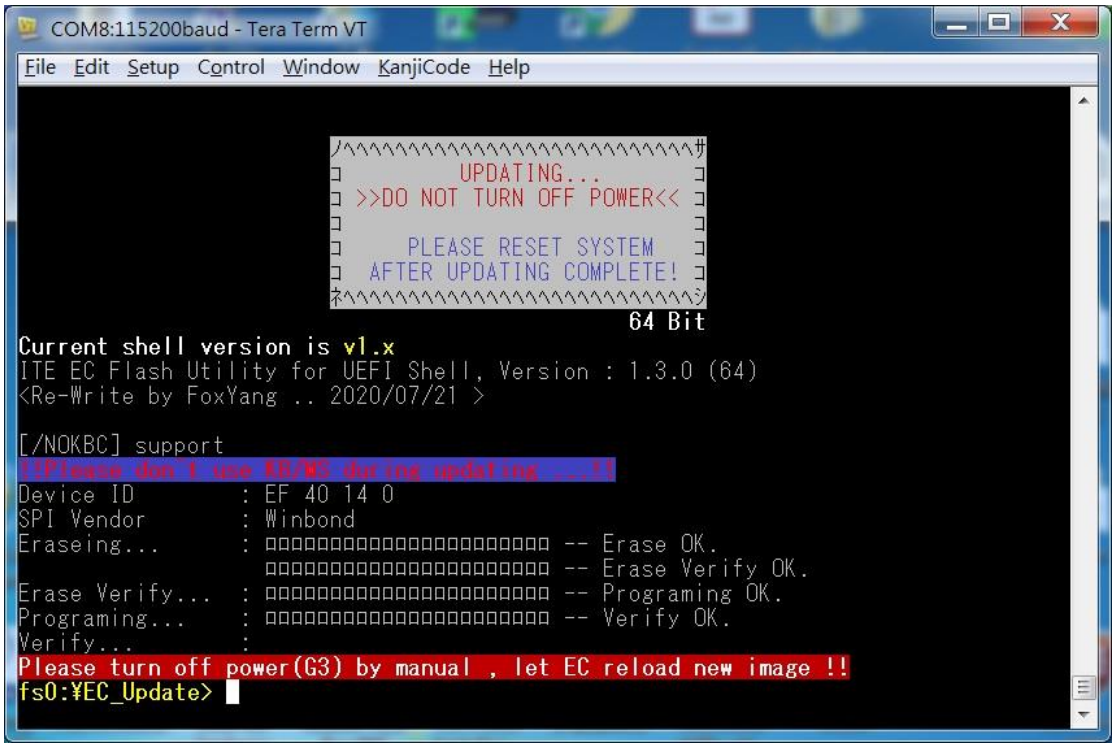
Step 5. The updating process will start and you can see the updating progress.

When you see the following pictures, which means the BIOS / EC update processes finished.

Please cut the AC power off and wait for 10 seconds before powering on.



(BIOS update finished)



(EC update finished)

Chapter 7

Overview

7 System Resources

7.1 Intel PCH

Intel® Q870 Chipset

7.2 Main Memory

RUBY-D814-Q870 provides 4 Dual Channel DDR5 U-DIMMs sockets which support the maximum memory can be up to 192GB. Memory clock and related settings can be detected by BIOS via SPD interface.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory modules into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

7.3 Installing the Single Board Computer

To install your RUBY-D814-Q870 into the standard chassis or proprietary environment, please perform the following:
Step 1: Check all jumpers setting on proper position
Step 2: Install and configure CPU, CPU cooler and memory module on right position
Step 3: Place RUBY-D814-Q870 into the dedicated position in the system
Step 4: Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that the motherboard is properly inserted and fixed by the mechanism.

Note:

Please find drivers in the RUBY-D814-Q870 of Portwell's download center. The driver supports Windows 10/11.

Chapter 8

Overview

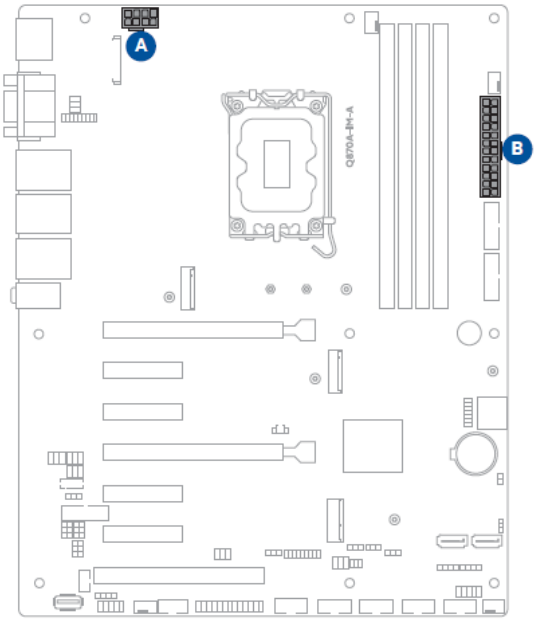
8 Troubleshooting

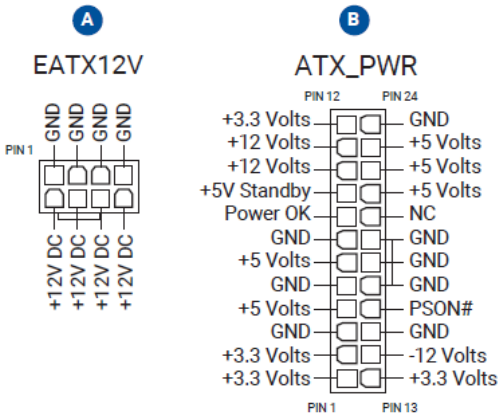
This chapter provides a few useful tips to quickly get RUBY-D814-Q870 running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

8.1 Hardware Quick Installation

ATX Power Setting

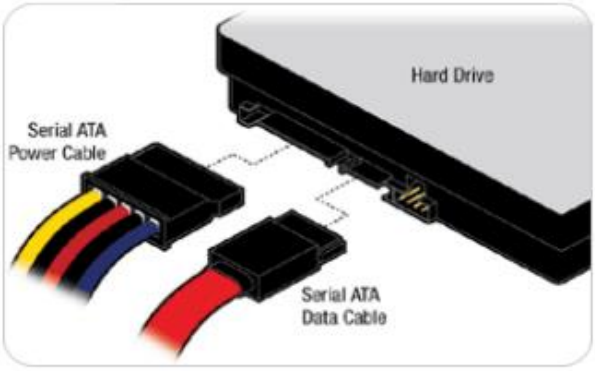
Correctly orient the ATX power supply plugs into these connectors and push down firmly until the connectors completely fit.





Serial ATA

Serial ATA Hard Disk Setting for SATA Speed Selection



System BIOS Main Menu

Configuration

SATA Configuration ..... [Press enter]

SATA Speed Selection [Auto, Gen1, Gen2, Gen3]

8.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power.

DDR5 UDIMM Memory, keyboard, mouse, SATA hard disk, VGA connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with RUBY-D814-Q870, it is recommended, when going with the boot-up sequence, to hit "DEL" and" ESC" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can

wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to "**RestoreDefaults**", press "**Enter**" and select "**Yes**" to load default optimal BIOS setup. This will force your BIOS setting back to the initial factory configurations. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting at any time when system appears to be unstable in boot up sequence.

8.3 FAQ

Information & Support

Question: I forgot my password for system BIOS, what am I supposed to do?

Answer: You can switch off your power supply then find the RTC battery on the RUBY-D814-Q870. Then remove the RTC battery and wait 5 seconds to clean your password then to switch on your power supply.

Question: How to update the BIOS file of RUBY-D814-Q870?

Answer:

1. Please visit web site of Portwell download center as below hyperlink https://download.portwell.tw/
2. Select “Search download” and type the keyword “RUBY-D814-Q870”.
3. Find the “BIOS “page and download the ROM file and flash utility.
4. Unzip file to bootable USB flash drive which can boot to shell mode. Then execute the “update.efi”. It will start to update BIOS.
5. When you see the “FPT Operation Passed” message, which means the BIOS update processes finished. Please cut the AC power off and wait for 10 seconds before powering on.
6. If you have other additional technical information or requests which are not covered in this manual, please fill in the technical request form as below hyperlink.

https://www.portwell.com.tw/support-center/technical-request/

We will do our best to provide a suggestion or solution for you.

Chapter 9

Overview

9 Portwell Software Service

9 Portwell Software Service

Portwell Evaluation Tool (PET)

The Portwell Evaluation Tool (PET) is an API which Portwell's customers can access the GPIO, I2C, SMBus, etc under Windows and Linux OS. For more information, please contact Portwell.

Portwell

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