COM Express Carrier Design Guide

Carrier design guideline for PCOM-B705GT

Rev. R0.2

Revision history

Rev.	Date	Note
R0.1	AUG.2023	Preliminary
R0.2	DEC.2023	•Update a note for “Table 6 Carrier Available Traces – PEG(Gen4)”.

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1 Introduction

The Carrier Design Guide provides the guideline of designing your own carrier board based on Portwell's COM Express Modular product PCOM-B705GT. PCOM-B705GT is Type 7, 95 × 125mm Module board, more information is included in PCOM-B705GT User's Guide and can be downloaded from Portwell download center (Or contacts your Portwell sales representative for acquiring PCOM-B705GT User's Guide). This carrier design guide is dedicated for the designers designing a COM Express Type 7 carrier board which will have an excellent compatibility with Portwell's PCOM-B705GT module product.

The layout guideline provided are 18 PCB layer stack up, each interface has three sections, which are detail PCOM-B705GT pin out, pin name, power rail, PU/PD, AC couple capacitor and etc. information are included. Second part containing PCB layout guide, impedance, and maximum trace, trace width, and trace spacing etc. Third section provides the available trace length of which designers able to optimize the high-speed signals such as PCIE, SATA, USB etc.

1.1 Comparison of Type 6 and Type 7 (COM Express R3.0)

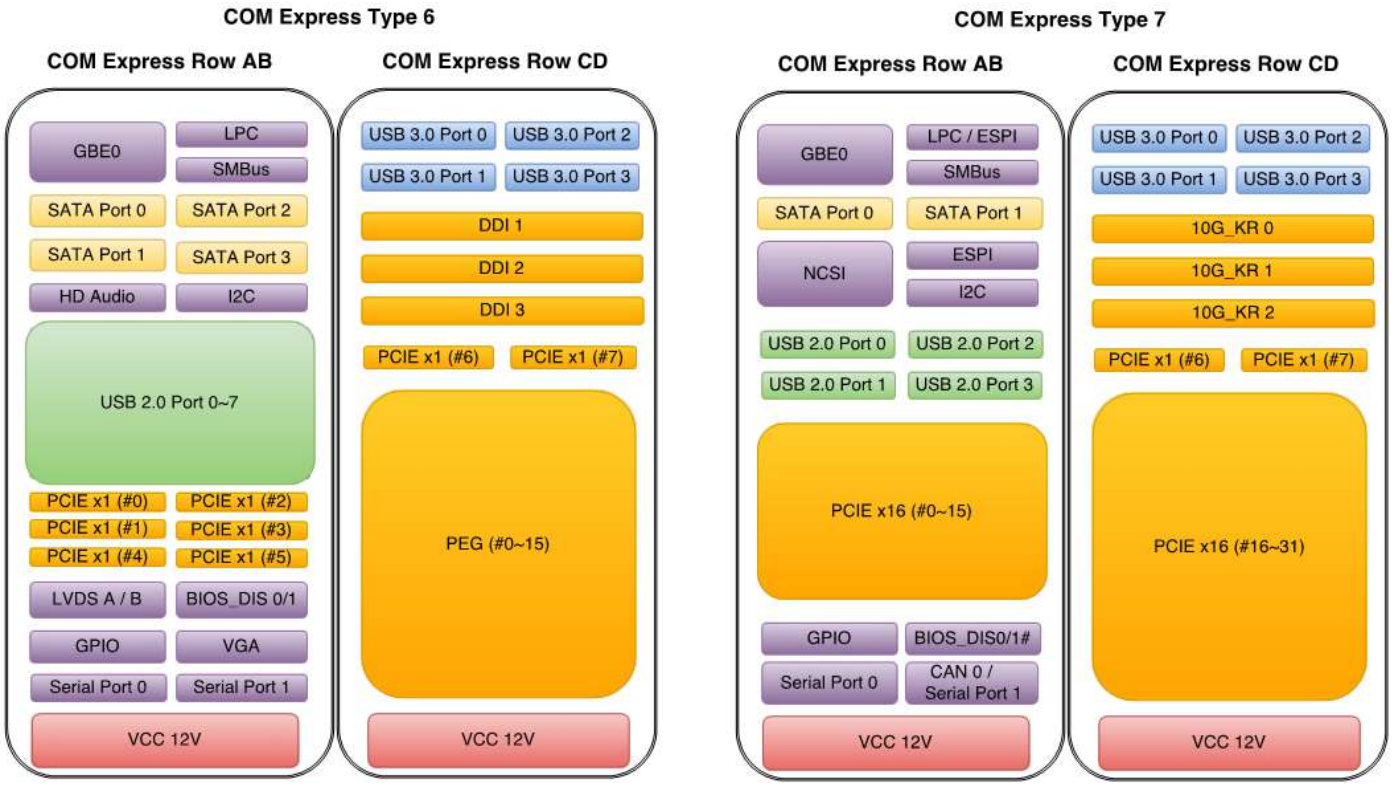

Figure 1 COM Express Type 6 and Type 7 Comparison

2 PCOM-B705GT

2.1 Block Diagram

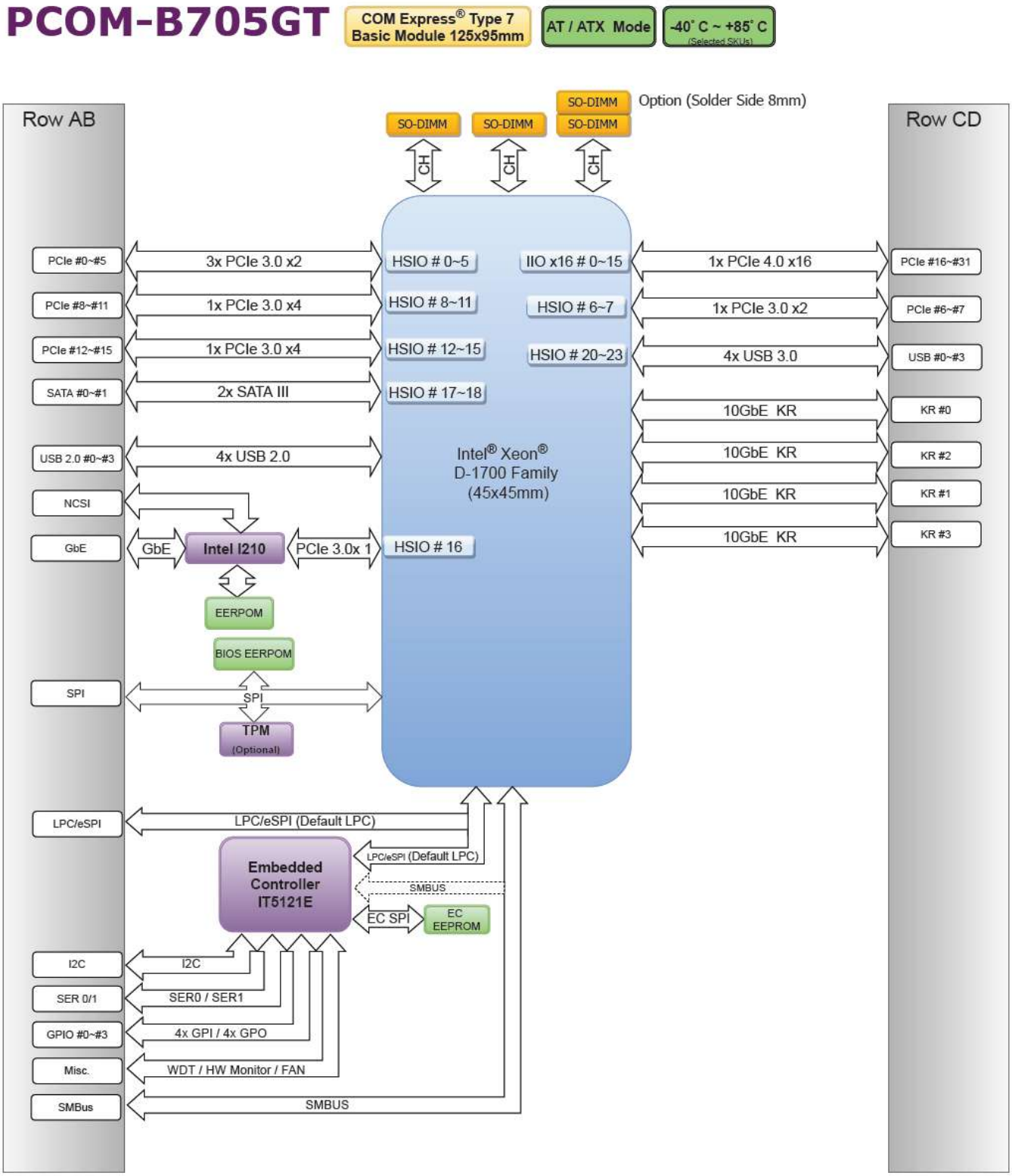

Figure 2 PCOM-B705GT Block Diagram

3 COM Express Interface

3.1 PCIe

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A22	PCIE_HSIO15_TXP15	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A23	PCIE_HSIO15_TXN15	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A25	PCIE_HSIO14_TXP14	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A26	PCIE_HSIO14_TXN14	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A36	PCIE_HSIO13_TXP13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A37	PCIE_HSIO13_TXN13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A39	PCIE_HSIO12_TXP12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A40	PCIE_HSIO12_TXN12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A52	PCIE_HSIO5_TXP5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A53	PCIE_HSIO5_TXN5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A55	PCIE_HSIO4_TXP4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A56	PCIE_HSIO4_TXN4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A58	PCIE_HSIO3_TXP3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A59	PCIE_HSIO3_TXN3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A61	PCIE_HSIO2_TXP2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

A62	PCIE_HSIO2_TXN2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A64	PCIE_HSIO1_TXP1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A65	PCIE_HSIO1_TXN1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A68	PCIE_HSIO0_TXP0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A69	PCIE_HSIO0_TXN0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A71	PCIE_HSIO8_TXP8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A72	PCIE_HSIO8_TXN8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A74	PCIE_HSIO9_TXP9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A75	PCIE_HSIO9_TXN9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A77	PCIE_HSIO10_TXP10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A78	PCIE_HSIO10_TXN10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A81	PCIE_HSIO11_TXP11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A82	PCIE_HSIO11_TXN11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
A88	COMe_PCIe_GEN3_CLKP	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE		
A89	COMe_PCIe_GEN3_CLKN	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE		
B22	PCIE_HSIO15_RXP15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		

B23	PCIE_HSIO15_RXN15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B25	PCIE_HSIO14_RXP14	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B26	PCIE_HSIO14_RXN14	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B29	COME_PCIe_GEN4_CLKP	Second reference clock output for higher speed PCI Express implementation on Lanes 16 to 31, for Type 7 implementations only,	O	PCIE	PCIE		
B30	COME_PCIe_GEN4_CLKN	Second reference clock output for higher speed PCI Express implementation on Lanes 16 to 31, for Type 7 implementations only,	O	PCIE	PCIE		
B36	PCIE_HSIO12_RXP12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B37	PCIE_HSIO12_RXN12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B39	PCIE_HSIO13_RXP13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B40	PCIE_HSIO13_RXN13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B52	PCIE_HSIO5_RXP5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B53	PCIE_HSIO5_RXN5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B55	PCIE_HSIO4_RXP4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B56	PCIE_HSIO4_RXN4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B58	PCIE_HSIO3_RXP3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B59	PCIE_HSIO3_RXN3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B61	PCIE_HSIO2_RXP2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B62	PCIE_HSIO2_RXN2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

B64	PCIE_HSIO1_RXP1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B65	PCIE_HSIO1_RXN1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B68	PCIE_HSIO0_RXP0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B69	PCIE_HSIO0_RXN0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B71	PCIE_HSIO8_RXP8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B72	PCIE_HSIO8_RXN8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B74	PCIE_HSIO9_RXP9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B75	PCIE_HSIO9_RXN9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B77	PCIE_HSIO10_RXP10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B78	PCIE_HSIO10_RXN10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B81	PCIE_HSIO11_RXP11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
B82	PCIE_HSIO11_RXN11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C19	PCIE_HSIO6_RXP6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
C20	PCIE_HSIO6_RXN6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
C22	PCIE_HSIO7_RXP7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
C23	PCIE_HSIO7_RXN7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
C52	COME_SoC_PCIE4_RXDP0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C53	COME_SoC_PCIE4_RXDN0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C55	COME_SoC_PCIE4_RXDP1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C56	COME_SoC_PCIE4_RXDN1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C58	COME_SoC_PCIE4_RXDP2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C59	COME_SoC_PCIE4_RXDN2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C61	COME_SoC_PCIE4_RXDP3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C62	COME_SoC_PCIE4_RXDN3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C65	COME_SoC_PCIE4_RXDP4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C66	COME_SoC_PCIE4_RXDN4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C68	COME_SoC_PCIE4_RXDP5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C69	COME_SoC_PCIE4_RXDN5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C71	COME_SoC_PCIE4_RXDP6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C72	COME_SoC_PCIE4_RXDN6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C74	COME_SoC_PCIE4_RXDP7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C75	COME_SoC_PCIE4_RXDN7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C78	COME_SoC_PCIE4_RXDP8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C79	COME_SoC_PCIE4_RXDN8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C81	COME_SoC_PCIE4_RXDP9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C82	COME_SoC_PCIE4_RXDN9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C85	COME_SoC_PCIE4_RXDP10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C86	COME_SoC_PCIE4_RXDN10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C88	COME_SoC_PCIE4_RXDP11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C89	COME_SoC_PCIE4_RXDN11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		

C91	COME_SoC_PCIE4_RXDP12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C92	COME_SoC_PCIE4_RXDN12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C94	COME_SoC_PCIE4_RXDP13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C95	COME_SoC_PCIE4_RXDN13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C98	COME_SoC_PCIE4_RXDP14	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C99	COME_SoC_PCIE4_RXDN14	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C101	COME_SoC_PCIE4_RXDP15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
C102	COME_SoC_PCIE4_RXDN15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module		
D20	PCIE_HSIO6_TXP6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D21	PCIE_HSIO6_TXN6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D22	PCIE_HSIO7_TXP7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D23	PCIE_HSIO7_TXN7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D52	SoC_COME_PCIE4_TXDP0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D53	SoC_COME_PCIE4_TXDN0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D55	SoC_COME_PCIE4_TXDP1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D56	SoC_COME_PCIE4_TXDN1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D58	SoC_COME_PCIE4_TXDP2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D59	SoC_COME_PCIE4_TXDN2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D61	SoC_COME_PCIE4_TXDP3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D62	SoC_COME_PCIE4_TXDN3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

D65	SoC_COME_PCIE4_TXDP4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D66	SoC_COME_PCIE4_TXDN4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D68	SoC_COME_PCIE4_TXDP5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D69	SoC_COME_PCIE4_TXDN5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D71	SoC_COME_PCIE4_TXDP6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D72	SoC_COME_PCIE4_TXDN6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D74	SoC_COME_PCIE4_TXDP7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D75	SoC_COME_PCIE4_TXDN7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D78	SoC_COME_PCIE4_TXDP8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D79	SoC_COME_PCIE4_TXDN8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D81	SoC_COME_PCIE4_TXDP9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D82	SoC_COME_PCIE4_TXDN9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D85	SoC_COME_PCIE4_TXDP10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D86	SoC_COME_PCIE4_TXDN10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D88	SoC_COME_PCIE4_TXDP11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D89	SoC_COME_PCIE4_TXDN11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D91	SoC_COME_PCIE4_TXDP12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D92	SoC_COME_PCIE4_TXDN12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D94	SoC_COME_PCIE4_TXDP13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D95	SoC_COME_PCIE4_TXDN13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		

D98	SoC_COME_PCIE4_TXDP14	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D99	SoC_COME_PCIE4_TXDN14	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D101	SoC_COME_PCIE4_TXDP15	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		
D102	SoC_COME_PCIE4_TXDN15	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module		

Table 1 PCIE Pin Out

3.1.1 AC Coupling Capacitor

PCIE / PEG AC Coupling: Device Down

While PCIE devices are designed on COM Express Carrier Board, the AC coupling Capacitor should be added on the carrier, please refer to below diagram.

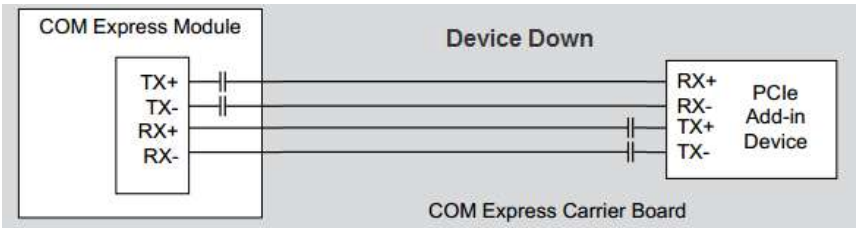

Figure 3 PCIE AC Coupling Capacitor - Device Down
(From PICMG COM Express Carrier Board Design Guide)

PCIE / PEG AC Coupling: Add-In Card

While PCIE devices are designed as Add In Card, the AC coupling Capacitor should be on PCIe Add-In Card, rather than on the COM Express Carrier Board, please refer to below diagram.

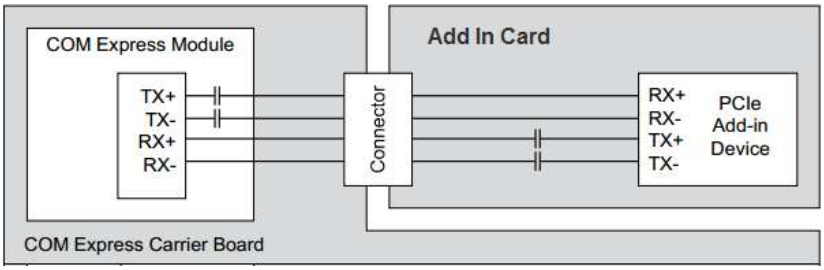

Figure 4 PCIE AC Coupling Capacitor - Add In Card
(From PICMG COM Express Carrier Board Design Guide)

3.1.2 PCB Layout Guideline - PCIE

Parameter	PCIe Gen2	PCIe Gen3	PCIe Gen 4
Symbol Rate / PCIe Lane	5.0 G Symbols/s	8.0 G Symbols/s	16 G Symbols/s
Nyquist Rate (used for loss calculations)	2.5 GHz	4 GHz	8 GHz
Module PCIe Trace Length Allowance	5.0 inches	4.0 inches	Std PCB 3.0 inches Mid Loss 4.7 inches Low Loss 6.1 inches
Carrier PCIe Trace Length Allowance Device Down	8.0 inches	10 inches	Std PCB 7.7 inches Mid Loss 12.3 inches Low Loss 15.9 inches
Carrier PCIe Trace Length Allowance Device Up	4.45 inches	4.0 inches	Std PCB 4.7 inches Mid Loss 7.5 inches Low Loss 9.8 inches
Differential Impedance (Per PCI-SIG and COMe CDG Rev. 2.0)	85 Ω +/-15%	85 Ω +/-15%	85 Ω +/-15%
Single-ended Impedance	50 Ω +/-15%	50 Ω +/-15%	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent	PCB stack-up dependent	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent	PCB stack-up dependent	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils	Min. 20mils	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils	Min. 50mils	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils	Min. 20mils	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils	Max. 5mils	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	Max. 5mils	Max. 5mils	Max. 5mils
Length matching between reference clock pairs (inter-pair)	No electrical requirements.	No electrical requirements.	No electrical requirements.
Reference plane	GND	GND	GND
Spacing from edge of plane	Min. 40mils	Min. 40mils	Min. 40mils

Via Usage	Max. 2 vias per TX trace Max. 4 vias per RX trace	Max. 2 vias / TX Max. 4 vias / RX (to device) Max. 2 vias / RX (to slot)	Max. 2 vias / TX Max. 4 vias / RX (to device) Max. 2 vias / RX (to slot)
AC coupling capacitors The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board (for Device Down). For Device Up (on slot card, mini -PCIe or M.2) the COMe RX caps are on the add in card. For MXM card implementations, the COMe RX caps are on the Carrier.	X7R dielectric 100nF +/-10% 16V 0402 or 0201 pkg Do not use arrays	X7R dielectric 200nF +/-10% 16V 0402 or 0201 pkg Do not use arrays	X7R dielectric 200nF +/-10% 16V 0402 or 0201 pkg Do not use arrays

Table 2 Layout Guideline – PCIE/PEG

(Reference from COM Express Module Base Specification Rev. 3.1 RC1.0 - June 16, 2022)

3.1.3 Passive Devices

AC Cap value (Gen1/Gen2/Gen3/Gen4)	Intel® Xeon® D-1700 Processor Families (PDG) value [220nF]	PCOM-B705GT AC Cap value [220nF]

Table 3 PCIE/PEG AC Coupling Capacitor Value

3.1.4 Reference Schematic - PCIE

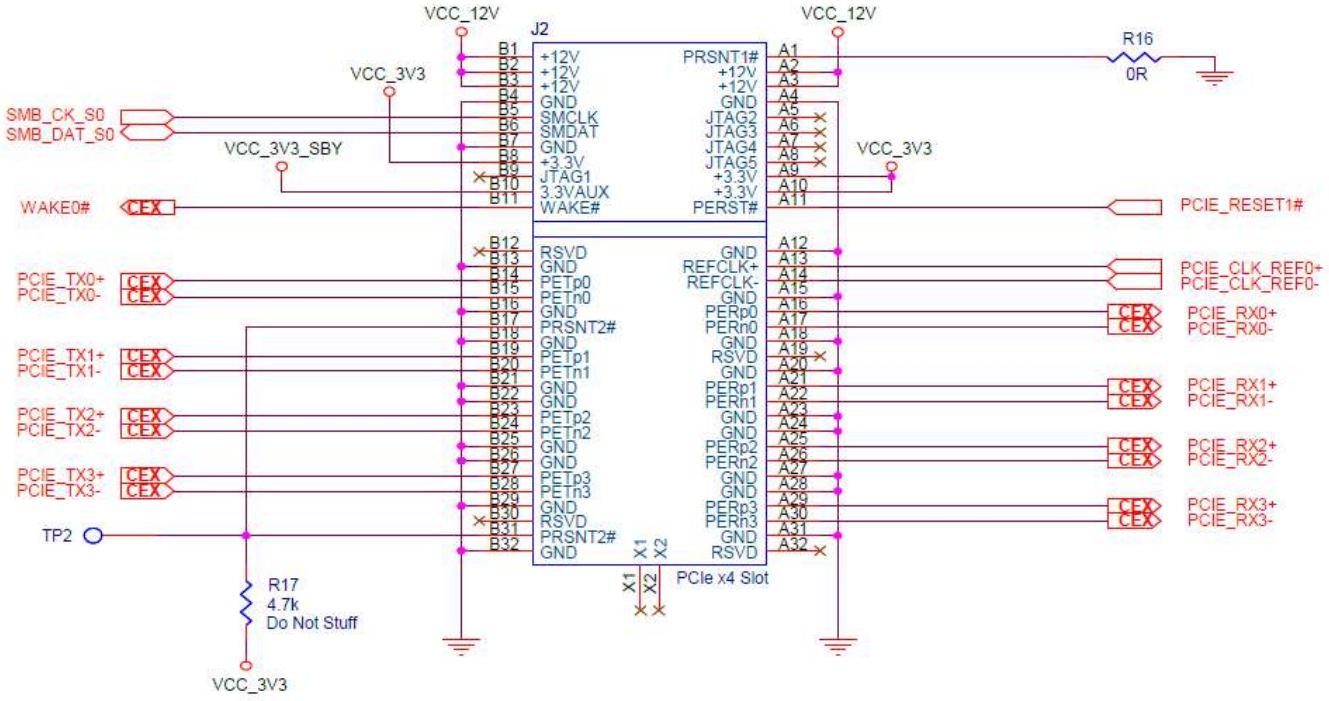

Figure 5 PCIE Reference Schematic

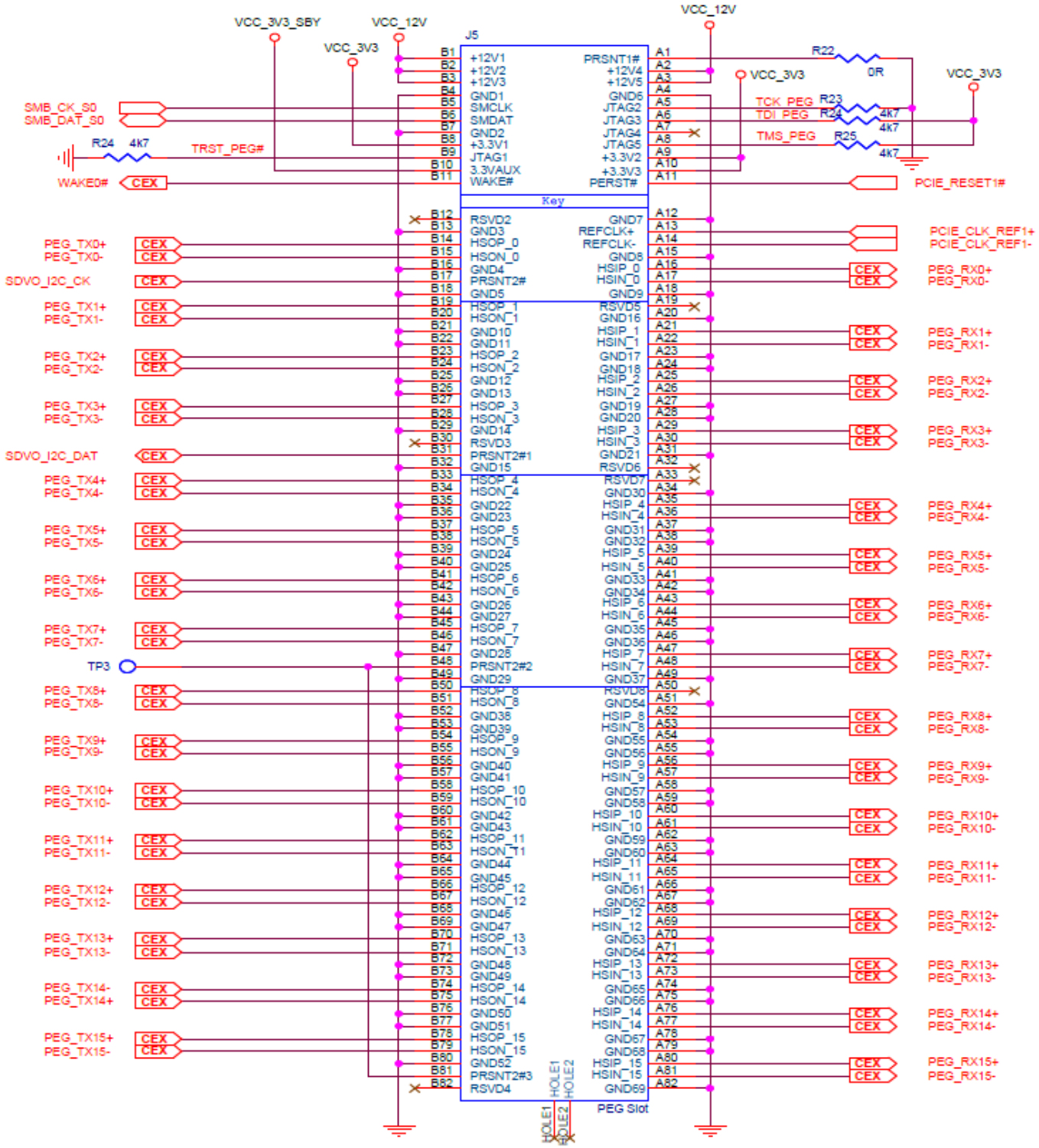

Figure 6 PEG Reference Schematic

3.1.5 Max Trace Length and Available Carrier Trace Length – PCIE (Gen 3) Add-In Card

That follow provide layout guidelines for mid-loss material.

Pin	Signal	Max Length	Module length	Available carrier length
A22	PCIE_HSIO15_TXP15	15000	3328.96	11671.04
A23	PCIE_HSIO15_TXN15	15000	3330.15	11669.85
A25	PCIE_HSIO14_TXP14	15000	3188.43	11811.57
A26	PCIE_HSIO14_TXN14	15000	3188.55	11811.45
A36	PCIE_HSIO13_TXP13	15000	3091.47	11908.53
A37	PCIE_HSIO13_TXN13	15000	3093.7	11906.3
A39	PCIE_HSIO12_TXP12	15000	3232.91	11767.09
A40	PCIE_HSIO12_TXN12	15000	3232.49	11767.51
A52	PCIE_HSIO5_TXP5	15000	2997.67	12002.33
A53	PCIE_HSIO5_TXN5	15000	2997.81	12002.19
A55	PCIE_HSIO4_TXP4	15000	2944.98	12055.02
A56	PCIE_HSIO4_TXN4	15000	2947.01	12052.99
A58	PCIE_HSIO3_TXP3	15000	2862.92	12137.08
A59	PCIE_HSIO3_TXN3	15000	2865.46	12134.54
A61	PCIE_HSIO2_TXP2	15000	2810.57	12189.43
A62	PCIE_HSIO2_TXN2	15000	2812.96	12187.04
A64	PCIE_HSIO1_TXP1	15000	2759.57	12240.43
A65	PCIE_HSIO1_TXN1	15000	2760.35	12239.65
A68	PCIE_HSIO0_TXP0	15000	2668.51	12331.49
A69	PCIE_HSIO0_TXN0	15000	2668.94	12331.06
A71	PCIE_HSIO8_TXP8	15000	2768.51	12231.49
A72	PCIE_HSIO8_TXN8	15000	2768.62	12231.38
A74	PCIE_HSIO9_TXP9	15000	3009.28	11990.72

A75	PCIE_HSIO9_TXN9	15000	3008.62	11991.38
A77	PCIE_HSIO10_TXP10	15000	3044.88	11955.12
A78	PCIE_HSIO10_TXN10	15000	3047.13	11952.87
A81	PCIE_HSIO11_TXP11	15000	3202.77	11797.23
A82	PCIE_HSIO11_TXN11	15000	3203.03	11796.97
A88	COMe_PCIe_GEN3_CLKP	16000	4306.38	11693.62
A89	COMe_PCIe_GEN3_CLKN	16000	4310.22	11689.78
B22	PCIE_HSIO15_RXP15	15000	1964.54	13035.46
B23	PCIE_HSIO15_RXN15	15000	1966.09	13033.91
B25	PCIE_HSIO14_RXP14	15000	2052.08	12947.92
B26	PCIE_HSIO14_RXN14	15000	2052.55	12947.45
B36	PCIE_HSIO12_RXP12	15000	2161.9	12838.1
B37	PCIE_HSIO12_RXN12	15000	2161.25	12838.75
B39	PCIE_HSIO13_RXP13	15000	2250.39	12749.61
B40	PCIE_HSIO13_RXN13	15000	2252.82	12747.18
B52	PCIE_HSIO5_RXP5	15000	1990.55	13009.45
B53	PCIE_HSIO5_RXN5	15000	1988.63	13011.37
B55	PCIE_HSIO4_RXP4	15000	1811.94	13188.06
B56	PCIE_HSIO4_RXN4	15000	1809.16	13190.84
B58	PCIE_HSIO3_RXP3	15000	1905.54	13094.46
B59	PCIE_HSIO3_RXN3	15000	1903.86	13096.14
B61	PCIE_HSIO2_RXP2	15000	1696.16	13303.84
B62	PCIE_HSIO2_RXN2	15000	1695.41	13304.59
B64	PCIE_HSIO1_RXP1	15000	1751.71	13248.29
B65	PCIE_HSIO1_RXN1	15000	1753.55	13246.45
B68	PCIE_HSIO0_RXP0	15000	1944.34	13055.66
B69	PCIE_HSIO0_RXN0	15000	1946.27	13053.73
B71	PCIE_HSIO8_RXP8	15000	2302.19	12697.81
B72	PCIE_HSIO8_RXN8	15000	2301.17	12698.83

B74	PCIE_HSIO9_RXP9	15000	2015	12985
B75	PCIE_HSIO9_RXN9	15000	2013.42	12986.58
B77	PCIE_HSIO10_RXP10	15000	2129.7	12870.3
B78	PCIE_HSIO10_RXN10	15000	2128.63	12871.37
B81	PCIE_HSIO11_RXP11	15000	2387.32	12612.68
B82	PCIE_HSIO11_RXN11	15000	2388.99	12611.01
C19	PCIE_HSIO6_RXP6	15000	1738.79	13261.21
C20	PCIE_HSIO6_RXN6	15000	1739.7	13260.3
C22	PCIE_HSIO7_RXP7	15000	1840.39	13159.61
C23	PCIE_HSIO7_RXN7	15000	1840.91	13159.09
D20	PCIE_HSIO6_TXP6	15000	1738.79	13261.21
D21	PCIE_HSIO6_TXN6	15000	1739.7	13260.3
D22	PCIE_HSIO7_TXP7	15000	1840.39	13159.61
D23	PCIE_HSIO7_TXN7	15000	1840.91	13159.09

Table 4 Carrier Available Traces – PCIE

3.1.6 Max Trace Length and Available Carrier Trace Length – PEG (Gen 3) Add-In Card

That follow provide layout guidelines for mid-loss material.

Pin	Signal	Max Length	Module length	Available carrier length
C52	COME_SoC_PCIE4_RXDP0	15000	1566.4	13433.59
C53	COME_SoC_PCIE4_RXDN0	15000	1568.1	13431.89
C55	COME_SoC_PCIE4_RXDP1	15000	1564.2	13435.79
C56	COME_SoC_PCIE4_RXDN1	15000	1565.5	13434.51
C58	COME_SoC_PCIE4_RXDP2	15000	1603.6	13396.4
C59	COME_SoC_PCIE4_RXDN2	15000	1601.1	13398.95

C61	COME_SoC_PCIE4_RXDP3	15000	1457.1	13542.91
C62	COME_SoC_PCIE4_RXDN3	15000	1458.7	13541.29
C65	COME_SoC_PCIE4_RXDP4	15000	1547.4	13452.61
C66	COME_SoC_PCIE4_RXDN4	15000	1544.7	13455.32
C68	COME_SoC_PCIE4_RXDP5	15000	1502.1	13497.88
C69	COME_SoC_PCIE4_RXDN5	15000	1503.9	13496.13
C71	COME_SoC_PCIE4_RXDP6	15000	1536.7	13463.27
C72	COME_SoC_PCIE4_RXDN6	15000	1534.7	13465.26
C74	COME_SoC_PCIE4_RXDP7	15000	1491.9	13508.1
C75	COME_SoC_PCIE4_RXDN7	15000	1493.5	13506.48
C78	COME_SoC_PCIE4_RXDP8	15000	1556.3	13443.73
C79	COME_SoC_PCIE4_RXDN8	15000	1556.6	13443.45
C81	COME_SoC_PCIE4_RXDP9	15000	1533.5	13466.48
C82	COME_SoC_PCIE4_RXDN9	15000	1535.7	13464.34
C85	COME_SoC_PCIE4_RXDP10	15000	1581.8	13418.16
C86	COME_SoC_PCIE4_RXDN10	15000	1579.6	13420.39
C88	COME_SoC_PCIE4_RXDP11	15000	1546.4	13453.61
C89	COME_SoC_PCIE4_RXDN11	15000	1548	13452.01
C91	COME_SoC_PCIE4_RXDP12	15000	1595.2	13404.76
C92	COME_SoC_PCIE4_RXDN12	15000	1593.3	13406.74
C94	COME_SoC_PCIE4_RXDP13	15000	1669.9	13330.14
C95	COME_SoC_PCIE4_RXDN13	15000	1671	13328.99
C98	COME_SoC_PCIE4_RXDP14	15000	1807	13193.01
C99	COME_SoC_PCIE4_RXDN14	15000	1806	13193.96

C101	COME_SoC_PCIE4_RXDP15	15000	1881.1	13118.87
C102	COME_SoC_PCIE4_RXDN15	15000	1881.9	13118.07
D52	SoC_COME_PCIE4_TXDP0	15000	1157.7	13842.29
D53	SoC_COME_PCIE4_TXDN0	15000	1155.7	13844.26
D55	SoC_COME_PCIE4_TXDP1	15000	1125.4	13874.56
D56	SoC_COME_PCIE4_TXDN1	15000	1126.5	13873.51
D58	SoC_COME_PCIE4_TXDP2	15000	1250.8	13749.17
D59	SoC_COME_PCIE4_TXDN2	15000	1251	13748.96
D61	SoC_COME_PCIE4_TXDP3	15000	1125.1	13874.95
D62	SoC_COME_PCIE4_TXDN3	15000	1125.3	13874.73
D65	SoC_COME_PCIE4_TXDP4	15000	1399.4	13600.56
D66	SoC_COME_PCIE4_TXDN4	15000	1398.7	13601.32
D68	SoC_COME_PCIE4_TXDP5	15000	1231.2	13768.84
D69	SoC_COME_PCIE4_TXDN5	15000	1231.8	13768.21
D71	SoC_COME_PCIE4_TXDP6	15000	1343.2	13656.8
D72	SoC_COME_PCIE4_TXDN6	15000	1344.6	13655.39
D74	SoC_COME_PCIE4_TXDP7	15000	1240.7	13759.29
D75	SoC_COME_PCIE4_TXDN7	15000	1240.5	13759.54
D78	SoC_COME_PCIE4_TXDP8	15000	1719.2	13280.76
D79	SoC_COME_PCIE4_TXDN8	15000	1722	13277.99
D81	SoC_COME_PCIE4_TXDP9	15000	1516.8	13483.22
D82	SoC_COME_PCIE4_TXDN9	15000	1514.6	13485.45
D85	SoC_COME_PCIE4_TXDP10	15000	1468.6	13531.44
D86	SoC_COME_PCIE4_TXDN10	15000	1467.4	13532.57

D88	SoC_COME_PCIE4_TXDP11	15000	1488.2	13511.81
D89	SoC_COME_PCIE4_TXDN11	15000	1488.8	13511.2
D91	SoC_COME_PCIE4_TXDP12	15000	1557.5	13442.54
D92	SoC_COME_PCIE4_TXDN12	15000	1554.2	13445.85
D94	SoC_COME_PCIE4_TXDP13	15000	1538.3	13461.74
D95	SoC_COME_PCIE4_TXDN13	15000	1536.4	13463.56
D98	SoC_COME_PCIE4_TXDP14	15000	1570.4	13429.58
D99	SoC_COME_PCIE4_TXDN14	15000	1569.8	13430.25
D101	SoC_COME_PCIE4_TXDP15	15000	1587.8	13412.23
D102	SoC_COME_PCIE4_TXDN15	15000	1588.4	13411.6
A88	COMe_PCIe_GEN3_CLKP	16000	4306.4	11693.62
A89	COMe_PCIe_GEN3_CLKN	16000	4310.2	11689.78

Table 5 Carrier Available Traces – PEG(Gen3)

3.1.7 Max Trace Length and Available Carrier Trace Length – PEG (Gen 4) Add-In Card

That follow provide layout guidelines for low-loss material

Pin	Signal	Max Length	Module length	Available carrier length
C52	COME_SoC_PCIE4_RXDP0	8000	1566.41	6433.59
C53	COME_SoC_PCIE4_RXDN0	8000	1568.11	6431.89
C55	COME_SoC_PCIE4_RXDP1	8000	1564.21	6435.79
C56	COME_SoC_PCIE4_RXDN1	8000	1565.49	6434.51
C58	COME_SoC_PCIE4_RXDP2	8000	1603.6	6396.4
C59	COME_SoC_PCIE4_RXDN2	8000	1601.05	6398.95
C61	COME_SoC_PCIE4_RXDP3	8000	1457.09	6542.91
C62	COME_SoC_PCIE4_RXDN3	8000	1458.71	6541.29
C65	COME_SoC_PCIE4_RXDP4	8000	1547.39	6452.61
C66	COME_SoC_PCIE4_RXDN4	8000	1544.68	6455.32
C68	COME_SoC_PCIE4_RXDP5	8000	1502.12	6497.88
C69	COME_SoC_PCIE4_RXDN5	8000	1503.87	6496.13
C71	COME_SoC_PCIE4_RXDP6	8000	1536.73	6463.27
C72	COME_SoC_PCIE4_RXDN6	8000	1534.74	6465.26
C74	COME_SoC_PCIE4_RXDP7	8000	1491.9	6508.1
C75	COME_SoC_PCIE4_RXDN7	8000	1493.52	6506.48
C78	COME_SoC_PCIE4_RXDP8	8000	1556.27	6443.73
C79	COME_SoC_PCIE4_RXDN8	8000	1556.55	6443.45
C81	COME_SoC_PCIE4_RXDP9	8000	1533.52	6466.48
C82	COME_SoC_PCIE4_RXDN9	8000	1535.66	6464.34
C85	COME_SoC_PCIE4_RXDP10	8000	1581.84	6418.16
C86	COME_SoC_PCIE4_RXDN10	8000	1579.61	6420.39

C88	COME_SoC_PCIE4_RXDP11	8000	1546.39	6453.61
C89	COME_SoC_PCIE4_RXDN11	8000	1547.99	6452.01
C91	COME_SoC_PCIE4_RXDP12	8000	1595.24	6404.76
C92	COME_SoC_PCIE4_RXDN12	8000	1593.26	6406.74
C94	COME_SoC_PCIE4_RXDP13	8000	1669.86	6330.14
C95	COME_SoC_PCIE4_RXDN13	8000	1671.01	6328.99
C98	COME_SoC_PCIE4_RXDP14	8000	1806.99	6193.01
C99	COME_SoC_PCIE4_RXDN14	8000	1806.04	6193.96
C101	COME_SoC_PCIE4_RXDP15	8000	1881.13	6118.87
C102	COME_SoC_PCIE4_RXDN15	8000	1881.93	6118.07
D52	SoC_COME_PCIE4_TXDP0	8000	1157.71	6842.29
D53	SoC_COME_PCIE4_TXDN0	8000	1155.74	6844.26
D55	SoC_COME_PCIE4_TXDP1	8000	1125.44	6874.56
D56	SoC_COME_PCIE4_TXDN1	8000	1126.49	6873.51
D58	SoC_COME_PCIE4_TXDP2	8000	1250.83	6749.17
D59	SoC_COME_PCIE4_TXDN2	8000	1251.04	6748.96
D61	SoC_COME_PCIE4_TXDP3	8000	1125.05	6874.95
D62	SoC_COME_PCIE4_TXDN3	8000	1125.27	6874.73
D65	SoC_COME_PCIE4_TXDP4	8000	1399.44	6600.56
D66	SoC_COME_PCIE4_TXDN4	8000	1398.68	6601.32
D68	SoC_COME_PCIE4_TXDP5	8000	1231.16	6768.84
D69	SoC_COME_PCIE4_TXDN5	8000	1231.79	6768.21
D71	SoC_COME_PCIE4_TXDP6	8000	1343.2	6656.8
D72	SoC_COME_PCIE4_TXDN6	8000	1344.61	6655.39
D74	SoC_COME_PCIE4_TXDP7	8000	1240.71	6759.29
D75	SoC_COME_PCIE4_TXDN7	8000	1240.46	6759.54
D78	SoC_COME_PCIE4_TXDP8	8000	1719.24	6280.76
D79	SoC_COME_PCIE4_TXDN8	8000	1722.01	6277.99

D81	SoC_COME_PCIE4_TXDP9	8000	1516.78	6483.22
D82	SoC_COME_PCIE4_TXDN9	8000	1514.55	6485.45
D85	SoC_COME_PCIE4_TXDP10	8000	1468.56	6531.44
D86	SoC_COME_PCIE4_TXDN10	8000	1467.43	6532.57
D88	SoC_COME_PCIE4_TXDP11	8000	1488.19	6511.81
D89	SoC_COME_PCIE4_TXDN11	8000	1488.8	6511.2
D91	SoC_COME_PCIE4_TXDP12	8000	1557.46	6442.54
D92	SoC_COME_PCIE4_TXDN12	8000	1554.15	6445.85
D94	SoC_COME_PCIE4_TXDP13	8000	1538.26	6461.74
D95	SoC_COME_PCIE4_TXDN13	8000	1536.44	6463.56
D98	SoC_COME_PCIE4_TXDP14	8000	1570.42	6429.58
D99	SoC_COME_PCIE4_TXDN14	8000	1569.75	6430.25
D101	SoC_COME_PCIE4_TXDP15	8000	1587.77	6412.23
D102	SoC_COME_PCIE4_TXDN15	8000	1588.4	6411.6
B29	COME_PCIe_GEN4_CLKP	16000	1398.14	14601.86
B30	COME_PCIe_GEN4_CLKN	16000	1401.54	14598.46

Table 6 Carrier Available Traces – PEG(Gen4)

3.2 USB 2.0/3.0

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A42	SOC_USB2_DN2	USB differential pairs, channels 2.	I/O	USB	3.3V Suspend / 3.3V	-	-
A43	SOC_USB2_DP2	USB differential pairs, channels 2.	I/O	USB	3.3V Suspend / 3.3V	-	-
A45	SOC_USB2_DN0	USB differential pairs, channels 0.	I/O	USB	3.3V Suspend / 3.3V	-	-
A46	SOC_USB2_DP0	USB differential pairs, channels 0.	I/O	USB	3.3V Suspend / 3.3V	-	-
B42	SOC_USB2_DN3	USB differential pairs, channels 3.	I/O	USB	3.3V Suspend / 3.3V	-	-
B43	SOC_USB2_DP3	USB differential pairs, channels 3.	I/O	USB	3.3V Suspend / 3.3V	-	-
B45	SOC_USB2_DN1	USB differential pairs, channels 1.	I/O	USB	3.3V Suspend / 3.3V	-	-
B46	SOC_USB2_DP1	USB differential pairs, channels 1.	I/O	USB	3.3V Suspend / 3.3V	-	-
C3	USB3_HSIO20_RXN0	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
C4	USB3_HSIO20_RXP0	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
C6	USB3_HSIO21_RXN1	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		

C7	USB3_HSIO21_RXP1	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
C9	USB3_HSIO22_RXN2	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
C10	USB3_HSIO22_RXP2	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
C12	USB3_HSIO23_RXN3	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
C13	USB3_HSIO23_RXP3	Additional receive signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module		
D3	USB3_HSIO20_TXN0	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D4	USB3_HSIO20_TXP0	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D6	USB3_HSIO21_TXN1	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D7	USB3_HSIO21_TXP1	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D9	USB3_HSIO22_TXN2	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D10	USB3_HSIO22_TXP2	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D12	USB3_HSIO23_TXN3	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		
D13	USB3_HSIO23_TXP3	Additional receive signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module		

Table 5 USB Pin Out

3.2.1 PCB Layout Guideline – USB 2.0 / 3.0

Parameter	Trace Routing
Transfer rate / Port	480 MBit/s
Maximum signal line length (coupled traces)	Max. 17.0 inches
Signal length used on COM Express Module (including the COM Express connector)	3.0 inches
Signal length allowance for the COM Express Carrier Board	14.0 inches
Differential Impedance	90 Ω +/-15%
Single-ended Impedance	45 Ω +/-10%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	150mils
Reference plane	GND referenced preferred
Spacing from edge of plane	Min. 40mils
Via Usage	Try to minimize number of vias

Note: USB 2.0 for this platform differential Impedance is 85 OHM

Table 6 Layout Guideline – USB 2.0

Parameter	Trace Routing
Transfer rate / Port	5.0 GBit/s
Maximum signal line length (coupled traces)	7.5 inches
Signal length used on COM Express Module (including the COM Express connector)	3.0 inches
Signal length allowance for the COM Express Carrier Board	4.5 inches
Differential Impedance	85 Ω +/-10%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 15mils
Spacing between differential pairs and high-speed periodic signals	Min. 15mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Reference plane	Ground
Spacing from edge of plane	Min. 40mils
Via Usage	Max. 3 vias per differential signal trace

Table 7 Layout Guideline – USB 3.0

3.2.2 Reference Schematic – USB 2.0 / 3.0

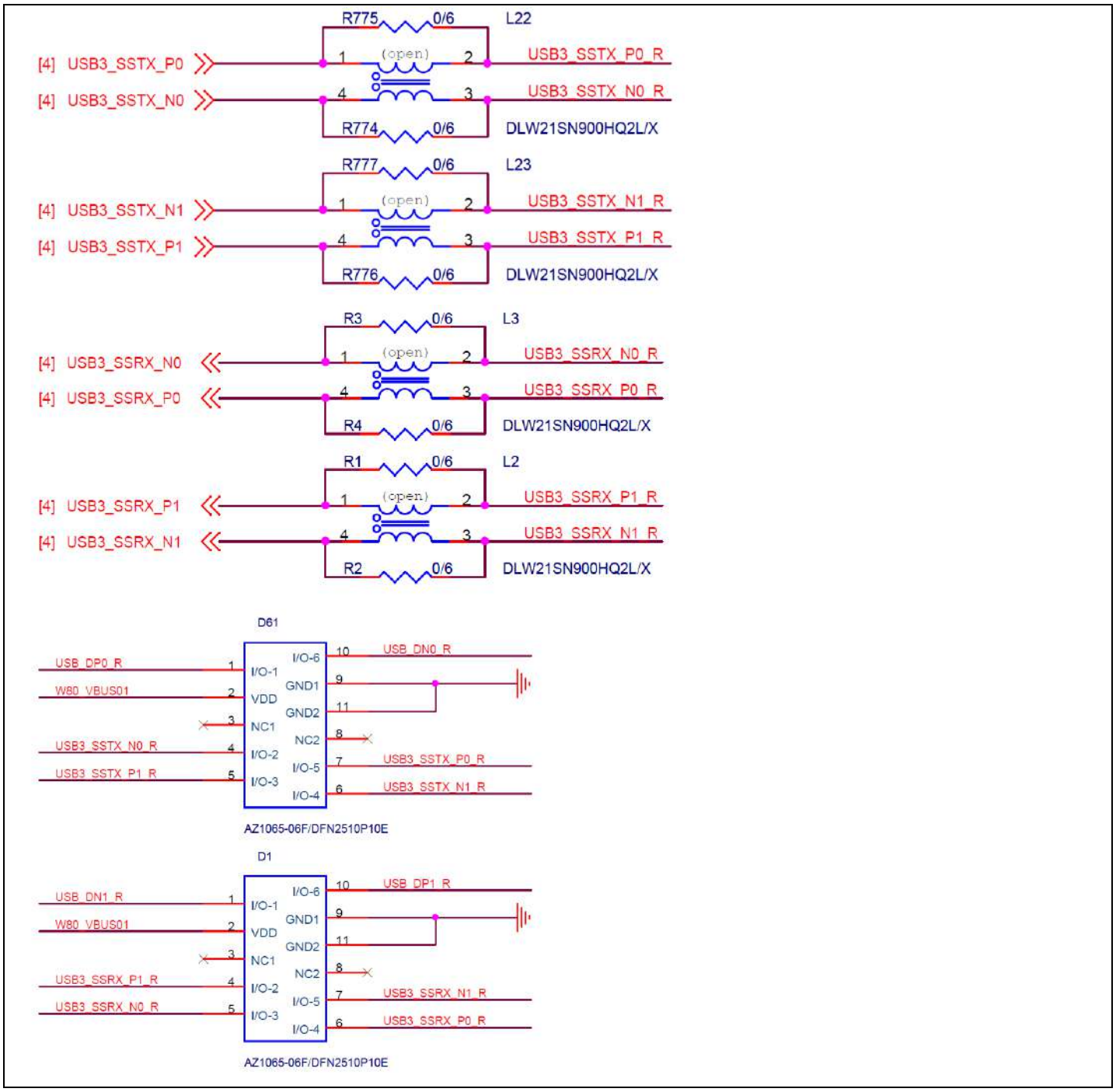

Figure 6 USB 2.0 / 3.0 Reference Schematic 1

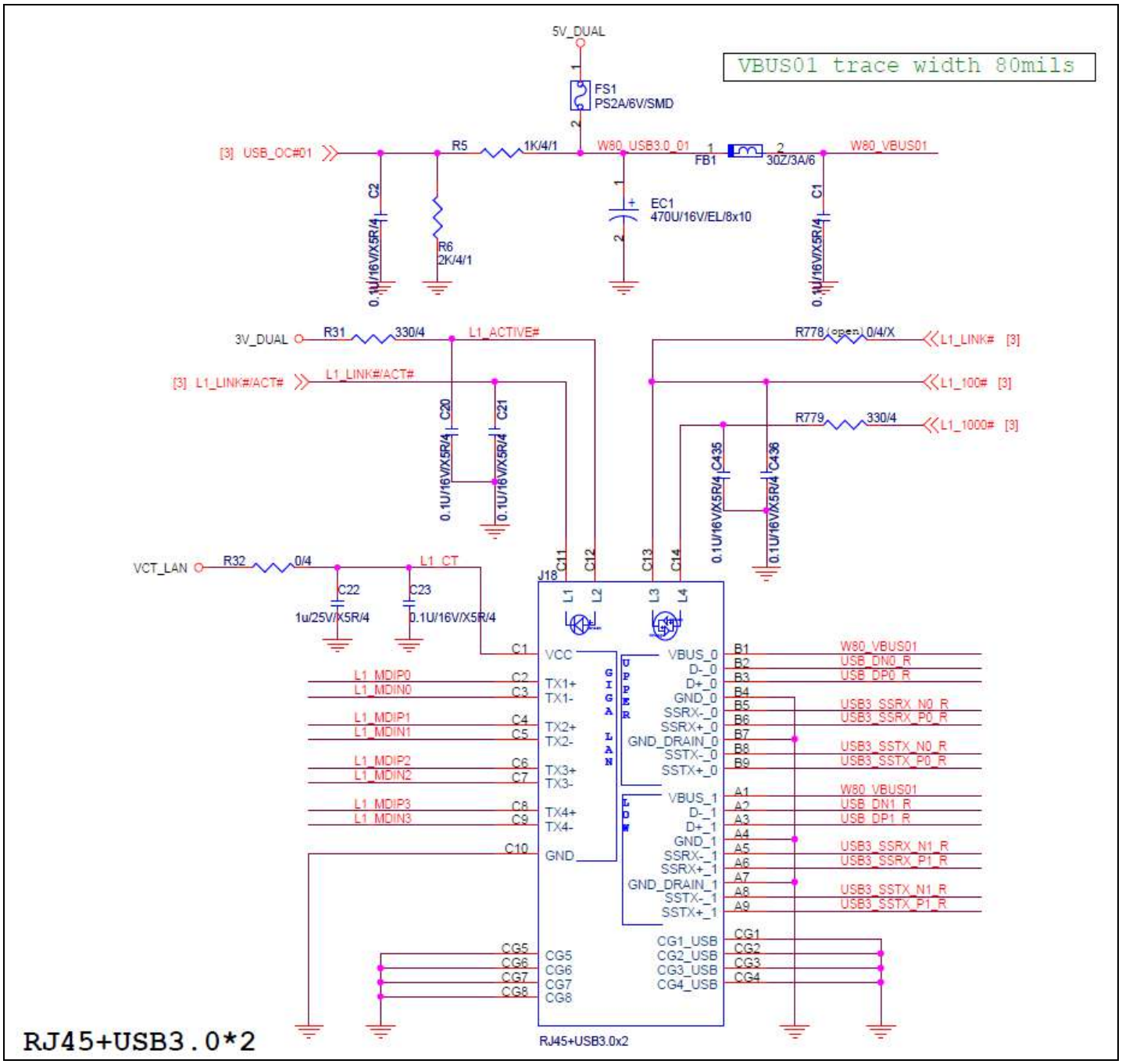

Figure 7 USB 2.0/3.0 Reference Schematic 2

3.2.3 Max Trace Length and Available Carrier Trace Length - USB 2.0 / 3.0

That follow provide layout guidelines for mid-loss material

Pin	Signal	Max Length	Module length	Available carrier length
A42	SOC_USB2_DN2	7000	4175.68	2824.32
A43	SOC_USB2_DP2	7000	4174.35	2825.65
A45	SOC_USB2_DN0	7000	3821.51	3178.49
A46	SOC_USB2_DP0	7000	3819.37	3180.63
B42	SOC_USB2_DN3	7000	3997.25	3002.75
B43	SOC_USB2_DP3	7000	3998.11	3001.89
B45	SOC_USB2_DN1	7000	3709.6	3290.4
B46	SOC_USB2_DP1	7000	3709.83	3290.17
C3	USB3_HSIO20_RXN0	5500	2121.51	3378.49
C4	USB3_HSIO20_RXP0	5500	2123.32	3376.68
C6	USB3_HSIO21_RXN1	5500	2152.37	3347.63
C7	USB3_HSIO21_RXP1	5500	2150.58	3349.42
C9	USB3_HSIO22_RXN2	5500	2112.51	3387.49
C10	USB3_HSIO22_RXP2	5500	2113.04	3386.96
C12	USB3_HSIO23_RXN3	5500	2496.23	3003.77
C13	USB3_HSIO23_RXP3	5500	2494.9	3005.1
D3	USB3_HSIO20_TXN0	5500	1697.13	3802.87
D4	USB3_HSIO20_TXP0	5500	1694.88	3805.12
D6	USB3_HSIO21_TXN1	5500	1718.45	3781.55

D7	USB3_HSIO21_TXP1	5500	1718.53	3781.47
D9	USB3_HSIO22_TXN2	5500	1839.7	3660.3
D10	USB3_HSIO22_TXP2	5500	1841.35	3658.65
D12	USB3_HSIO23_TXN3	5500	1937.22	3562.78
D13	USB3_HSIO23_TXP3	5500	1936.04	3563.96

Table 8 Carrier Available Traces – USB 2.0 / 3.0

3.3 GbE LAN

External Ethernet magnetic shall be implemented on the Carrier Board.

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A2	I210_MDI3_N	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A3	I210_MDI3_P	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A4	I210_100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A5	I210_1G#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A6	I210_MDI2_N	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A7	I210_MDI2_P	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A8	I210_LINK#	Gigabit Ethernet Controller 0 link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A9	I210_MDI1_N	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A10	I210_MDI1_P	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A12	I210_MDI0_N	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A13	I210_MDI0_P	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A49	GBE0_SDP	Gigabit Ethernet Controller 0 Software-Definable Pins. Can also be used for	I/O	CMOS	3.3V Suspend /	-	-

B2	I210_ACT#	Gigabit Ethernet Controller 1 activity indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-

Table 9 GbE LAN Pin Out

3.3.1 PCB Layout Guideline - GbE LAN

Parameter	Trace Routing
Signal length allowance for the COM Express Carrier Board	5.0 inches from the COM Express Module to the magnetics Module
Maximum signal length between isolation magnetics Module and RJ45 connector on the Carrier Board	1.0 inch
Differential Impedance	95 Ω +/-20%
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50mils
Spacing between differential pairs and high-speed periodic signals	Min. 300mils
Spacing between differential pairs and low-speed non periodic signals	Min. 100mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	Max. 30mils
Spacing between digital ground and analog ground plane (between the magnetics Module and RJ45 connector)	Min. 60mils
Spacing from edge of plane	Min. 40mils
Via Usage	Max. of 2 vias on TX path Max. of 2 vias on RX path

Note: GbE LAN for this platform differential Impedance is 100 OHM

Table 10 Layout Guideline – GbE LAN

3.3.2 Max Trace Length and Available Carrier Trace Length – GbE LAN

That follow provide layout guidelines for mid-loss material

Pin	Signal	Module length	Available carrier length
A2	I210_MDI3_N	766.33	2100.00
A3	I210_MDI3_P	765.09	2100.00
A6	I210_MDI2_N	698.17	2100.00
A7	I210_MDI2_P	694.37	2100.00
A9	I210_MDI1_N	751.03	2100.00
A10	I210_MDI1_P	749.78	2100.00
A12	I210_MDI0_N	705.58	2100.00
A13	I210_MDI0_P	706.41	2100.00

Table 10 Carrier Available Traces – GbE LAN

3.4 SATA

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A16	SATA_HSIO17_TXP17	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A17	SATA_HSIO17_TXN17	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A19	SATA_HSIO17_RXP17	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A20	SATA_HSIO17_RXN17	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
B16	SATA_HSIO18_TXP18	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B17	SATA_HSIO18_TXN18	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B19	SATA_HSIO18_RXP18	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B20	SATA_HSIO18_RXN18	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-

Table 11 SATA Pin Out

3.4.1 PCB Layout Guideline - SATA

Parameter	Trace Routing
Transfer Rate	Up to 6.0 GBit/s
Maximum signal line length (coupled traces)	5.0 inches on PCB (COM Express Module and Carrier Board. The length of the SATA cable is specified between 0 and 40 inches)
Signal length used on COM Express Module (including the COM Express Carrier Board connector)	2 inches
Signal length available for the COM Express Carrier Board	3 inches, a redriver may be necessary for GEN3 signaling rates
Differential Impedance	85 Ω +/-20%
Single-ended Impedance	50 Ω +/-15%
Trace width (W)	PCB stack-up dependent
Spacing between differential pairs (intra-pair) (S)	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict length-matching requirements. Route the signals as directly as possible.
Spacing from edge of plane	Min. 40mils
Via Usage	A maximum of 2 vias is recommended.
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are incorporated on the COM Express Module.

Table 12 Layout Guideline – SATA

3.4.2 Max Trace Length and Available Carrier Trace Length – SATA

That follow provide layout guidelines for mid-loss material

Pin	Signal	Max Length	Module length	Available carrier length
A16	SATA_HSIO17_TXP17	6000	2567.14	3432.86
A17	SATA_HSIO17_TXN17	6000	2566.87	3433.13
A19	SATA_HSIO17_RXP17	6000	2619.1	3380.9
A20	SATA_HSIO17_RXN17	6000	2618.64	3381.36
B16	SATA_HSIO18_TXP18	6000	2163.29	3836.71
B17	SATA_HSIO18_TXN18	6000	2163.5	3836.5
B19	SATA_HSIO18_RXP18	6000	2057.62	3942.38
B20	SATA_HSIO18_RXN18	6000	2056.74	3943.26

Table 13 Carrier Available Traces – SATA

3.5 NCSI

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A84	LAN_NCSI_TXEN	NCSI Transmit Enable	I	-	3.3V Suspend / 3.3V	Module PD 10K	-
B89	NCSI_RX_ER_CN	NC-SI Receive error	O	-	3.3V Suspend / 3.3V	NC	-
B91	LAN_NCSI_CLKIN	NC-SI Clock reference for receive, transmit, and control interface.	I	-	3.3V Suspend / 3.3V	Module PD 10K	-
B92	LAN_NCSI_RXD1	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Module PU 10K	-
B93	LAN_NCSI_RXD0	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Module PU 10K	-
B94	LAN_NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O	-	3.3V Suspend / 3.3V	Module PD 10K	-
B95	LAN_NCSI_TXD1	NC-SI Transmit Data (from BMC to NC).	I	-	3.3V Suspend / 3.3V	Module PU 10K	-
B96	LAN_NCSI_TXD0	NC-SI Transmit Data (from BMC to NC).	I	-	3.3V Suspend / 3.3V	Module PU 10K	-
B98	NCSI_ARB_IN	NC-SI hardware arbitration input.	I	-	3.3V Suspend / 3.3V	Module PU 10K	-
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output.	O	-	3.3V Suspend / 3.3V	-	-

Table 14 NCSI Pin Out

3.5.1 Max Trace Length and Available Carrier Trace Length - NCSI

That follow provide layout guidelines for mid-loss material

Pin	Signal	Max Length	Module length	Available carrier length
A84	LAN_NCSI_TXEN	7000	2,256.08	4743.92
B91	LAN_NCSI_CLKIN	7000	2,052.70	4947.3
B92	LAN_NCSI_RXD1	7000	2,072.35	4927.65
B93	LAN_NCSI_RXD0	7000	2,333.79	4666.21
B94	LAN_NCSI_CRS_DV	7000	2,051.17	4948.83
B95	LAN_NCSI_TXD1	7000	2647.22	4352.78
B96	LAN_NCSI_TXD0	7000	2969.69	4030.31
B98	NCSI_ARB_IN	7000	3323.64	3676.36
B99	NCSI_ARB_OUT	7000	2786.81	4213.19

Table 15 Carrier Available Traces – NCSI

3.6 10GbE LAN

Pin out

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
D26	ETH0_COME_KR_TXDP3	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D27	ETH0_COME_KR_TXDN3	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D29	ETH0_COME_KR_TXDP2	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D30	ETH0_COME_KR_TXDN2	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D32	NAC_I2C_SCL3	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-
D33	NAC_I2C_SCL2	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-
C26	COME_ETH0_KR_RXDP3	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C27	COME_ETH0_KR_RXDN3	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module		
C29	COME_ETH0_KR_RXDP2	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C30	COME_ETH0_KR_RXDN2	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C15	10PHY_MDC3_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	NC	-

C16	10PHY_MDC2_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	NC	-
C24	10G_INT2_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.	I	CMOS	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-
D15	10PHY_MDA3_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	NC	-
D16	10PHY_MDA2_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	NC	-
D34	10GPHY_SEL23_CN	Indicates if the PHY for 10G lanes 2 and 3 is capable of configuration by I²C. High indicates MDIO-only configuration, and low indicates configuration capability via I²C or MDIO.	I	CMOS	3.3V Suspend / 3.3V	Module PU 10kohm to 3.3V	
D35	CEI_PRSNT#	Input signal from Carrier indicating presence of CEI compliant hardware on the Carrier	I	CMOS	3.3V Suspend / 3.3V	Module PU 10kohm to 3.3V	For COM.0 Rev 3.1
D38	NAC_I2C_SCL1	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-
D39	CEI_SCL	I2C clock for CEI I2C port	I/O	OD	3.3V Suspend / 3.3V	Module PU 10kohm to 3.3V	For COM.0 Rev 3.1
D40	10G_PORT1_SDP	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 10kohm to 3.3V	-
D42	ETH0_COME_KR_TXDP1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D43	ETH0_COME_KR_TXDN1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at	-	-

					receiver		
D45	10PHY_MDA1_CN	MDIO Mode / I2C Mode	O, I/O	CMOS	3.3V Suspend / 3.3V	NC	-
D46	CEI_MDIO	MDIO data – for PHY setup	I/O OD	-	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	For COM.0 Rev 3.1
D47	ETH_PHY_INT#	Second active low interrupt input to Module from Carrier based I2C I/O expander	I	CMOS	3.3V Suspend / 3.3V	Module PU 20kohm to 3.3V	For COM.0 Rev. 3.1
D49	ETH0_COME_KR_TXDP0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D50	ETH0_COME_KR_TXDN0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
C32	NAC_I2C_SDA3	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-
C33	NAC_I2C_SDA2	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-
C34	10GPHY_RST23_CN	Output signal that resets an optical PHY on port 2 and port 3 (with copper PHY this signal is not used).	O	CMOS	3.3V Suspend / 3.3V	NC	
C35	CEI_RST#	Active low reset output from Module to Carrier based I/O expander	O	CMOS	3.3V Suspend / 3.3V	Module PD 10kohm	For COM.0 Rev 3.1
C39	CEI_SDA	I2C data – for SFP setup, serialized status LEDs and miscellaneous serialized signals.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 10kohm to 3.3V	For COM.0 Rev 3.1
C40	10G_PORT0_SDP	Software-Definable Pins. Can also be used for IEEE1588	I/O	CMOS	3.3V Suspend /	-	-

		support such as a 1pps signal.			3.3V		
C42	COME_ETH0_KR_RXDP1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C43	COME_ETH0_KR_RXDN1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C45	10PHY_MDC1_CN	MDIO Mode / I2C Mode	O	-	3.3V Suspend / 3.3V	NC	-
C46	CEI_MDC	MDIO clock - for PHY setup	O, I/O	CMOS	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	For COM.0 Rev 3.1
C47	CEI_INT#	Active low interrupt input to Module from Carrier based I2C I/O expander	I	CMOS	3.3V Suspend / 3.3V	Module PU 10k ohm to 3.3V	For COM.0 Rev 3.1
C49	COME_ETH0_KR_RXDP0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C50	COME_ETH0_KR_RXDN0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C36	10G_LED_SDA	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 4.7kohm to 3.3V	-
C37	10G_LED_SCL	I2C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 4.7kohm to 3.3V	-
C38	NAC_I2C_SDA1	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-

Table 16 10GbE LAN Pin Out

3.6.1 Max Trace Length and Available Carrier Trace Length – 10GbE LAN

That follow provide layout guidelines for mid-loss material

Pin	Signal	Max Length	Module length	Available carrier length
D26	ETH0_COME_KR_TXDP3	14400	3958.38	10441.62
D27	ETH0_COME_KR_TXDN3	14400	3958.23	10441.77
D29	ETH0_COME_KR_TXDP2	14400	3846.38	10553.62
D30	ETH0_COME_KR_TXDN2	14400	3846.91	10553.09
D32	NAC_I2C_SCL3	10000	2923.96	7076.04
D33	NAC_I2C_SCL2	10000	3086.79	6913.21
C26	COME_ETH0_KR_RXDP3	14400	4086.8	10313.2
C27	COME_ETH0_KR_RXDN3	14400	4087.41	10312.59
C29	COME_ETH0_KR_RXDP2	14400	4299.46	10100.54
C30	COME_ETH0_KR_RXDN2	14400	4299.48	10100.52
D38	NAC_I2C_SCL1	10000	2681.11	7318.89
D39	CEI_SCL	10000	1865.53	8134.47
D42	ETH0_COME_KR_TXDP1	14400	3660	10740
D43	ETH0_COME_KR_TXDN1	14400	3659.93	10740.07
D46	CEI_MDIO	8600	5312.47	3287.53
D49	ETH0_COME_KR_TXDP0	14400	3851.14	10548.86
D50	ETH0_COME_KR_TXDN0	14400	3851.69	10548.31
C32	NAC_I2C_SDA3	10000	3168.78	6831.22
C33	NAC_I2C_SDA2	10000	2891.91	7108.09
C39	CEI_SDA	10000	2188.61	7811.39
C42	COME_ETH0_KR_RXDP1	14400	3918.24	10481.76
C43	COME_ETH0_KR_RXDN1	14400	3918.42	10481.58
C46	CEI_MDC	9100	4270.87	4829.13
C49	COME_ETH0_KR_RXDP0	14400	3986.7	10413.3
C50	COME_ETH0_KR_RXDN0	14400	3986.34	10413.66
C36	10G_LED_SDA	10000	1839.78	8160.22
C37	10G_LED_SCL	10000	2037.92	7962.08
C38	NAC_I2C_SDA1	10000	2734.98	7265.02

Table 17 Carrier Available Traces – 10GbE LAN

3.7 UART

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A50	ESPI_ALERT1#_SIRQ	LPC serial interrupt / Shared pin with ESPI_CS1#	I/O	CMOS	3.3V / 3.3V	Module PU 1K ohm to 3.3V	-
A98	SER0_TX	General purpose serial port transmitter	O	CMOS	3.3V / 12V	Module PD 4.7K	-
A99	SER0_RX	General purpose serial port receiver	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O	CMOS	3.3V / 12V	Module PD 4.7K	-
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-

Table 18 UART Pin Out

3.7.1 Reference Schematic - UART

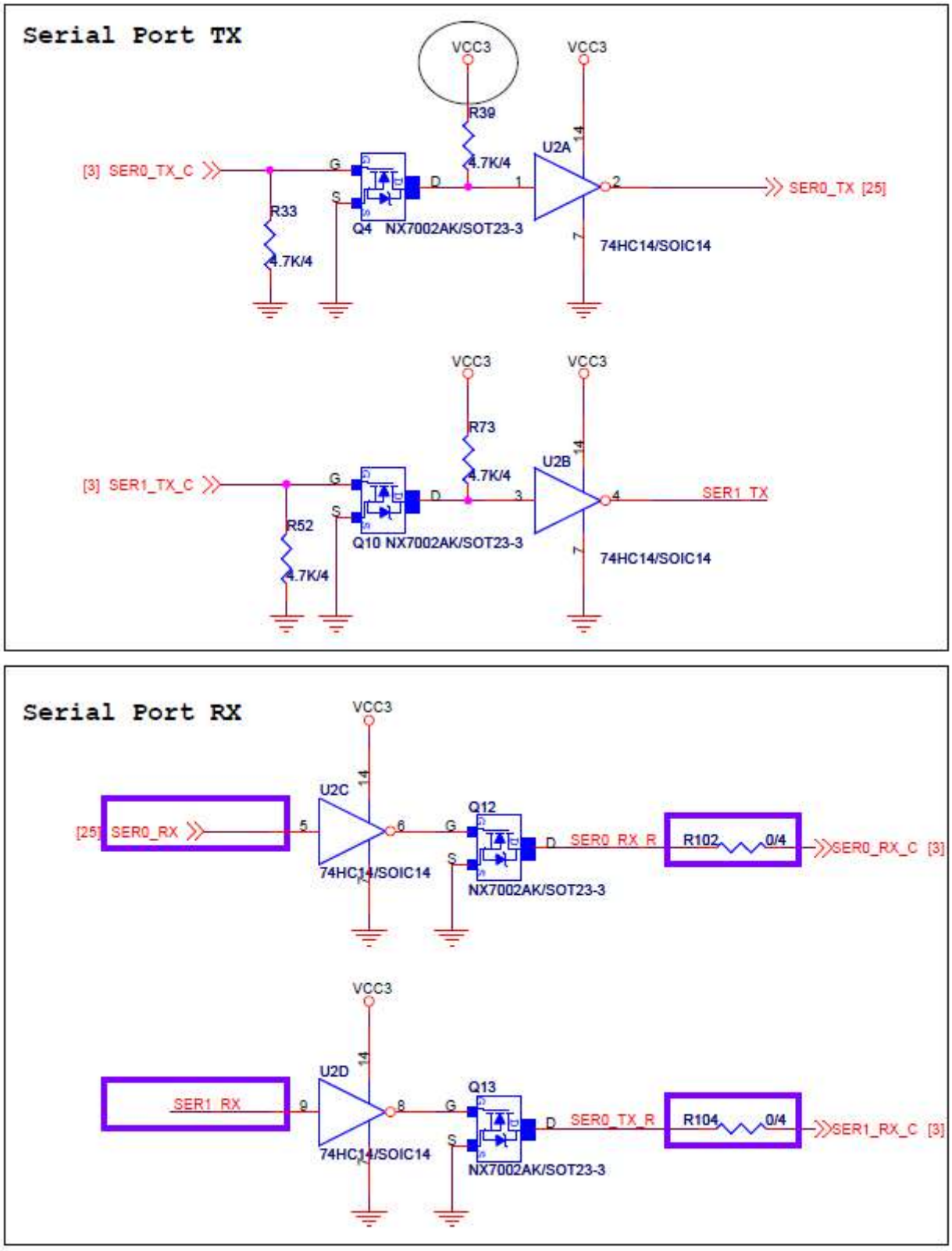

Figure 8 UART Reference Schematic 1

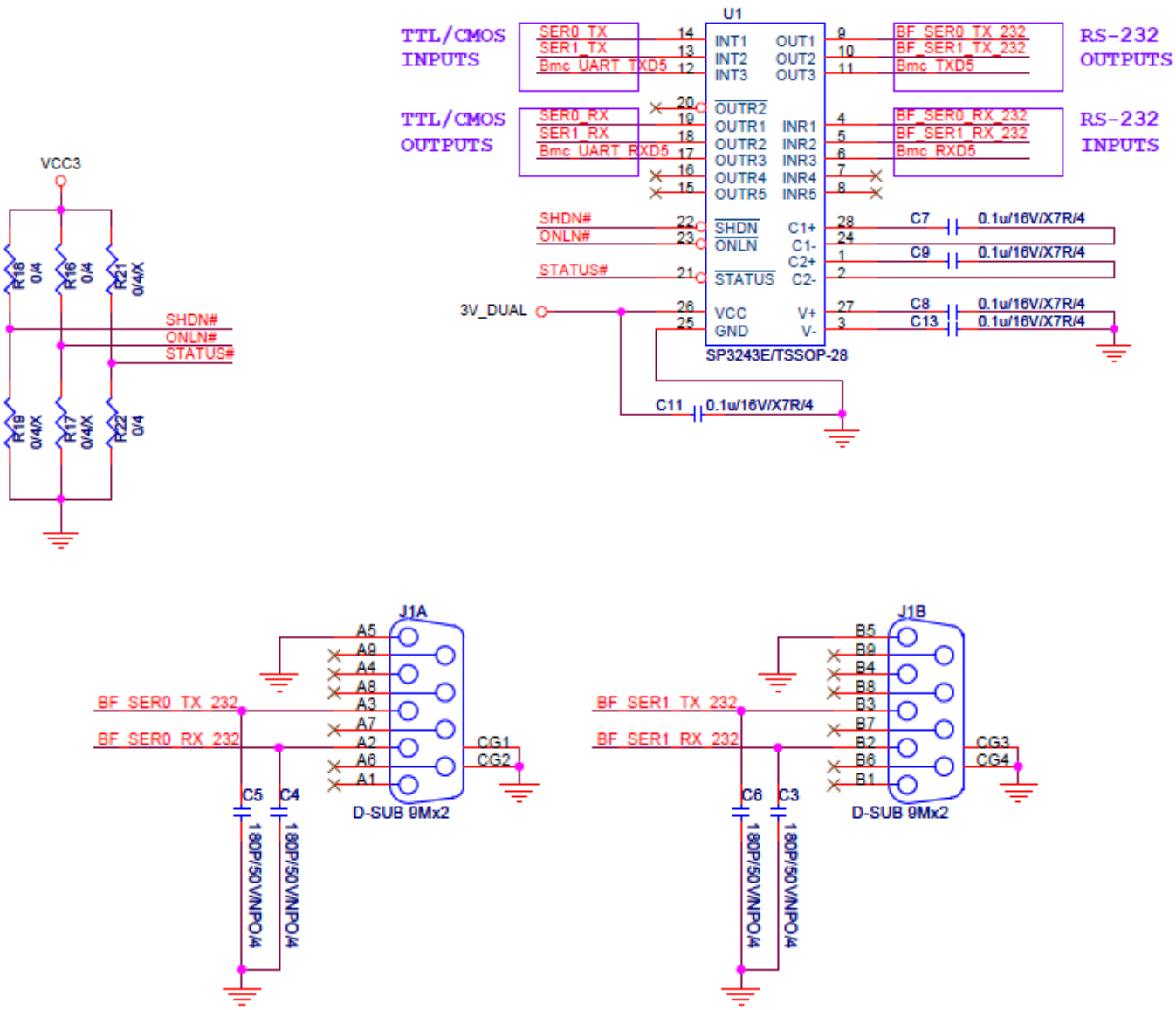

Figure 9 UART Reference Schematic 2

3.8 I2C

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
B33	SMB1_CLK_COMe	General purpose I2C port clock output	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 4.7k ohm to 3.3V	-
B34	SMB1_DATA_COMe	General purpose I2C port data I/O line	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 4.7k ohm to 3.3V	-

Table 19 I2C Pin Out

3.9 SMBus

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
B13	SoC_SMB_SCL	System Management Bus bidirectional clock line.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 10k ohm to 3.3V	-
B14	SoC_SMB_SDA	System Management Bus bidirectional data line.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 10k ohm to 3.3V	-
B15	SoC_SMB_ALERT#	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I	CMOS	3.3V Suspend / 3.3V	-	-

Table 20 SMBus Pin Out

3.10 GPIO

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A54	EC_GPI0	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	Module PU 10k ohm to 3.3V	-
A63	EC_GPI1	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	Module PU 4.7k ohm to 3.3V	-
A67	EC_GPI2	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	Module PU 4.7k ohm to 3.3V	-
A85	EC_GPI3	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	Module PU 4.7k ohm to 3.3V	-
A93	EC_GPO0	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B54	EC_GPO1	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B57	EC_GPO2	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B63	EC_GPO3	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-

Table 21 GPIO Pin Out

3.11 LPC

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A50	ESPI_ALERT1#_SIRQ	LPC serial interrupt / Shared pin with ESPI_CS1#	I/O	CMOS	3.3V / 3.3V	Module PU 1K ohm to 3.3V	-
B3	ESPI_CS1#_FRAME#	LPC frame indicates the start of an LPC cycle / Shared pin with ESPI_CS0#	O	CMOS	3.3V / 3.3V	-	-
B4	ESPI_IO0_LAD0	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-
B5	ESPI_IO1_LAD1	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-
B6	ESPI_IO2_LAD2	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-
B7	ESPI_IO3_LAD3	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-
B8	ESPI_ALERT1#_SIRQ	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	Module PU 1K ohm to 3.3V	-
B9	ESPI_ALERT#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	Module PU 1K ohm to 3.3V	-
B10	ESPI_CLK_COME	LPC clock output - 33MHz nominal / Shared pin with ESPI_Clock	O	CMOS	3.3V / 3.3V	-	-

Table 22 LPC Pin Out

3.12 SPI

An external SPI BIOS is designed on the Carrier board, which allows the Module boot from the Carrier SPI BIOS. To achieve this function, the BIOS_DIS0# and BIOS_DIS1# must be designed as a selectable method on the Carrier.

PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A34	BIOS_DIS0#	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low. Shared pin with ESPI_SAFS	I	CMOS	NA	-	-
A92	COME_SPI_MISO	Data in to Module from Carrier SPI	I	CMOS	3.3V Suspend / 3.3V	-	-
A94	COME_SPI_CLK	Clock from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A95	COME_SPI_MOSI	Data out from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
B8	ESPI_ALERT1#_SIRQ	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	PU 1K ohm to 3.3V	-
B9	ESPI_ALERT#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	PU 1K ohm to 3.3V	-

B47	COME_ESPI_EN#	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If pulled down by the Carrier LPC mode is selected. If pulled up or left floating, eSPI is selected if available. This signal is pulled up on the Module. This signal is a “don’t care” for Modules that do not support eSPI	I	CMOS	NA	PU 10K ohm to 3.3V	-
B88	BIOS_DIS1#	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low / Shared pin with ESPI_BBS	I	CMOS	NA	PU 10k ohm to 3.3V	-
B97	COME_SPI_CS0#	Chip select for Carrier Board SPI - maybe sourced from chipset SPI0 or SPI1	O	CMOS	3.3V Suspend / 3.3V	-	-

Table 23 SPI Pin Out

4 Power

PCOM-B705GT is designed for AT power mode, which depends on the power mode design on carrier board. The following AT mode power sequences are provided for the carrier design guideline.

4.1 Power Sequence

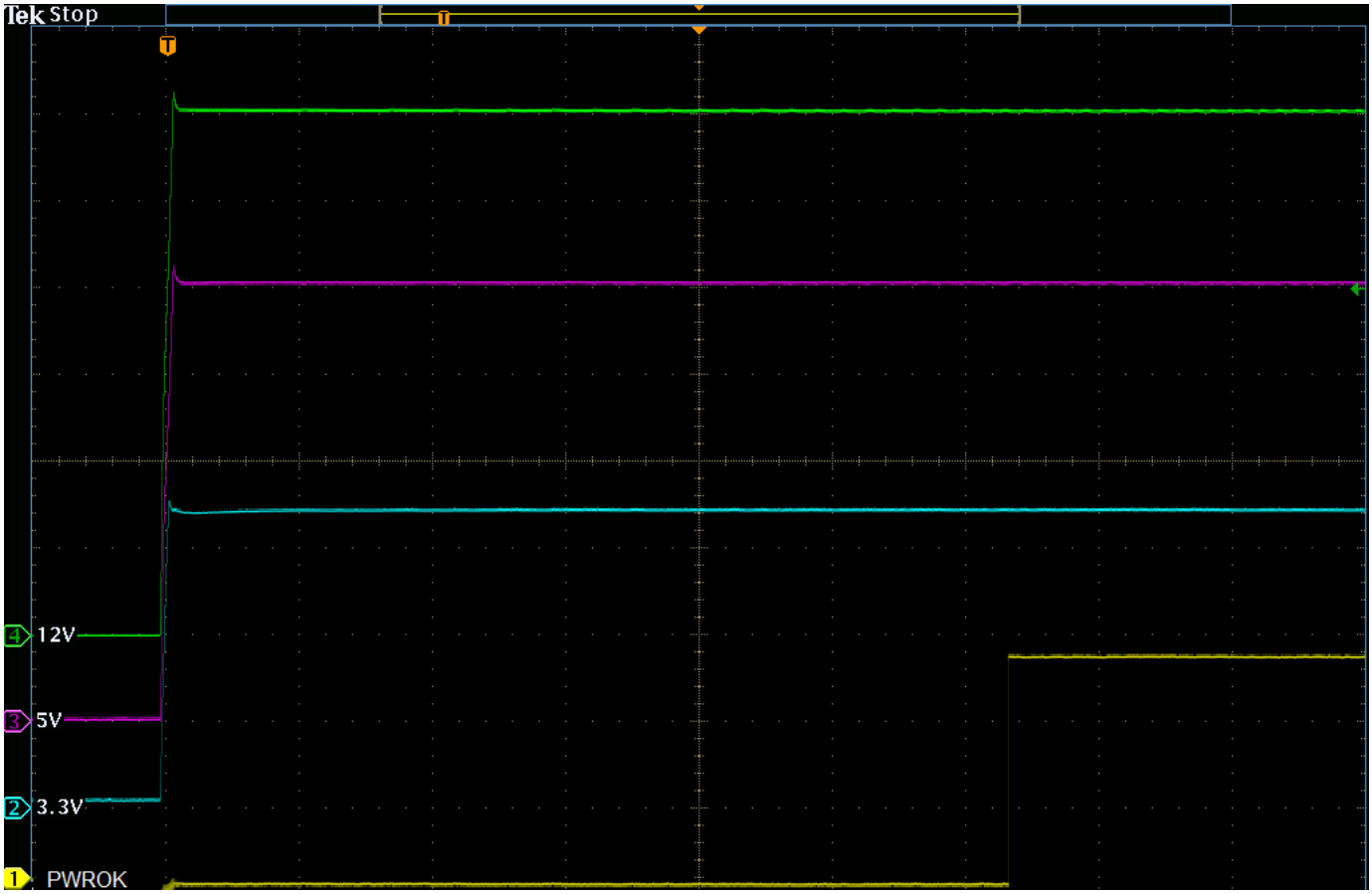

Figure 10 Power Sequence

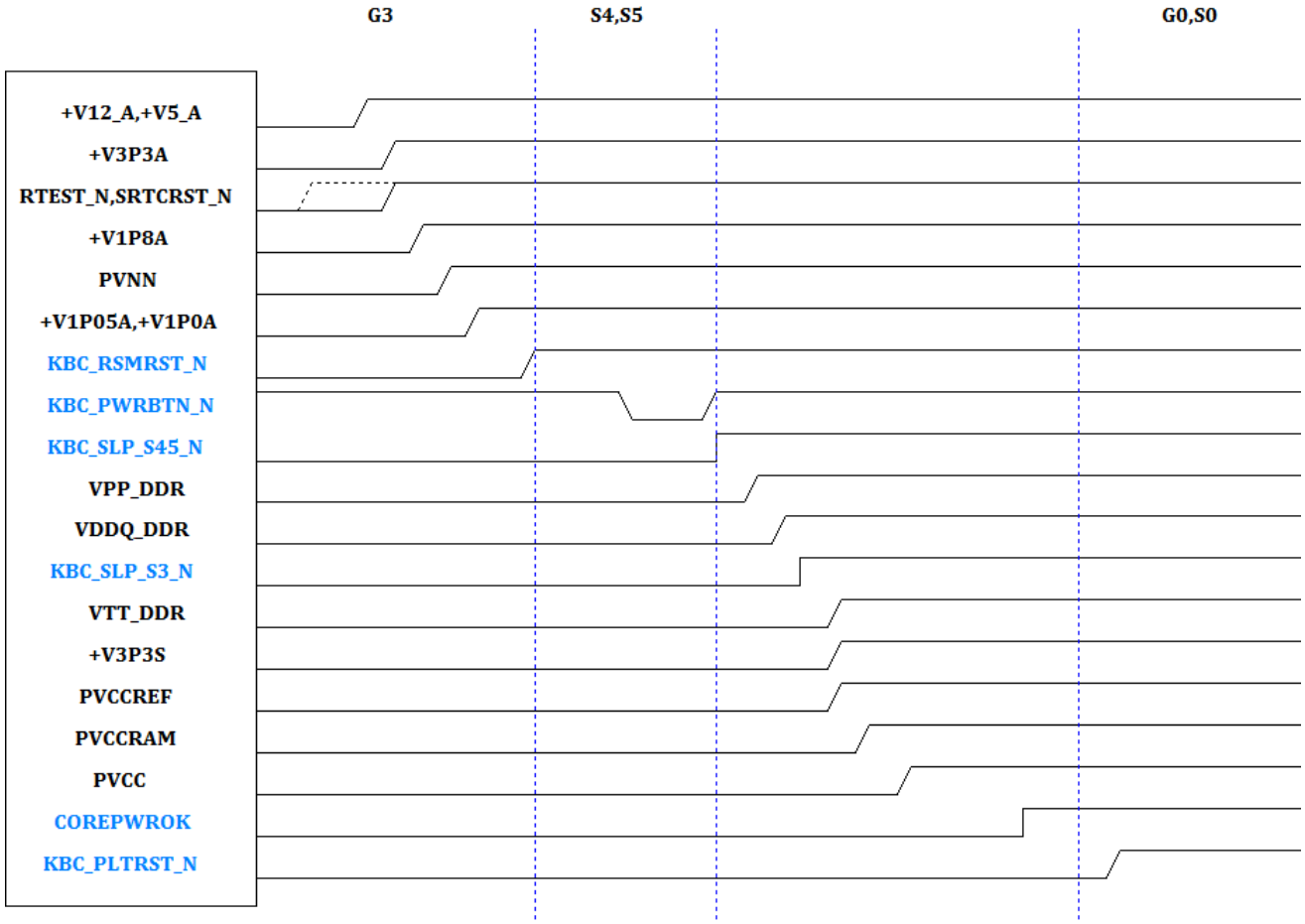

Figure 11 Carrier Power Sequence

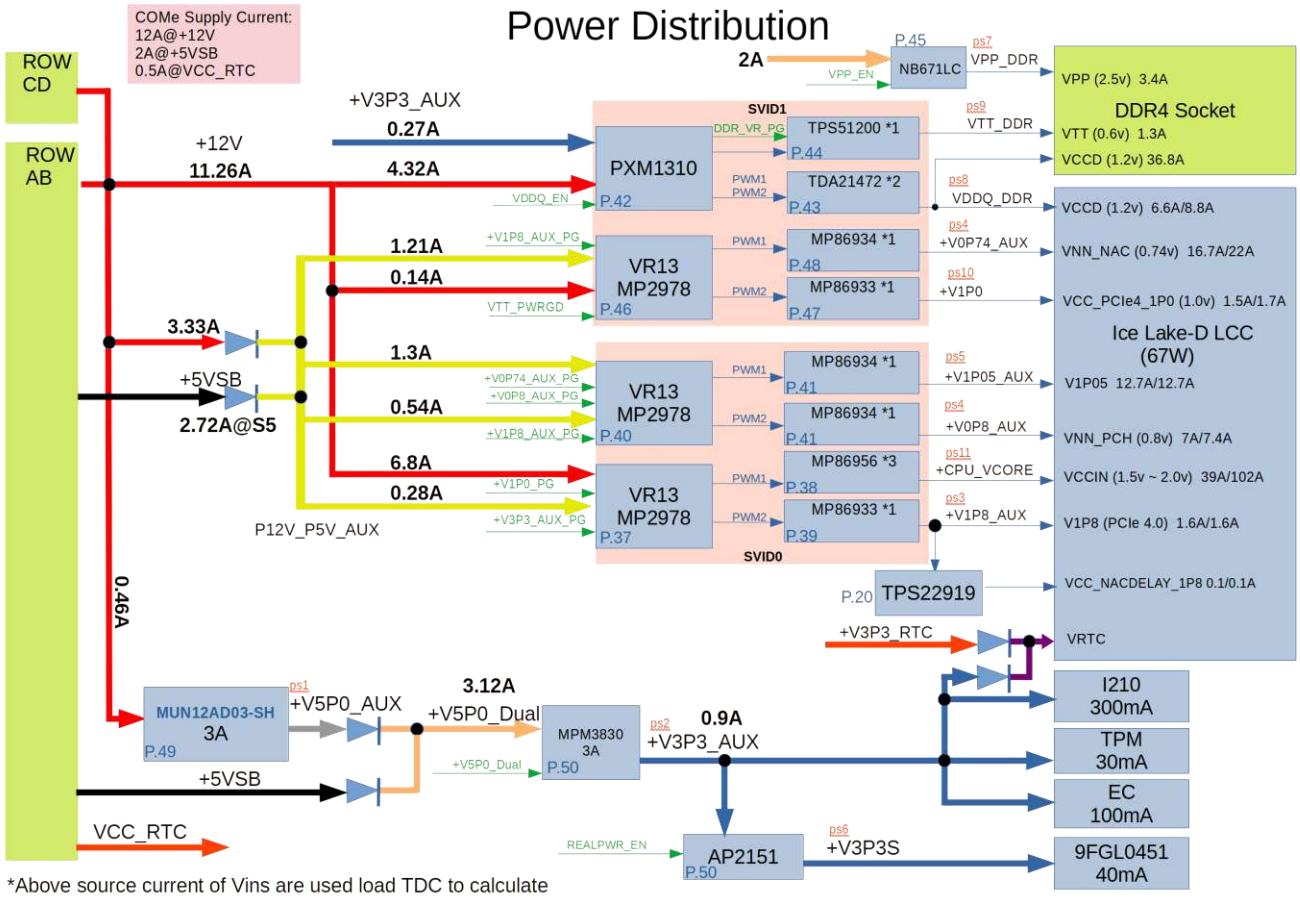

Figure 12 Power Distribution

5 Mechanical

5.1 PCOM-B705GT Dimension

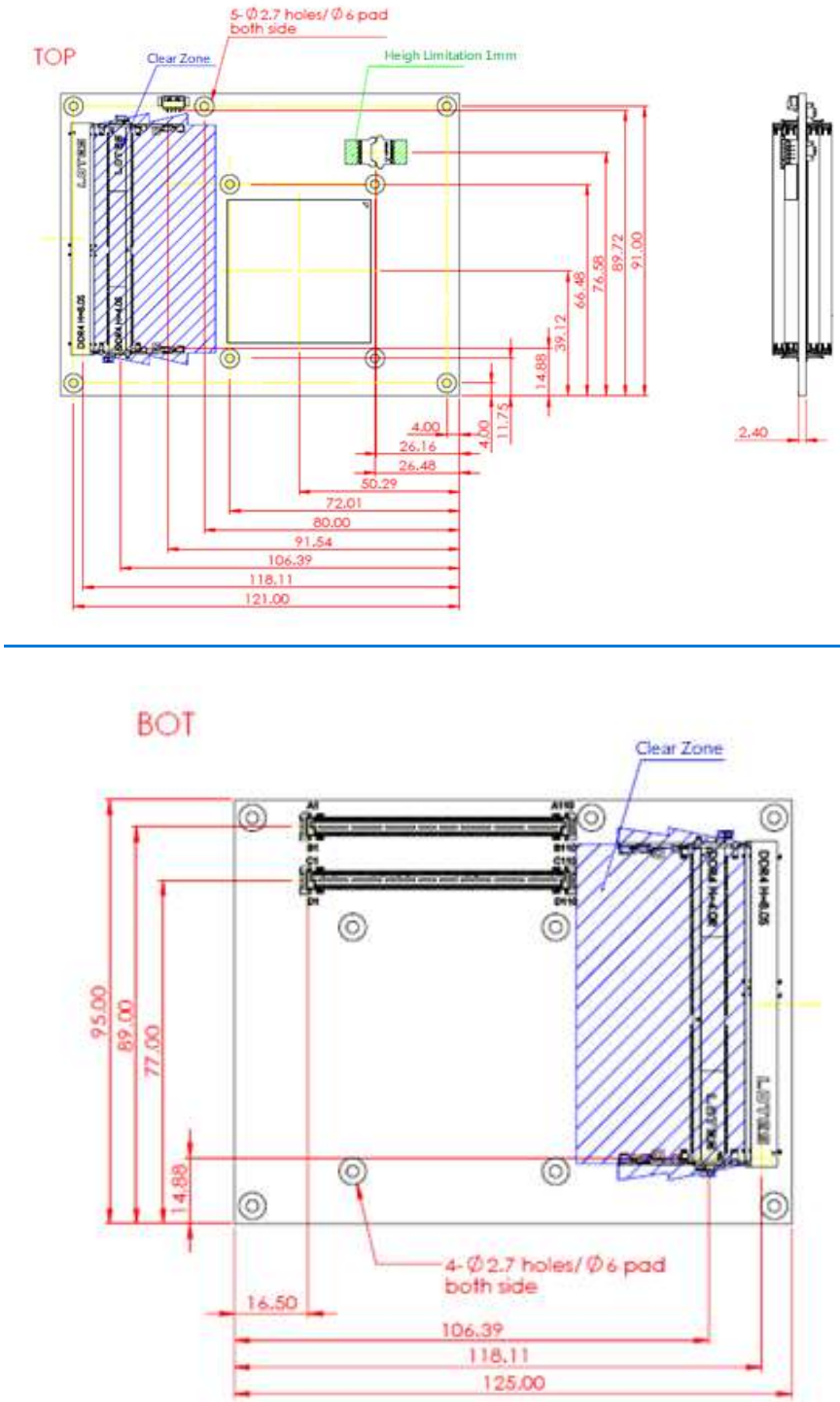

Figure 13 Mechanical – Top, Side and Bottom View

6 Pin out

PCOM-B705GT AB & CD row connectors PIN OUT

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A1	GND	GND(FIXED)	-	-	-	-	-
A2	I210_MDI3_N	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A3	I210_MDI3_P	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A4	I210_100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A5	I210_1G#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A6	I210_MDI2_N	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A7	I210_MDI2_P	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A8	I210_LINK#	Gigabit Ethernet Controller 0 link indicator, active	OD	CMOS	3.3V Suspend / 3.3V	-	-

		low.					
A9	I210_MDI1_N	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A10	I210_MDI1_P	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A11	GND	GND(FIXED)	-	-	-	-	-
A12	I210_MDI0_N	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A13	I210_MDI0_P	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A14	GBE_CTREF_CN	Reference voltage for Carrier Board Ethernet channel 0 magnetic center tap.	-	-	GND min 3.3V max	NC	-
A15	KBC_SLPS3#	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.	O	CMOS	3.3V Suspend / 3.3V	Module PD 470 ohm	-
A16	SATA_HSIO17_TXP17	Serial ATA or SAS	O	SATA	AC	-	-

		Channel 0 transmit differential pair.			coupled on Module		
A17	SATA_HSIO17_TXN17	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A18	KBC_SLPS45#	Indicates system is in Suspend to Disk state. Active low output.	O	CMOS	3.3V Suspend / 3.3V	-	-
A19	SATA_HSIO17_RXP17	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A20	SATA_HSIO17_RXN17	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A21	GND	GND(FIXED)	-	-	-	-	-
A22	PCIE_HSIO15_TXP15	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A23	PCIE_HSIO15_TXN15	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A24	KBC_SLPS45#	Indicates system is in Soft Off state.	O	CMOS	3.3V Suspend / 3.3V	-	-
A25	PCIE_HSIO14_TXP14	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A26	PCIE_HSIO14_TXN14	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

A27	BATLOW_N	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	I	CMOS	3.3V Suspend / 3.3V	Module PU 10K ohm to 3.3V	-
A28	COMe_SATA_LED#	SATA activity indicator, active low.	I/O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-
A29	RSVD	Reserved Pin	-	-	-	NC	-
A30	RSVD	Reserved Pin	-	-	-	NC	-
A31	GND	GND(FIXED)	-	-	-	-	-
A32	IPMB_CLK	Clock I/O line for the multi-master IPMB port	I/O	CMOS	3.3V / 3.3V	Module PU 4.7K ohm to 3.3V	For COM.0 Rev 3.1
A33	IPMB_DAT	Data I/O line for the multi-master IPMB port	I/O	CMOS	3.3V / 3.3V	Module PU 4.7K ohm to 3.3V	For COM.0 Rev 3.1
A34	BIOS_DIS0#	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low. Shared pin with ESPI_SAFS	I	CMOS	NA	-	-
A35	SoC_THERMTRIP#	Active low output indicating that the CPU has entered thermal shutdown	O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-
A36	PCIE_HSIO13_TXP13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on	-	-

					Module		
A37	PCIE_HSIO13_TXN13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A38	GND	GND	-	-	-	-	-
A39	PCIE_HSIO12_TXP12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A40	PCIE_HSIO12_TXN12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A41	GND	GND(FIXED)	-	-	-	-	-
A42	SOC_USB2_DN2	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A43	SOC_USB2_DP2	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A44	COMe_USB_OC#	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. Do not pull this line high on the Carrier Board	I	CMOS	3.3V Suspend / 3.3V	Go through diode PU 10K to 3.3V	-
A45	SOC_USB2_DN0	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall	I/O	USB	3.3V Suspend / 3.3V	-	-

		be host ports.					
A46	SOC_USB2_DP0	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A47	+V3P3_RTC	Real-time clock circuit-power input. Nominally +3.0V.	-	PWR	-	-	-
A48	RSMRST_OUT#	USB devices that are to be powered in the S5 / S4 / S3 Suspend states should not have their 5V VBUS power enabled before RSMRST_OUT# transitions to the hi state.	O CMOS	USB	3.3V Suspend / 3.3V	-	For COM.0 Rev 3.1
A49	GBE0_SDP	Gigabit Ethernet Controller 0 Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 4.3.4 for details.	I/O	CMOS	3.3V Suspend / 3.3V	-	-
A50	ESPI_ALERT1#_SIRQ	LPC serial interrupt / Shared pin with ESPI_CS1#	I/O	CMOS	3.3V / 3.3V	Module PU 1K ohm to 3.3V	-
A51	GND	GND(FIXED)	-	-	-	-	-
A52	PCIE_HSIO5_TXP5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

A53	PCIE_HSIO5_TXN5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A54	EC_GPI0	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	Module PU 10k ohm to 3.3V	-
A55	PCIE_HSIO4_TXP4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A56	PCIE_HSIO4_TXN4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A57	GND	GND	-	-	-	-	-
A58	PCIE_HSIO3_TXP3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A59	PCIE_HSIO3_TXN3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A60	GND	GND(FIXED)	-	-	-	-	-
A61	PCIE_HSIO2_TXP2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A62	PCIE_HSIO2_TXN2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A63	EC_GPI1	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	Module PU 4.7k ohm to 3.3V	-
A64	PCIE_HSIO1_TXP1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on	-	-

					Module		
A65	PCIE_HSIO1_TXN1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A66	GND	GND	-	-	-	-	-
A67	EC_GPI2	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	Module PU 4.7k ohm to 3.3V	-
A68	PCIE_HSIO0_TXP0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A69	PCIE_HSIO0_TXN0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A70	GND	GND(FIXED)	-	-	-	-	-
A71	PCIE_HSIO8_TXP8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A72	PCIE_HSIO8_TXN8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A73	GND	GND	-	-	-	-	-
A74	PCIE_HSIO9_TXP9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A75	PCIE_HSIO9_TXN9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A76	GND	GND	-	-	-	-	-
A77	PCIE_HSIO10_TXP10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

A78	PCIE_HSIO10_TXN10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A79	GND	GND	-	-	-	-	-
A80	GND	GND(FIXED)	-	-	-	-	-
A81	PCIE_HSIO11_TXP11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A82	PCIE_HSIO11_TXN11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A83	GND	GND	-	-	-	-	-
A84	LAN_NCSI_TXEN	NCSI Transmit Enable (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	Module PD 10k ohm	-
A85	EC_GPI3	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	Module PU 4.7k ohm to 3.3V	-
A86	RSVD	Reserved Pin	-	-	-	NC	-
A87	GND	GND	-	-	-	-	-
A88	COMe_PCIe_GEN3_CLKP	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A89	COMe_PCIe_GEN3_CLKN	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A90	GND	GND(FIXED)	-	-	-	-	-

A91	SPI_PWR_CN	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O	-	3.3V Suspend / 3.3V	Through 0 ohm PU to 3.3V	-
A92	COME_SPI_MISO	Data in to Module from Carrier SPI	I	CMOS	3.3V Suspend / 3.3V	-	-
A93	EC_GPO0	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
A94	COME_SPI_CLK	Clock from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A95	COME_SPI_MOSI	Data out from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A96	TPM_PP	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I	CMOS	3.3V / 3.3V	Module PD 4.7k ohm	-

A97	TYPE10#	Dual use pin. Indicates to the Carrier Board that a Type 10 module is installed. Indicates to the Carrier that a Rev 1.0/2.0 module is installed	-	-	-	NC	
A98	SER0_TX	General purpose serial port transmitter	O	CMOS	3.3V / 12V	Module PD 4.7K	-
A99	SER0_RX	General purpose serial port receiver	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-
A100	GND	GND(FIXED)	-	-	-	-	-
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O	CMOS	3.3V / 12V	Module PD 4.7K	-
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I	CMOS	3.3V / 12V	Go through diode PU 47K to 3.3V	-
A103	LID#_CN	LID button. Low active signal used by the ACPI operating system for a LID switch.	I	CMOS	3.3V Suspend / 12V	Go through diode PU 47K to 3.3V	-
A104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-

A107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A110	GND	GND(FIXED)	-	-	-	-	-
B1	GND	GND(FIXED)	-	-	-	-	-
B2	I210_ACT#	Gigabit Ethernet Controller 1 activity indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
B3	ESPI_CS1#_FRAME#	LPC frame indicates the start of an LPC cycle / Shared pin with ESPI_CS0#	O	CMOS	3.3V / 3.3V	-	-
B4	ESPI_IO0_LAD0	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-
B5	ESPI_IO1_BMC	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-
B6	ESPI_IO2_LAD2	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-
B7	ESPI_IO3_LAD3	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	Module PU 10K ohm to 3.3V	-

B8	ESPI_ALERT1#_SIRQ	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	Module PU 1K ohm to 3.3V	-
B9	ESPI_ALERT#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	Module PU 1K ohm to 3.3V	-
B10	ESPI_CLK_COME	LPC clock output - 33MHz nominal / Shared pin with ESPI_Clock	O	CMOS	3.3V / 3.3V	-	-
B11	GND	GND(FIXED)	-	-	-	-	-
B12	COME_PWRBTN#	Power button to bring system out of S5 (soft off), active on falling edge.	I	CMOS	3.3V Suspend / 3.3V	Module PU 10k ohm to 3.3V	-
B13	SoC_SMB_SCL	System Management Bus bidirectional clock line.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 10k ohm to 3.3V	-
B14	SoC_SMB_SDA	System Management Bus bidirectional data line.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 10k ohm to 3.3V	-
B15	SoC_SMB_ALERT#	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I	CMOS	3.3V Suspend / 3.3V	-	-
B16	SATA_HSIO18_TXP18	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B17	SATA_HSIO18_TXN18	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on	-	-

					Module		
B18	ESPI_RESET#_SUSSTATE#	Indicates imminent suspend operation; used to notify LPC devices / Shared pin with ESPI_RESET	O	CMOS	3.3V Suspend / 3.3V	-	-
B19	SATA_HSIO18_RXP18	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B20	SATA_HSIO18_RXN18	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B21	GND	GND(FIXED)	-	-	-	-	-
B22	PCIE_HSIO15_RXP15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B23	PCIE_HSIO15_RXN15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B24	COME_PWROK	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or other configurable devices time to be programmed.	I	CMOS	3.3V / 3.3V	-	-
B25	PCIE_HSIO14_RXP14	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off	-	-

					Module		
B26	PCIE_HSIO14_RXN14	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B27	WDTO#	Output indicating that a watchdog time-out event has occurred.	O	CMOS	3.3V / 3.3V	-	-
B28	GND	GND(FIXED)		-	-	-	-
B29	COME_PCIe_GEN4_CLKP	Second reference clock output for higher speed PCI Express implementation on Lanes 16 to 31, for Type 7 implementations only	O	PCIE	PCIE	-	For COM.0 Rev 3.1
B30	COME_PCIe_GEN4_CLKN	Second reference clock output for higher speed PCI Express implementation on Lanes 16 to 31, for Type 7 implementations only,	O	PCIE	PCIE	-	For COM.0 Rev 3.1
B31	GND	GND(FIXED)	-	-	-	-	-
B32	SPKR	Output for audio enunciator	O	CMOS	3.3V / 3.3V	-	-
B33	SMB1_CLK_COMe	General purpose I2C port clock output	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 4.7k ohm to 3.3V	-
B34	SMB1_DATA_COMe	General purpose I2C port data I/O line	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 4.7k ohm to 3.3V	-
B35	COMe_THRM#	Input from off-Module temp	I	CMOS	3.3V / 3.3V	Module PU 10k	-

		sensor indicating an over-temp situation				ohm to 3.3V	
B36	PCIE_HSIO13_RXP13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B37	PCIE_HSIO13_RXN13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B38	GND	GND	-	-	-	-	-
B39	PCIE_HSIO12_RXP12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B40	PCIE_HSIO12_RXN12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B41	GND	GND(FIXED)	-	-	-	-	-
B42	SOC_USB2_DN3	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B43	SOC_USB2_DP3	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B44	COMe_USB_OC#	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. Do not pull this line high on the	I	CMOS	3.3V Suspend / 3.3V	-	-

		Carrier Board					
B45	SOC_USB2_DN1	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B46	SOC_USB2_DP1	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B47	COME_ESPI_EN#	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If pulled down by the Carrier LPC mode is selected. If pulled up or left floating, eSPI is selected if available. This signal is pulled up on the Module. This signal is a “don’t care” for Modules that do not support eSPI	I	CMOS	NA	Module PU 10K ohm to 3.3V	-
B48	USB0_HOST_PRSNT	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.	I	CMOS	3.3V Suspend/ 3.3V	NC	-

B49	COME_RSTBTN#	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used	I	CMOS	3.3V Suspend / 3.3V	Module PU 2.7k ohm to 3.3V	-
B50	PLTRST2#	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12Vpower input that falls below the minimum specification, a watchdog timeout, or maybe initiated by the Module software.	O	CMOS	3.3V Suspend / 3.3V	-	-
B51	GND	GND(FIXED)	-	-	-	-	-
B52	PCIE_HSIO5_RXP5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B53	PCIE_HSIO5_RXN5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

B54	EC_GPO1	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B55	PCIE_HSIO4_RXP4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B56	PCIE_HSIO4_RXN4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B57	EC_GPO2	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B58	PCIE_HSIO3_RXP3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B59	PCIE_HSIO3_RXN3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B60	GND	GND(FIXED)	-	-	-	-	-
B61	PCIE_HSIO2_RXP2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B62	PCIE_HSIO2_RXN2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B63	EC_GPO3	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B64	PCIE_HSIO1_RXP1	PCI Express	I	PCIE	AC	-	-

		Differential Receive Pairs			coupled off Module		
B65	PCIE_HSIO1_RXN1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B66	WAKE0#_CN	PCI Express wake up signal.	I	CMOS	3.3V Suspend / 3.3V	-	-
B67	WAKE1#_CN	General purpose wake up signal. Maybe used to implement wake-up on PS2 keyboard or mouse activity	I	CMOS	3.3V Suspend / 3.3V	-	-
B68	PCIE_HSIO0_RXP0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B69	PCIE_HSIO0_RXN0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B70	GND	GND(FIXED)	-	-	-	-	-
B71	PCIE_HSIO8_RXP8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B72	PCIE_HSIO8_RXN8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B73	GND	GND	-	-	-	-	-
B74	PCIE_HSIO9_RXP9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B75	PCIE_HSIO9_RXN9	PCI Express Differential	I	PCIE	AC coupled	-	-

		Receive Pairs			off Module		
B76	GND	GND	-	-	-	-	-
B77	PCIE_HSIO10_RXP10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B78	PCIE_HSIO10_RXN10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B79	COME_B79	GND	-	-	-	Through 0 ohm to GND	-
B80	GND	GND(FIXED)	-	-	-	-	-
B81	PCIE_HSIO11_RXP11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B82	PCIE_HSIO11_RXN11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B83	GND	GND	-	-	-	-	-
B84	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B85	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B86	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B87	+5VSB	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B88	BIOS_DIS1#	Selection straps to determine the BIOS boot device. The Carrier should	I	CMOS	NA	Module PU 10k ohm to 3.3V	-

		only float these or pull them low / Shared pin with ESPI_BBS					
B89	NCSI_RX_ER_CN	NC-SI Receive error	O	-	3.3V Suspend / 3.3V	NC	-
B90	GND	GND(FIXED)	-	-	-	-	-
B91	LAN_NCSI_CLKIN	NC-SI Clock reference for receive, transmit, and control interface. (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	Module PD 10K	-
B92	LAN_NCSI_RXD1	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Module PU 10K to 3.3V	-
B93	LAN_NCSI_RXD0	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	Module PU 10K to 3.3V	-
B94	LAN_NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O	-	3.3V Suspend / 3.3V	Module PD 10K	-
B95	LAN_NCSI_TXD1	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	Module PU 10K to 3.3V	-
B96	LAN_NCSI_TXD0	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	Module PU 10K to 3.3V	-

B97	COME_SPI_CS0#	Chip select for Carrier Board SPI - maybe sourced from chipset SPI0 or SPI1	O	CMOS	3.3V Suspend / 3.3V	-	-
B98	NCSI_ARB_IN	NC-SI hardware arbitration input.	I	-	3.3V Suspend / 3.3V	Module PU 10K to 3.3V	-
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output.	O	-	3.3V Suspend / 3.3V	-	-
B100	GND	GND(FIXED)	-	-	-	-	-
B101	FAN_PWMOUT_CN	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM	O	CMOS	3.3V / 12V	Go through diode then PU 10K ohm to 3.3V	-
B102	FAN_TACHIN_CN	Fan tachometer input for a fan with a two pulse output.	I	CMOS	3.3V / 12V	Go through diode then PU 47K ohm to 3.3V	-
B103	SLEEP#_CN	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I	CMOS	3.3V Suspend / 12V	Go through diode then PU 47K ohm to 3.3V	-
B104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B106	+V12_A	Primary power input: +12V	-	PWR	+12V	-	-

		nominal.					
B107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B110	GND	GND(FIXED)	-	-	-	-	-
C1	GND	GND(FIXED)	-	-	-	-	-
C2	GND	GND	-	-	-	-	-
C3	USB3_HSIO20_RXN0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C4	USB3_HSIO20_RXP0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C5	GND	GND	-	-	-	-	-
C6	USB3_HSIO21_RXN1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C7	USB3_HSIO21_RXP1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C8	GND	GND	-	-	-	-	-
C9	USB3_HSIO22_RXN2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-

C10	USB3_HSIO22_RXP2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C11	GND					-	-
C12	USB3_HSIO23_RXN3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C13	USB3_HSIO23_RXP3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C14	GND	GND	-	-	-	-	-
C15	10PHY_MDC3_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	NC	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	NC	-
C16	10PHY_MDC2_CN	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an	O	-	3.3V Suspend / 3.3V	NC	-

		external PHY.					
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	NC	-
C17	10G_PORT2_SDP	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	Module PU 10K ohm to 3.3V	-
C18	GND	GND	-	-	-	-	-
C19	PCIE_HSIO6_RXP6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C20	PCIE_HSIO6_RXN6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C21	GND	GND(FIXED)	-	-	-	-	-
C22	PCIE_HSIO7_RXP7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C23	PCIE_HSIO7_RXN7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C24	10G_INT2_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-
C25	GND	GND	-	-	-	-	-

C26	COME_ETH0_KR_RXDP3	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C27	COME_ETH0_KR_RXDN3	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C28	GND	GND	-	-	-	-	-
C29	COME_ETH0_KR_RXDP2	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C30	COME_ETH0_KR_RXDN2	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C31	GND	GND(FIXED)	-	-	-	-	-
C32	NAC_I2C_SDA3	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	Module PU 2.2K ohm to 3.3V	-
C33	NAC_I2C_SDA2	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	Module PU 2.2K ohm to 3.3V	-

C34	10GPHY_RST23_CN	Output signal that resets an optical PHY on port 2 and port3 (Not used with copper PHY)	O	-	3.3V Suspend / 3.3V	NC	-
C35	CEI_RST#	Active low reset output from Module to Carrier based I/O expander	O	-	3.3V Suspend / 3.3V		For COM.0 Rev 3.1
C36	10G_LED_SDA	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.	I/O	OD	3.3V Suspend / 3.3V	Module PU 2.2K ohm to 3.3V	-
C37	10G_LED_SCL	I2C Clock, of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs	I/O	OD	3.3V Suspend / 3.3V	Module PU 2.2K ohm to 3.3V	-
C38	NAC_I2C_SDA1	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	Module PU 2.2K ohm to 3.3V	-
C39	CEI_SDA	I2C data – for SFP setup, serialized status LEDs and miscellaneous serialized signals	I/O	OD	3.3V Suspend / 3.3V	NC	For COM.0 Rev 3.1

C40	10G_PORT0_SDP	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	-	-
C41	GND	GND(FIXED)	-	-	-	-	-
C42	COME_ETH0_KR_RXDP1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C43	COME_ETH0_KR_RXDN1	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C44	GND	GND	-	-	-	-	-
C45	10PHY_MDC1_CN	MDIO clock - for PHY setup	O	-	3.3V Suspend / 3.3V	NC	-
C46	CEI_MDC	MDIO clock - for PHY setup	O	-	3.3V Suspend / 3.3V	Module PU 1k ohm to 3.3V	For COM.0 Rev 3.1
C47	CEI_INT#	Active low interrupt input to Module from Carrier based I2C I/O expander	I	-	3.3V Suspend / 3.3V	Module PU 10k ohm to 3.3V	For COM.0 Rev 3.1
C48	GND	GND	-	-	-	-	-
C49	COME_ETH0_KR_RXDP0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C50	COME_ETH0_KR_RXDN0	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C51	GND	GND(FIXED)	-	-	-	-	-
C52	COME_SoC_PCIE4_RXDP0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C53	COME_SoC_PCIE4_RXDN0	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C54	GND	GND(FIXED)	-	-	-		-
C55	COME_SoC_PCIE4_RXDP1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C56	COME_SoC_PCIE4_RXDN1	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C57	TYPE1	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	NC	-
C58	COME_SoC_PCIE4_RXDP2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C59	COME_SoC_PCIE4_RXDN2	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C60	GND	GND(FIXED)	-	-	-	-	-
C61	COME_SoC_PCIE4_RXDP3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C62	COME_SoC_PCIE4_RXDN3	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C63	RSVD	Reserved Pin	-	-	-	Connect to GND	-
C64	RSVD	Reserved Pin	-	-	-	Connect	-

						to GND	
C65	COME_SoC_PCIE4_RXDP4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C66	COME_SoC_PCIE4_RXDN4	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C67	RAPID_SUTDN	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for a	I	CMOS	5.0V Suspend/ 5.0V	Module PD 150 ohm	-
C68	COME_SoC_PCIE4_RXDP5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C69	COME_SoC_PCIE4_RXDN5	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C70	GND	GND(FIXED)	-	-	-	-	-
C71	COME_SoC_PCIE4_RXDP6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C72	COME_SoC_PCIE4_RXDN6	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C73	GND	GND	-	-	-	-	-
C74	COME_SoC_PCIE4_RXDP7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C75	COME_SoC_PCIE4_RXDN7	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C76	GND	GND	-	-	-	-	-
C77	GND	GND	-	-	-	-	-
C78	COME_SoC_PCIE4_RXDP8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C79	COME_SoC_PCIE4_RXDN8	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C80	GND	GND(FIXED)	-	-	-	-	-
C81	COME_SoC_PCIE4_RXDP9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C82	COME_SoC_PCIE4_RXDN9	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C83	GND	GND(FIXED)	-	-	-	-	-
C84	GND	GND	-	-	-	-	-
C85	COME_SoC_PCIE4_RXDP10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C86	COME_SoC_PCIE4_RXDN10	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C87	GND	GND	-	-	-	-	-
C88	COME_SoC_PCIE4_RXDP11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C89	COME_SoC_PCIE4_RXDN11	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C90	GND	GND(FIXED)	-	-	-	-	-
C91	COME_SoC_PCIE4_RXDP12	PCI Express Differential	I	PCIE	AC coupled	-	-

		Receive Pairs			off Module		
C92	COME_SoC_PCIE4_RXDN12	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C93	GND	GND	-	-	-	-	-
C94	COME_SoC_PCIE4_RXDP13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C95	COME_SoC_PCIE4_RXDN13	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C96	GND	GND	-	-	-	-	-
C97	RSVD	Reserved Pin	-	-	-	Connect to GND	-
C98	COME_SoC_PCIE4_RXDP14	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C99	COME_SoC_PCIE4_RXDN14	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C100	GND	GND(FIXED)	-	-	-	-	-
C101	COME_SoC_PCIE4_RXDP15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C102	COME_SoC_PCIE4_RXDN15	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C103	GND	GND	-	-	-	-	-
C104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C105	+V12_A	Primary power input: +12V	-	PWR	+12V	-	-

		nominal.					
C106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C110	GND	GND(FIXED)	-	-	-	-	-
D1	GND	GND(FIXED)	-	-	-	-	-
D2	GND	GND	-	-	-	-	-
D3	USB3_HSIO20_TXN0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D4	USB3_HSIO20_TXP0	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D5	GND	GND	-	-	-	-	-
D6	USB3_HSIO21_TXN1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D7	USB3_HSIO21_TXP1	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D8	GND	GND	-	-	-	-	-
D9	USB3_HSIO22_TXN2	Additional transmit signal differential pairs for the	O	PCIE	AC coupled on	-	-

		SuperSpeed USB data path.			Module		
D10	USB3_HSIO22_TXP2	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D11	GND	GND(FIXED)	-	-	-	-	-
D12	USB3_HSIO23_TXN3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D13	USB3_HSIO23_TXP3	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D14	GND	GND	-	-	-	-	-
D15	10PHY_MDA3_CN	MDIO data – for PHY setup	O	-	3.3V Suspend / 3.3V	NC	-
D16	10PHY_MDA2_CN	MDIO data – for PHY setup	O	-	3.3V Suspend / 3.3V	NC	-
D17	10G_PORT3_SDP	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	Module PU 10k ohm to 3.3V	-
D18	GND	GND	-	-	-	-	-
D19	PCIE_HSIO6_TXP6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D20	PCIE_HSIO6_TXN6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D21	GND(FIXED)	GND(FIXED)	-	-	-	-	-

D22	PCIE_HSIO7_TXP7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D23	PCIE_HSIO7_TXN7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D24	10G_INT3_CN	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	Module PU 2.2k ohm to 3.3V	-
D25	GND	GND	-	-	-	-	-
D26	ETH0_COME_KR_TXDP3	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D27	ETH0_COME_KR_TXDN3	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D28	GND	GND	-	-	-	-	-
D29	ETH0_COME_KR_TXDP2	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D30	ETH0_COME_KR_TXDN2	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled at receiver	-	-
D31	GND	GND(FIXED)	-	-	-	-	-
D32	NAC_I2C_SCL3	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-

		external Optical SFP Module.					
D33	NAC_I2C_SCL2	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O	CMOS	3.3V Suspend / 3.3V	Module PU 2.2kohm to 3.3V	-
D34	10GPHY_SEL23_CN	PHY mode select pin: If high Phy2 and Phy3 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode, this pin should be left not connected on the Carrier. For I2C mode pull down with 1K on Carrier	I	-	3.3V Suspend / 3.3V	Module PU 10k ohm to 3.3V	-
D35	CEI_PRSNT#	Input signal from Carrier indicating presence of CEI compliant hardware on the Carrier	I	-	3.3V Suspend / 3.3V	Module PU 10kohm to 3.3V	For COM.0 Rev 3.1
D36	RSVD	RSVD	-	-	-	NC	-
D37	RSVD	RSVD	-	-	-	NC	-
D38	NAC_I2C_SCL1	I2C clock signal of the 2-wire management interface used by	I/O	OD	3.3V Suspend / 3.3V	Module PU 2.2kohm to	-

		the 10GbE controller to access the management registers of an external Optical SFP Module				3.3V	
D39	CEI_SCL	I2C clock for CEI I2C port	I/O	OD	3.3V Suspend / 3.3V	Module PU 10kohm to 3.3V	For COM.0 Rev. 3.1
D40	10G_PORT1_SDP	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	Module PU 10kohm to 3.3V	-
D41	GND	GND(FIXED)	-	-	-	-	-
D42	ETH0_COME_KR_TXDP1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D43	ETH0_COME_KR_TXDN1	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D44	GND	GND	-	-	-	-	-
D45	10PHY_MDA1_CN	MDIO data – for PHY setup	O	-	3.3V Suspend / 3.3V	NC	-
D46	CEI_MDIO	MDIO data – for PHY setup	I/O OD	-	3.3V Suspend / 3.3V	Module PU 1kohm to 3.3V	For COM.0 Rev. 3.1
D47	ETH_PHY_INT#	Second active low interrupt input to Module from Carrier based I2C I/O	I	-	3.3V Suspend / 3.3V	Module PU 20kohm to 3.3V	For COM.0 Rev. 3.1

		expander					
D48	GND	GND	-	-	-	-	-
D49	ETH0_COME_KR_TXDP0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D50	ETH0_COME_KR_TXDN0	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D51	GND	GND(FIXED)	-	-	-	-	-
D52	SoC_COME_PCIE4_TXDP0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D53	SoC_COME_PCIE4_TXDN0	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D54	RSVD	Reserved Pin	-	-	-	Connect to GND	-
D55	SoC_COME_PCIE4_TXDP1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D56	SoC_COME_PCIE4_TXDN1	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D57	GND	GND(FIXED)	-	-	-		-
D58	SoC_COME_PCIE4_TXDP2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D59	SoC_COME_PCIE4_TXDN2	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

D60	GND	GND(FIXED)	-	-	-	-	-
D61	SoC_COME_PCIE4_TXDP3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D62	SoC_COME_PCIE4_TXDN3	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D63	RSVD	Reserved Pin	-	-	-	Connect to GND	-
D64	RSVD	Reserved Pin	-	-	-	Connect to GND	-
D65	SoC_COME_PCIE4_TXDP4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D66	SoC_COME_PCIE4_TXDN4	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D67	GND	GND	-	-	-	-	-
D68	SoC_COME_PCIE4_TXDP5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D69	SoC_COME_PCIE4_TXDN5	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D70	GND	GND(FIXED)	-	-	-	-	-
D71	SoC_COME_PCIE4_TXDP6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D72	SoC_COME_PCIE4_TXDN6	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D73	GND	GND	-	-	-	-	-
D74	SoC_COME_PCIE4_TXDP7	PCI Express	O	PCIE	AC	-	-

		Differential Transmit Pairs			coupled on Module		
D75	SoC_COME_PCIE4_TXDN7	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D76	GND	GND	-	-	-	-	-
D77	RSVD	Reserved Pin	-	-	-	Connect to GND -	-
D78	SoC_COME_PCIE4_TXDP8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D79	SoC_COME_PCIE4_TXDN8	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D80	GND	GND(FIXED)	-	-	-	-	-
D81	SoC_COME_PCIE4_TXDP9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D82	SoC_COME_PCIE4_TXDN9	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D83	RSVD	Reserved Pin	-	-	-	Connect to GND	-
D84	GND	GND	-	-	-	-	-
D85	SoC_COME_PCIE4_TXDP10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D86	SoC_COME_PCIE4_TXDN10	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D87	GND	GND	-	-	-	-	-
D88	SoC_COME_PCIE4_TXDP11	PCI Express	O	PCIE	AC	-	-

		Differential Transmit Pairs			coupled on Module		
D89	SoC_COME_PCIE4_TXDN11	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D90	GND	GND(FIXED)	-	-	-	-	-
D91	SoC_COME_PCIE4_TXDP12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D92	SoC_COME_PCIE4_TXDN12	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D93	GND	GND	-	-	-	-	-
D94	SoC_COME_PCIE4_TXDP13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D95	SoC_COME_PCIE4_TXDN13	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D96	GND	GND	-	-	-	-	-
D97	RSVD	Reserved Pin	-	-	-	Connect to GND	-
D98	SoC_COME_PCIE4_TXDP14	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D99	SoC_COME_PCIE4_TXDN14	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D100	GND	GND(FIXED)	-	-	-	-	-
D101	SoC_COME_PCIE4_TXDP15	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

D102	SoC_COME_PCIE4_TXDN15	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D103	GND	GND	-	-	-	-	-
D104	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D105	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D106	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D107	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D108	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D109	+V12_A	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D110	GND	GND(FIXED)	-	-	-	-	-

Table 24 PCOM-B705GT AB & CD Row Connectors Pin Out

7 Industry Specifications

Low Pin Count Interface Specification, Revision 1.0 (LPC)
http://www.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0 http://www.usb.org/home
PCI Specification, Revision 2.3 https://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0 http://www.serialata.org/
PCI Express Base Specification, Revision 2.0 https://www.pcisig.com/specifications
PICMG® COM Express Module™ Base Specification http://www.picmg.org/
PICMG®COM Express Carrier Board Design Guide http://www.picmg.org/