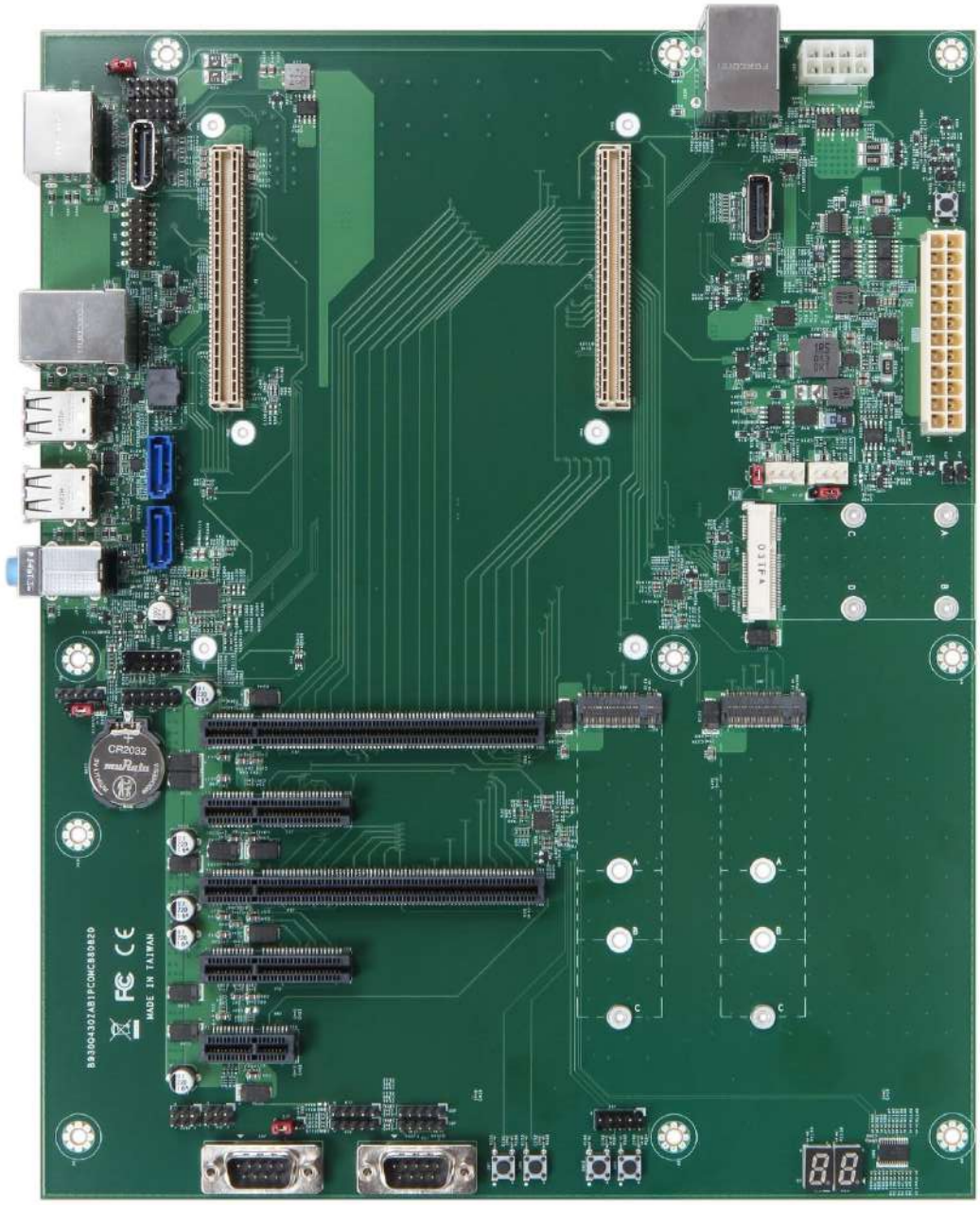

COM-HPC™
PCOM-C880
User's Guide R0.1

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Revision History

Rev.	Note	Date
R0.1	Preliminary release	2023 / 05 / 05

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Contents

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List of Tables

List of Figures

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1 COM-HPC Introduction

COM-HPC®(for “Computer on Module – High Performance Computing”) is a PICMG® sponsored open standard for a family of high performance computer modules targeting the embedded computer space. The embedded space differs from the commercial space with respect to features such as long-term availability, extended temperature operation, mechanical ruggedness, hardware and firmware that can be customized to the application, and Module vendor support to product developers. In the COM development model, the COMs are standard product offerings, and they are used with Carrier boards that are usually application specific, with additional features, connectors and geometries suited to the customer product at hand.

The COM-HPC® modules are available in following form factors:

- Size A - 95 mm x 120 mm
- Size B - 120 mm x 120 mm
- Size C - 160 mm x 120 mm
- Size D - 160 mm x 160 mm
- Size E - 200 mm x 160 mm

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1.1 PCOM-C880

Portwell PCOM-C880 support the COM-HPC client type module Sizes A, B, and C with ATX size form factor. This carrier board passed the most of Portwell evaluation testing. These functions include but are not limited to a rich complement of high speed interfaces such as DP display, PCIe, RJ45, USB 3.2, SATA. And also support several legacy I/O such as UART, GPIO, SMBUS, I2C.

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2 Block Diagram

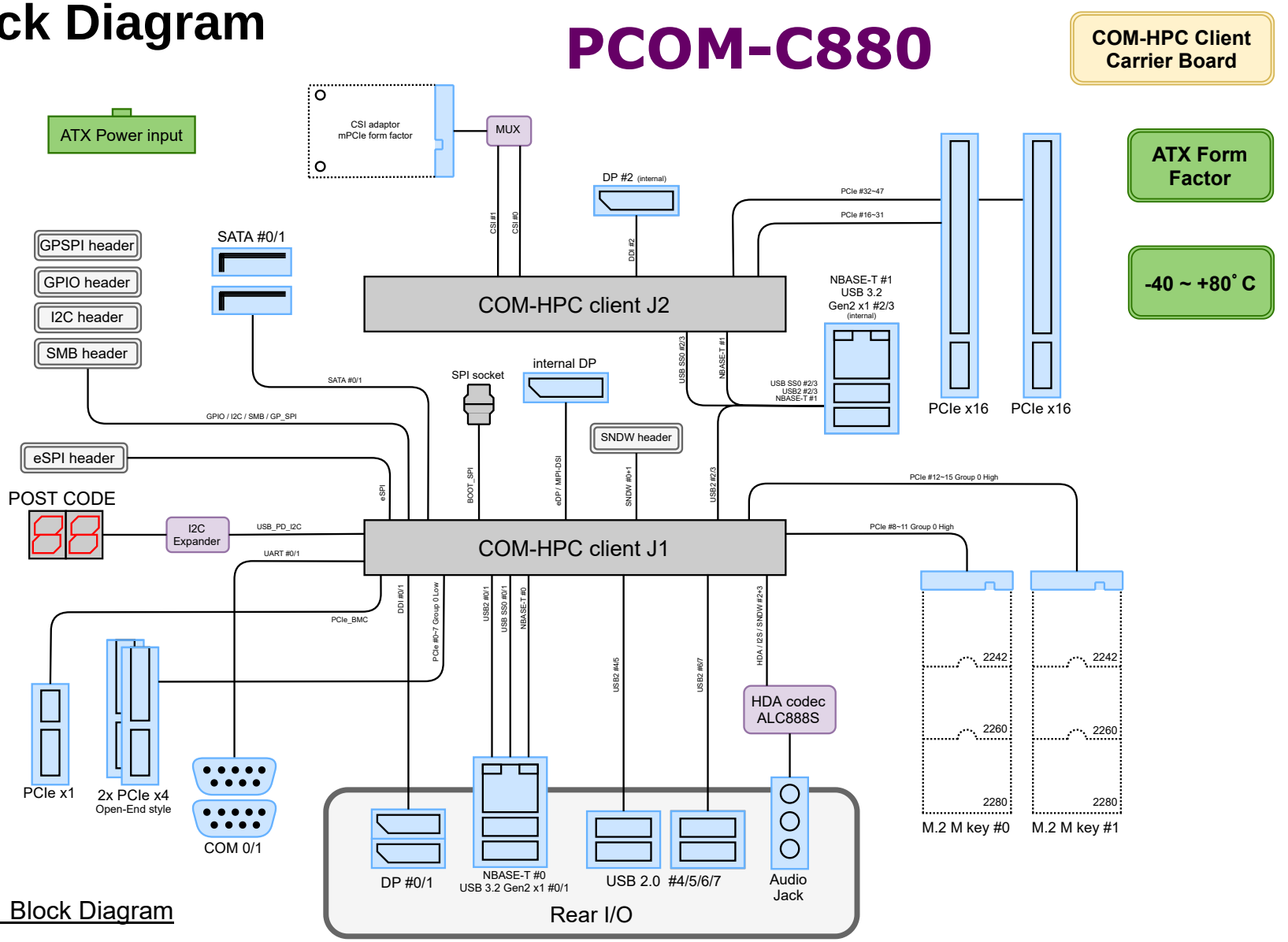

Figure 1 Block Diagram

3 Specifications

General	
Product	➢ PCOM-C880
Form Factor	➢ ATX Size (305 X 244mm)
Supported Module	➢ COM-HPC client, size A / B / C
General Function	➢ RTC battery ➢ Postcode display ➢ BIOS SPI Socket ➢ Power BTN / Reset BTN ➢ Lid BTN / Sleep BTN ➢ RapidShutdown BTN
Audio codec	➢ Realtek ALC888s

I/O Interface	
SATA	➢ 2 x SATA III
USB	➢ 4x USB 3.2 Gen2 port ➢ 4x USB 2.0 port
Ethernet	➢ 2x 2.5Gbe RJ45
PCI Express	➢ 2x PCIe x16 ➢ 2x PCIe x4 ➢ 2x M.2 M key ➢ 1x PCIe x1 (Route to PCIe_BMC lane)

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Display	➢ 3x DP (via module DDI signal) ➢ 1x DP (via module eDP signal, route to standard DP for evaluation purpose)
Legacy I/O	➢ GPIO ➢ I2C ➢ SMBus ➢ UART ➢ GP SPI
Others	➢ Audio jack ➢ 2x FAN (1x support PWM control) ➢ MIPI-CSI (for signal measurement purpose)

Table 1 PCOM-C880 SPEC

3.1 Mechanical Dimensions

- Top Side Dimension

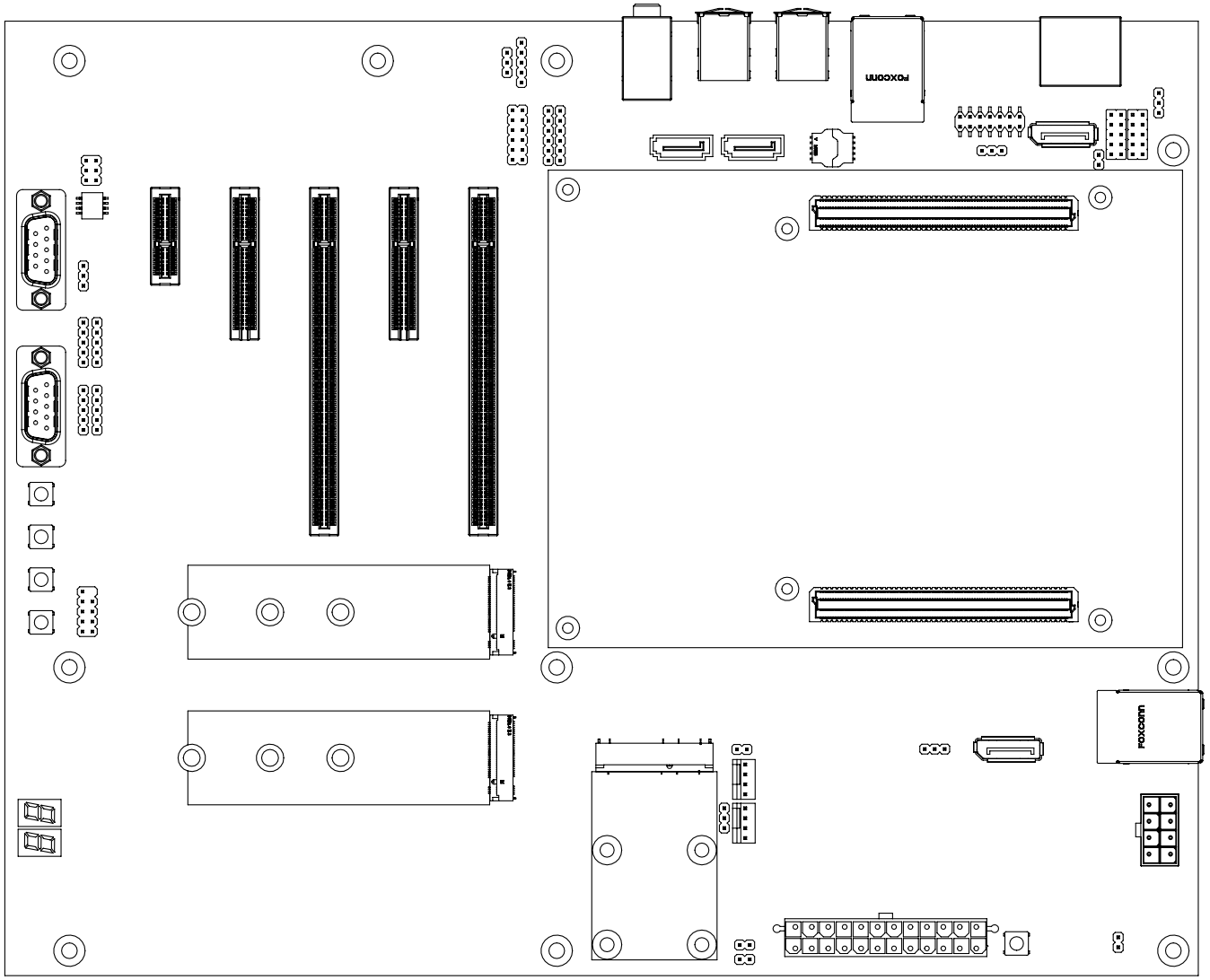

Figure 2
Mechanical Dimension - Top

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- Bottom Side Dimension

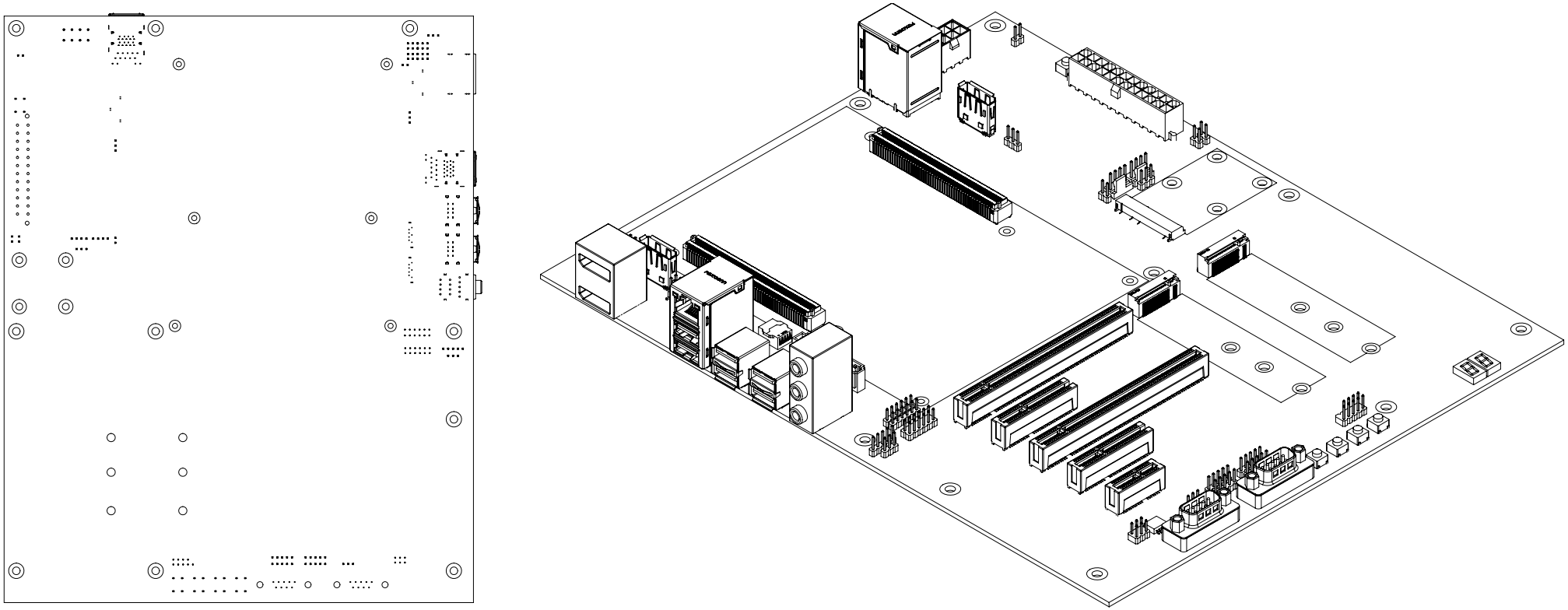

Figure 3 Mechanical Dimension - Bottom

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3.2 Environmental Specifications

Storage Temperature	-40°C ~ 85°C
Operation Temperature	-40°C ~ 85°C
Storage Humidity	0% ~ 95%
Operation Humidity	0% ~ 95%

Table 2 Environmental Specifications

3.3 Ordering Guide

- **Module**

Product	Ordering P/N
PCOM-C880	AB1-3L34Z

Table 3 Ordering Guide - PCOM-C880

- **Accessory**

Accessory	Ordering P/N	Remark

Table 4 Ordering Guide - Accessory

4 Pin out Tables

- **Connector J1**

J1							
Pin	RAW A	Pin	RAW B	Pin	RAW C	Pin	PAW D
A1	+V12P0S	B1	+V12P0S	C1	+V12P0S	D1	+V12P0S
A2	+V12P0S	B2	EXT_PWRBTN_N	C2	RSTBTN_N	D2	+V12P0S
A3	+V12P0S	B3	+V12P0S	C3	+V12P0S	D3	+V12P0S
A4	+V12P0S	B4	EXT_PWRBTN_N	C4	CARRIER_HOT_N	D4	+V12P0S
A5	+V12P0S	B5	+V12P0S	C5	+V12P0S	D5	+V12P0S
A6	+V12P0S	B6	TAMPER_N	C6	VIN_PWROK	D6	+V12P0S
A7	+V12P0S	B7	+V12P0S	C7	+V12P0S	D7	+V12P0S
A8	+V12P0S	B8	KBC_SLP_S3_N	C8	KBC_SLP_S4_N	D8	+V12P0S
A9	+V12P0S	B9	+V12P0S	C9	+V12P0S	D9	+V12P0S
A10	GND	B10	WDT_STROBE_N	C10	GND	D10	PCIE_WAKE_CN_N
A11	BATLOW_N	B11	EC_WDT_CN	C11	KBC_SYS_FANOUT1	D11	N/C
A12	PLTRST_N	B12	GND	C12	KBC_SYS_FANIN1	D12	GND
A13	GND	B13	USB2_P6_DN	C13	GND	D13	USB2_P2_DN
A14	USB2_P8_DN	B14	USB2_P6_DP	C14	USB2_P4_DN	D14	USB2_P2_DP
A15	USB2_P8_DP	B15	GND	C15	USB2_P4_DP	D15	GND
A16	GND	B16	USB2_P5_DN	C16	GND	D16	USB2_P1_DN
A17	USB2_P7_DN	B17	USB2_P5_DP	C17	USB2_P3_DN	D17	USB2_P1_DP
A18	USB2_P7_DP	B18	GND	C18	USB2_P3_DP	D18	GND

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A19	GND	B19	HDA_SYNC	C19	GND	D19	DDI1_CTRLDATA_AUXN
A20	DDI2_CTRLDATA_AUXN	B20	HDA_SDOUT	C20	DMIC1_CLK	D20	DDI1_CTRLCLK_AUXP
A21	DDI2_CTRLCLK_AUXP	B21	HDA_RST_N	C21	DMIC1_DATA	D21	GND
A22	GND	B22	HDA_SDIN0	C22	GND	D22	DDI1_TX0_DN
A23	DDI2_TX0_DN	B23	HDA_BITCLK	C23	SNDW0_CLK	D23	DDI1_TX0_DP
A24	DDI2_TX0_DP	B24	+5VSB	C24	SNDW0_DATA	D24	GND
A25	GND	B25	USB_OC3_N	C25	GND	D25	DDI1_TX1_DN
A26	DDI2_TX1_DN	B26	USB_OC2_N	C26	DDI1_AUX_SEL	D26	DDI1_TX1_DP
A27	DDI2_TX1_DP	B27	USB_OC1_N	C27	DDI2_AUX_SEL	D27	GND
A28	GND	B28	USB_OC0_N	C28	DDI1_HPD	D28	DDI1_TX2_DN
A29	DDI2_TX2_DN	B29	N/C	C29	DDI2_HPD	D29	DDI1_TX2_DP
A30	DDI2_TX2_DP	B30	N/C	C30	EDP_HPD	D30	GND
A31	GND	B31	N/C	C31	EDP_VDDEN	D31	DDI1_TX3_DN
A32	DDI2_TX3_DN	B32	N/C	C32	EDP_BKLTEN	D32	DDI1_TX3_DP
A33	DDI2_TX3_DP	B33	N/C	C33	EDP_BKLTCTL	D33	GND
A34	GND	B34	N/C	C34	GND	D34	PM_ACPRESENT
A35	eDP_AUXN	B35	USB_PD_I2C_CLK	C35	N/C	D35	N/C
A36	eDP_AUXP	B36	USB_PD_I2C_DATA	C36	N/C	D36	GND
A37	GND	B37	N/C	C37	GND	D37	USB3_TX2_DN
A38	eDP_TX0_DN	B38	N/C	C38	USB3_RX2_DN	D38	USB3_TX2_DP
A39	eDP_TX0_DP	B39	N/C	C39	USB3_RX2_DP	D39	GND
A40	GND	B40	N/C	C40	GND	D40	N/C
A41	eDP_TX1_DN	B41	N/C	C41	N/C	D41	N/C
A42	eDP_TX1_DP	B42	GND	C42	N/C	D42	GND
A43	GND	B43	N/C	C43	GND	D43	USB3_TX1_DN
A44	eDP_TX2_DN	B44	N/C	C44	USB3_RX1_DN	D44	USB3_TX1_DN

A45	eDP_TX2_DP	B45	LID_N	C45	USB3_RX1_DN	D45	GND
A46	GND	B46	SLEEP_N	C46	GND	D46	N/C
A47	eDP_TX3_DN	B47	+V3P3A	C47	N/C	D47	N/C
A48	eDP_TX3_DP	B48	SPI0_CS_CN_N	C48	N/C	D48	GND
A49	GND	B49	BSEL0	C49	GND	D49	SATA_RX0_DN
A50	eSPI_IO0	B50	BSEL1	C50	BOOT_SPI_IO0	D50	SATA_RX0_DP
A51	eSPI_IO1	B51	BSEL2	C51	BOOT_SPI_IO1	D51	GND
A52	eSPI_IO2	B52	eSPI_ALERT0_N	C52	BOOT_SPI_IO2	D52	SATA_TX0_DN
A53	eSPI_IO3	B53	eSPI_ALERT1_N	C53	BOOT_SPI_IO3	D53	SATA_TX0_DP
A54	eSPI_CLK	B54	eSPI_CS0_CN_N	C54	BOOT_SPI_CLK	D54	GND
A55	GND	B55	N/C	C55	GND	D55	SATA_RX1_DN
A56	SRCCLKREQ0_N	B56	eSPI_RST0_N	C56	CLK_PCIE1_DN	D56	SATA_RX1_DP
A57	SRCCLKREQ1_N	B57	GND	C57	CLK_PCIE1_DP	D57	GND
A58	GND	B58	PCIE_BMC_RX_DN	C58	GND	D58	SATA_TX1_DN
A59	PCIE_BMC_TX_DN	B59	PCIE_BMC_RX_DP	C59	CLK_PCIE0_DN	D59	SATA_TX1_DP
A60	PCIE_BMC_TX_DP	B60	GND	C60	CLK_PCIE0_DP	D60	GND
A61	GND	B61	PCIE_RX9_DN	C61	GND	D61	PCIE_TX1_DN
A62	PCIE_TX9_DN	B62	PCIE_RX9_DP	C62	PCIE_RX1_DN	D62	PCIE_TX1_DP
A63	PCIE_TX9_DP	B63	GND	C63	PCIE_RX1_DP	D63	GND
A64	GND	B64	PCIE_RX10_DN	C64	GND	D64	PCIE_TX2_DN
A65	PCIE_TX10_DN	B65	PCIE_RX10_DP	C65	PCIE_RX2_DN	D65	PCIE_TX2_DP
A66	PCIE_TX10_DP	B66	GND	C66	PCIE_RX2_DP	D66	GND
A67	GND	B67	PCIE_RX11_DN	C67	GND	D67	PCIE_TX3_DN
A68	PCIE_TX11_DN	B68	PCIE_RX11_DP	C68	PCIE_RX3_DN	D68	PCIE_TX3_DP
A69	PCIE_TX11_DP	B69	GND	C69	PCIE_RX3_DP	D69	GND
A70	GND	B70	PCIE_RX12_DN	C70	GND	D70	PCIE_TX4_DN

A71	PCIE_TX12_DN	B71	PCIE_RX12_DP	C71	PCIE_RX4_DN	D71	PCIE_TX4_DP
A72	PCIE_TX12_DP	B72	GND	C72	PCIE_RX4_DP	D72	GND
A73	GND	B73	PCIE_RX17_DN	C73	GND	D73	PCIE_TX5_DN
A74	PCIE_TX17_DN	B74	PCIE_RX17_DP	C74	PCIE_RX5_DN	D74	PCIE_TX5_DP
A75	PCIE_TX17_DP	B75	GND	C75	PCIE_RX5_DP	D75	GND
A76	GND	B76	PCIE_RX18_DN	C76	GND	D76	PCIE_TX6_DN
A77	PCIE_TX18_DN	B77	PCIE_RX18_DP	C77	PCIE_RX6_DN	D77	PCIE_TX6_DP
A78	PCIE_TX18_DP	B78	GND	C78	PCIE_RX6_DP	D78	GND
A79	GND	B79	PCIE_RX19_DN	C79	GND	D79	PCIE_TX7_DN
A80	PCIE_TX19_DN	B80	PCIE_RX19_DP	C80	PCIE_RX7_DN	D80	PCIE_TX7_DP
A81	PCIE_TX19_DP	B81	GND	C81	PCIE_RX7_DP	D81	GND
A82	GND	B82	PCIE_RX20_DN	C82	GND	D82	PCIE_TX8_DN
A83	PCIE_TX20_DN	B83	PCIE_RX20_DP	C83	PCIE_RX8_DN	D83	PCIE_TX8_DP
A84	PCIE_TX20_DP	B84	GND	C84	PCIE_RX8_DP	D84	GND
A85	GND	B85	N/C	C85	GND	D85	L1_MDI0_N
A86	+VRTC_C	B86	RSMRST_OUT_C	C86	SMB_CLK_DUAL	D86	L1_MDI0_P
A87	SUS_CLK	B87	UART1_TXD	C87	SMB_DATA_DUAL	D87	GND
A88	EC_GPIO0	B88	UART1_RXD	C88	SMBALERT_N	D88	L1_MDI1_N
A89	EC_GPIO1	B89	UART1_RTS_N	C89	UART0_TXD	D89	L1_MDI1_P
A90	EC_GPIO2	B90	UART1_CTS_N	C90	UART0_RXD	D90	GND
A91	EC_GPIO3	B91	N/C	C91	UART0_RTS_N	D91	L1_MDI2_N
A92	EC_GPIO4	B92	N/C	C92	UART0_CTS_N	D92	L1_MDI2_P
A93	EC_GPIO5	B93	GSPI_MOSI	C93	SMB_CLK_EC	D93	GND
A94	EC_GPIO6	B94	GSPI_MISO	C94	SMB_DATA_EC	D94	L1_MDI3_N
A95	EC_GPIO7	B95	GSPI_CS0_N	C95	I2C0_ALERT_N	D95	L1_MDI3_P
A96	EC_GPIO8	B96	GSPI_CS1_N	C96	I2C1_SCL	D96	GND

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A97	EC_GPIO9	B97	N/C	C97	I2C1_DATA	D97	L1_LED_2500_N
A98	EC_GPIO10	B98	N/C	C98	L1_SDP	D98	L1_LED_1000_N
A99	EC_GPIO11	B99	GSPI_CLK	C99	N/C	D99	L1_LED_LINK_N/ACT_N
A100	Type0	B100	GSPI_ALERT_N	C100	TYPE1	D100	TYPE2

- **Connector J2**

J2							
Pin	RAW E	Pin	RAW F	Pin	RAW G	Pin	RAW H
E1	RAPID_SHUTDOWN	F1	N/C	G1	RSVD	H1	GND
E2	GND	F2	N/C	G2	GND	H2	USB2_SSTX0_DN
E3	DDI3_CTRLDATA_AUXN	F3	N/C	G3	USB3_RX3_DN	H3	USB2_SSTX0_DP
E4	DDI3_CTRLCLK_AUXP	F4	N/C	G4	USB3_RX3_DP	H4	GND
E5	GND	F5	N/C	G5	GND	H5	N/C
E6	DDI3_TX0_DN	F6	N/C	G6	N/C	H6	N/C
E7	DDI3_TX0_DP	F7	N/C	G7	N/C	H7	GND
E8	GND	F8	N/C	G8	GND	H8	USB3_SSTX0_DN
E9	DDI3_TX1_DN	F9	N/C	G9	USB3_RX4_DN	H9	USB3_SSTX0_DP
E10	DDI3_TX1_DP	F10	N/C	G10	USB3_RX4_DP	H10	GND
E11	GND	F11	N/C	G11	GND	H11	N/C
E12	DDI3_TX2_DN	F12	N/C	G12	N/C	H12	N/C
E13	DDI3_TX2_DP	F13	N/C	G13	N/C	H13	GND
E14	GND	F14	N/C	G14	GND	H14	USB2_AUX_DN

E15	DDI3_TX3_DN	F15	N/C	G15	N/C	H15	USB2_AUX_DP
E16	DDI3_TX3_DP	F16	N/C	G16	N/C	H16	GND
E17	GND	F17	N/C	G17	N/C	H17	USB3_AUX_DN
E18	DDI3_AUX_SEL	F18	N/C	G18	N/C	H18	USB3_AUX_DP
E19	DDI3_HPD	F19	GND	G19	PEG_LANE_REV_N	H19	GND
E20	GND	F20	PCIE_RX21_DN	G20	GND	H20	N/C
E21	PCIE_TX21_DN	F21	PCIE_RX21_DP	G21	N/C	H21	N/C
E22	PCIE_TX21_DP	F22	GND	G22	N/C	H22	N/C
E23	GND	F23	PCIE_RX22_DN	G23	GND	H23	N/C
E24	PCIE_TX22_DN	F24	PCIE_RX22_DP	G24	N/C	H24	N/C
E25	PCIE_TX22_DP	F25	GND	G25	N/C	H25	N/C
E26	GND	F26	PCIE_RX23_DN	G26	GND	H26	N/C
E27	PCIE_TX23_DN	F27	PCIE_RX23_DP	G27	N/C	H27	N/C
E28	PCIE_TX23_DP	F28	GND	G28	N/C	H28	N/C
E29	GND	F29	PCIE_RX24_DN	G29	GND	H29	N/C
E30	PCIE_TX24_DN	F30	PCIE_RX24_DP	G30	N/C	H30	N/C
E31	PCIE_TX24_DP	F31	GND	G31	N/C	H31	N/C
E32	GND	F32	N/C	G32	GND	H32	N/C
E33	N/C	F33	N/C	G33	N/C	H33	N/C
E34	N/C	F34	GND	G34	N/C	H34	N/C
E35	GND	F35	N/C	G35	GND	H35	N/C
E36	N/C	F36	N/C	G36	N/C	H36	N/C
E37	N/C	F37	GND	G37	N/C	H37	N/C
E38	GND	F38	N/C	G38	GND	H38	N/C
E39	N/C	F39	N/C	G39	N/C	H39	N/C
E40	N/C	F40	GND	G40	N/C	H40	N/C

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E41	GND	F41	N/C	G41	GND	H41	N/C
E42	N/C	F42	N/C	G42	N/C	H42	N/C
E43	N/C	F43	GND	G43	N/C	H43	GND
E44	GND	F44	PEG_RX0_DN	G44	GND	H44	PEG_TX8_DN
E45	PEG_TX0_DN	F45	PEG_RX0_DP	G45	PEG_RX8_DN	H45	PEG_TX8_DP
E46	PEG_TX0_DP	F46	GND	G46	PEG_RX8_DP	H46	GND
E47	GND	F47	PEG_RX1_DN	G47	GND	H47	PEG_TX9_DN
E48	PEG_TX1_DN	F48	PEG_RX1_DP	G48	PEG_RX9_DN	H48	PEG_TX9_DP
E49	PEG_TX1_DP	F49	GND	G49	PEG_RX9_DP	H49	GND
E50	GND	F50	PEG_RX2_DN	G50	GND	H50	PEG_TX10_DN
E51	PEG_TX2_DN	F51	PEG_RX2_DP	G51	PEG_RX10_DN	H51	PEG_TX10_DP
E52	PEG_TX2_DP	F52	GND	G52	PEG_RX10_DP	H52	GND
E53	GND	F53	PEG_RX3_DN	G53	GND	H53	PEG_TX11_DN
E54	PEG_TX3_DN	F54	PEG_RX3_DP	G54	PEG_RX11_DN	H54	PEG_TX11_DP
E55	PEG_TX3_DP	F55	GND	G55	PEG_RX11_DP	H55	GND
E56	GND	F56	PEG_RX4_DN	G56	GND	H56	PEG_TX12_DN
E57	PEG_TX4_DN	F57	PEG_RX4_DP	G57	PEG_RX12_DN	H57	PEG_TX12_DP
E58	PEG_TX4_DP	F58	GND	G58	PEG_RX12_DP	H58	GND
E59	GND	F59	PEG_RX5_DN	G59	GND	H59	PEG_TX13_DN
E60	PEG_TX5_DN	F60	PEG_RX5_DP	G60	PEG_RX13_DN	H60	PEG_TX13_DP
E61	PEG_TX5_DP	F61	GND	G61	PEG_RX13_DP	H61	GND
E62	GND	F62	PEG_RX6_DN	G62	GND	H62	PEG_TX14_DN
E63	PEG_TX6_DN	F63	PEG_RX6_DP	G63	PEG_RX14_DN	H63	PEG_TX14_DP
E64	PEG_TX6_DP	F64	GND	G64	PEG_RX14_DP	H64	GND
E65	GND	F65	PEG_RX7_DN	G65	GND	H65	PEG_TX15_DN
E66	PEG_TX7_DN	F66	PEG_RX7_DP	G66	PEG_RX15_DN	H66	PEG_TX15_DP

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E67	PEG_TX7_DP	F67	GND	G67	PEG_RX15_DP	H67	GND
E68	GND	F68	N/C	G68	GND	H68	N/C
E69	N/C	F69	N/C	G69	N/C	H69	N/C
E70	N/C	F70	GND	G70	N/C	H70	GND
E71	N/C	F71	L2_MDI0_N	G71	GND	H71	N/C
E72	N/C	F72	L2_MDI0_P	G72	N/C	H72	N/C
E73	N/C	F73	GND	G73	N/C	H73	GND
E74	N/C	F74	L2_MDI1_N	G74	GND	H74	N/C
E75	N/C	F75	L2_MDI1_P	G75	N/C	H75	N/C
E76	N/C	F76	GND	G76	N/C	H76	GND
E77	N/C	F77	L2_MDI2_N	G77	GND	H77	N/C
E78	N/C	F78	L2_MDI2_P	G78	N/C	H78	N/C
E79	L2_SDP	F79	GND	G79	N/C	H79	GND
E80	L2_LED_1000_N	F80	L2_MDI3_N	G80	GND	H80	N/C
E81	L2_LED_LINK_N/ACT_N	F81	L2_MDI3_P	G81	N/C	H81	N/C
E82	L2_LED_2500_N	F82	GND	G82	N/C	H82	GND
E83	GND	F83	N/C	G83	GND	H83	N/C
E84	N/C	F84	N/C	G84	N/C	H84	N/C
E85	N/C	F85	N/C	G85	N/C	H85	GND
E86	GND	F86	N/C	G86	GND	H86	N/C
E87	N/C	F87	N/C	G87	N/C	H87	N/C
E88	N/C	F88	GND	G88	N/C	H88	N/C
E89	GND	F89	N/C	G89	N/C	H89	N/C
E90	N/C	F90	N/C	G90	N/C	H90	N/C
E91	N/C	F91	GND	G91	N/C	H91	GND
E92	GND	F92	CLK_PCIE3_DN_BF	G92	GND	H92	N/C

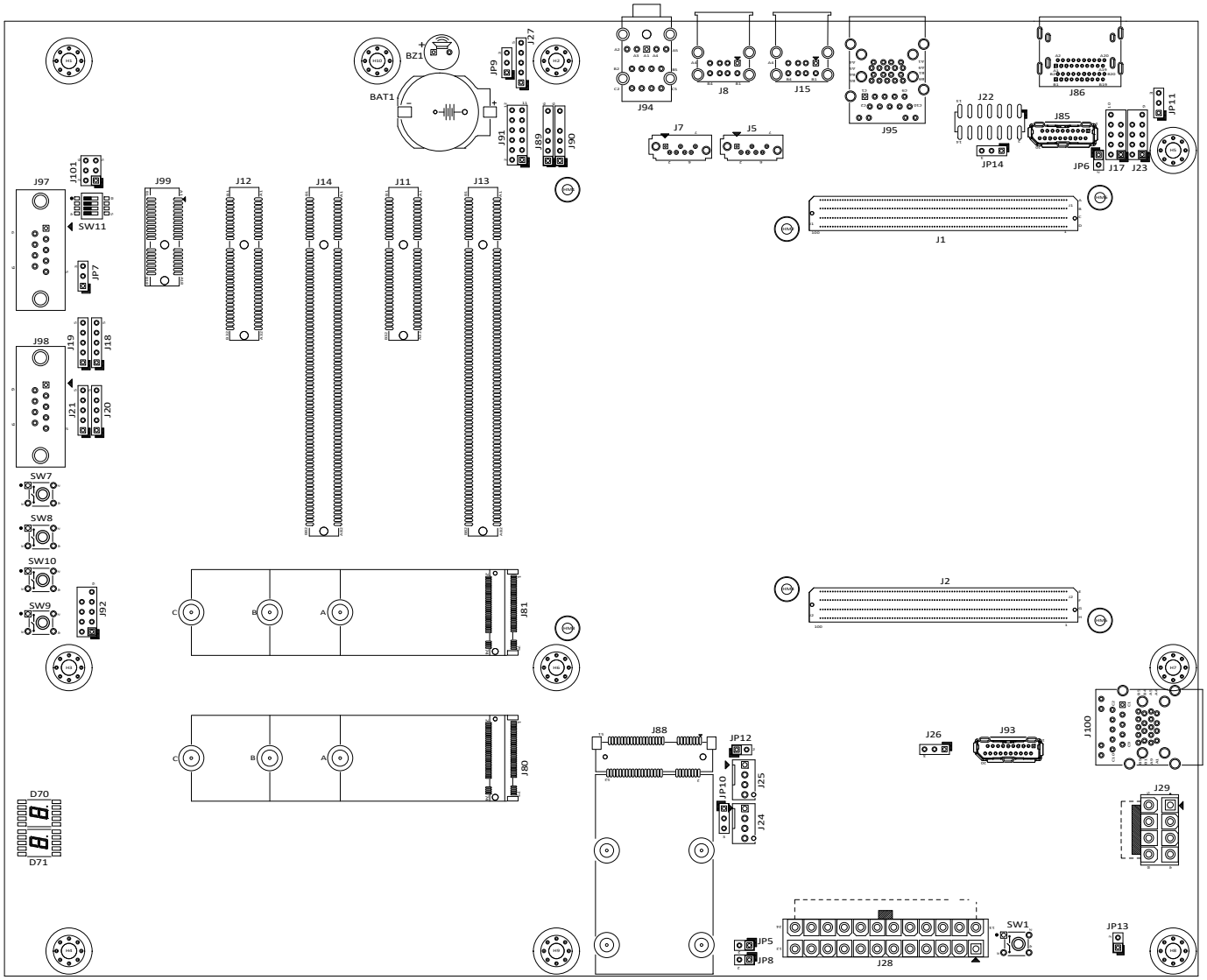
E93	CLK_PCIE2_DN_BF	F93	CLK_PCIE3_DP_BF	G93	N/C	H93	N/C
E94	CLK_PCIE2_DP_BF	F94	GND	G94	N/C	H94	GND
E95	GND	F95	N/C	G95	GND	H95	N/C
E96	SRCCLKREQ2_BF_N	F96	N/C	G96	N/C	H96	N/C
E97	SRCCLKREQ3_BF_N	F97	N/C	G97	N/C	H97	GND
E98	N/C	F98	N/C	G98	N/C	H98	N/C
E99	N/C	F99	N/C	G99	N/C	H99	N/C
E100	N/C	F100	N/C	G100	N/C	H100	N/C

Table 5 Pin out description

5 Connectors and Features

- **Layout silkscreen**

  The connector layout picture below shows each connector and its name designator.



PCIe Connectors

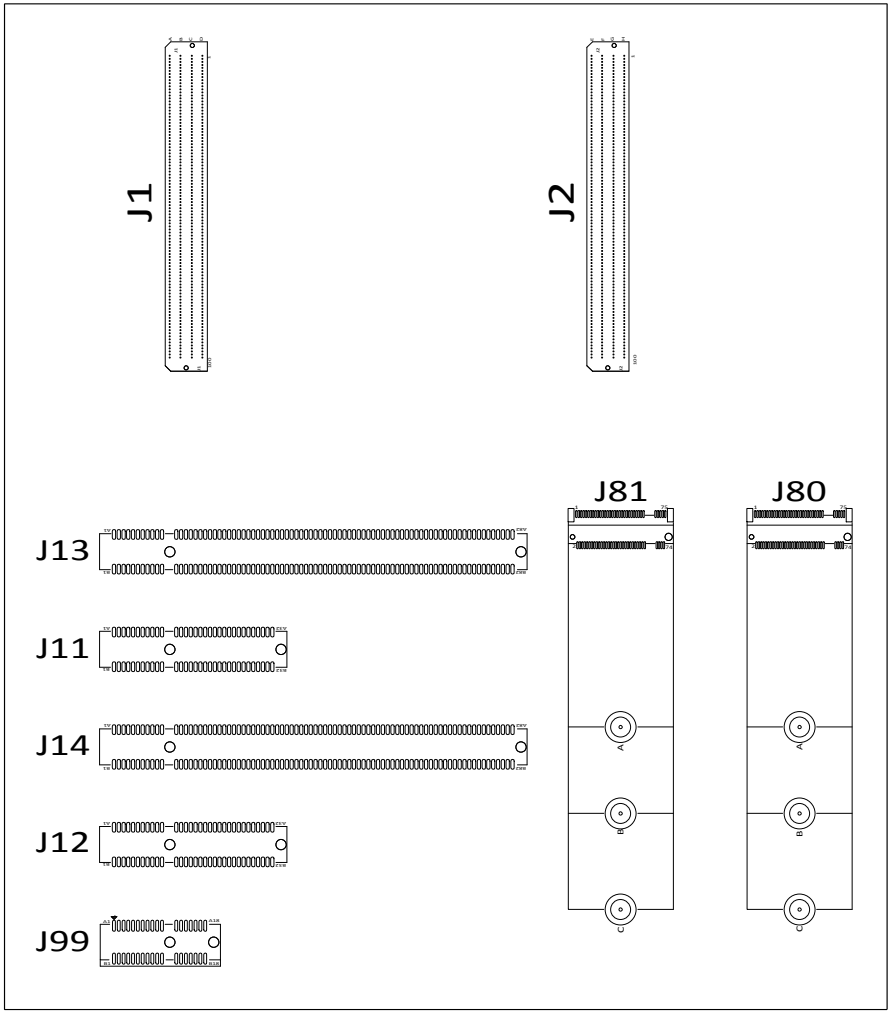
The PCOM-C880 provides the following PCIe connectors:

- PCIe x16 Slots
  J14 - #16 ~ #31 lanes
  J13 - #32 ~ #47 lanes

- PCIe x4 Slots
  J11 - #0 ~ #3 lanes
  J12 - #4 ~ #7 lanes

- M.2 Slots
  J80 - #8 ~ #11 lanes
  J81 - #12 ~ #15 lanes

- PCIe x1 Slot
  J99 - PCIe_BMC lanes



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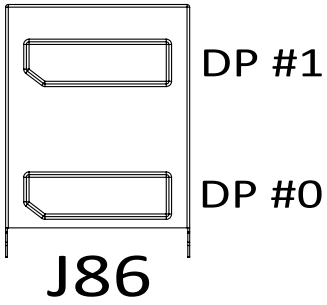
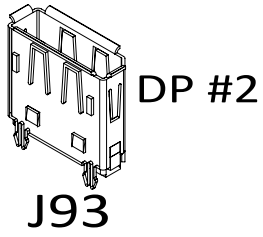
Display Interfaces

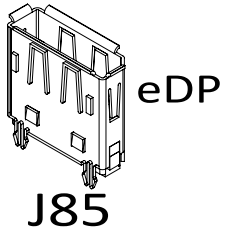
The PCOM-C880 provides total four DP connectors:

- Display Port ++
  The PCOM-C880 provides three DP++ ports via DDI interface, 2x DP on connector J86 (Rear I/O side), 1x DP on connector J93 (internal)

- eDP
  The PCOM-C880 connects the module's eDP interface to an internal DisplayPort (J85) for eDP signal evaluation.







USB

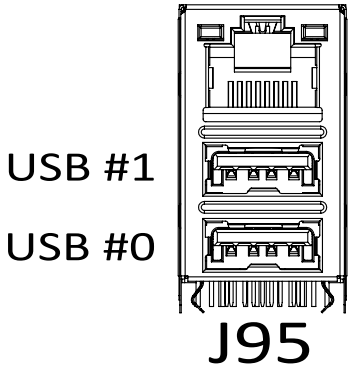
The PCOM-C880 provides the following USB connectors:

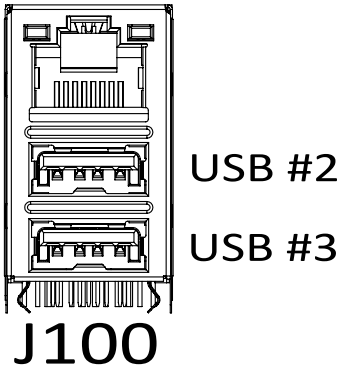
- J95 - Dual Stacked USB 3.2 Gen2 Type-A Ports

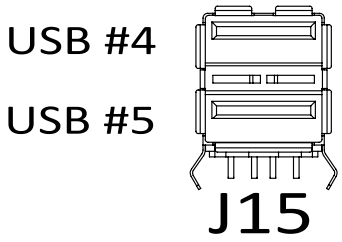
- J100 - Dual Stacked USB 3.2 Gen2 Type-A Ports
  (Internal I/O design for functional evaluation)

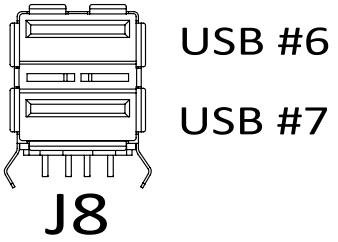
- J8 - Dual Stacked USB 2.0 Type-A Ports

- J15 - Dual Stacked USB 2.0 Type-A Ports









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SATA

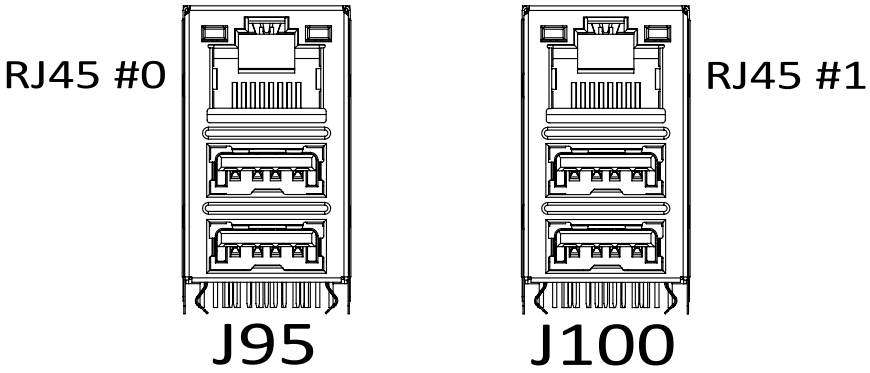
The PCOM-C880 provides two standard SATA connectors:

- J5 - SATA port 0
- J7 - SATA port 1

Ethernet

The PCOM-C880 provides two RJ45 ethernet ports:

- J95 - Ethernet port 0
- J100 - Ethernet port 1



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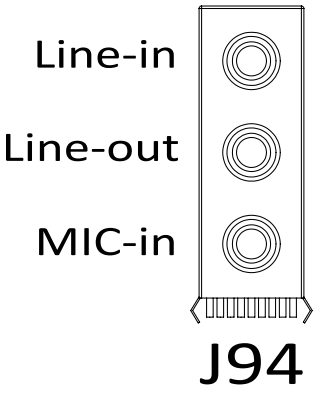
Audio

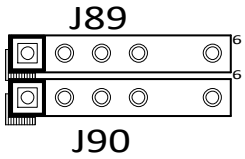
The PCOM-C880 features a multi-channel HDA codec (Realtek ALC888s).
The codec supports:

- MIC-In signals on connector J94 (lower jack)
- Line-in signals on connector J94 (upper jack)
- Line-out signal on connector J94 (middle jack)



The PCOM-C880 provides two SoundWire header for evaluation

- J89 - SoundWire 1
- J90 - SoundWire 0



J89 SoundWire 1

1	1.8V
2	SNDW_DMIC_DAT1
3	GND
4	SNDW_DMIC_CLK1
5	Key
6	3.3V

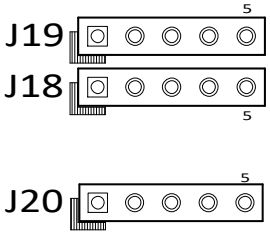
J90 SoundWire 0

1	1.8V
2	SNDW_DMIC_DAT0
3	GND
4	SNDW_DMIC_CLK0
5	Key
6	3.3V

I2C / SMBUS

The PCOM-C880 provides two I2C and one SMBUS header:

- J18 / J19 - I2C
- J20 - SMBUS



J18 I2C0

1	I2C0_CLK
2	I2C0_ALERT#
3	GND
4	I2C0_DAT
5	3.3V Standby

J19 I2C1

1	I2C1_CLK
2	
3	GND
4	I2C1_DAT
5	1.8V Standby

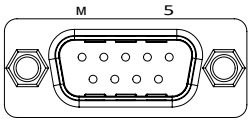
J20 SMB Bus

1	SMB_CLK
2	SMB_ALERT#
3	GND
4	SMB_DAT
5	3.3V Standby

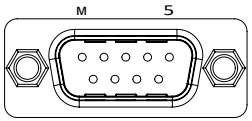
COM Ports

The PCOM-C880 provides two serial ports:

- Module Serial Port 0 - COM port 0 on connector J97
- Module Serial Port 1 - COM port 1 on connector J98



J97



J98

J97 COM Port 0

1	
2	RXD0#
3	TXD0#
4	
5	GND
6	
7	RTS0#
8	CTS0#
9	

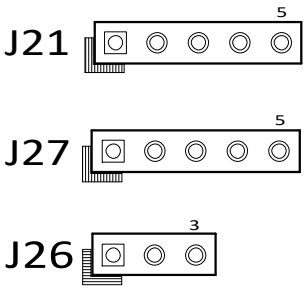
J97 COM Port 0

1	
2	RXD0#
3	TXD0#
4	
5	GND
6	
7	RTS0#
8	CTS0#
9	

IMPI / Watch Dog

The PCOM-C880 provides two IMPI and one WDT header:

- J21 - IMPI I2C
- J27 - IMPI USB
- J26 - WDT



J21 IPMI I2C

1	IPMB_CLK
2	
3	GND
4	IPMB_DAT
5	3.3V Standby

J27 IPMI USB

1	
2	USB0-_BMC
3	USB0+_BMC
4	GND
5	GND

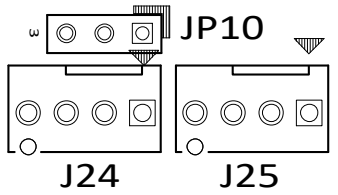
J26 WDT

1	WD_STROBE#
2	GND
3	WD_OUT

FAN

The PCOM-C880 provides two FAN header:

- J24 - 4 pin smart FAN support PWM control and RPM detection
- J25 - Normal FAN
- JP10 - Fan Voltage Selection
  [1-2] 12v
  [2-3] 5v

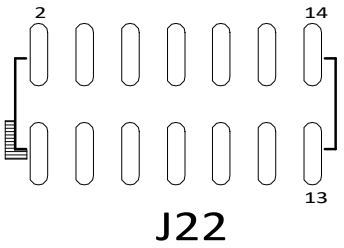


GPIO (General Purpose Input Output)

The PCOM-C880 provides 12bits GPIO on header J22.

- J22

1	GPIO_00	2	GPIO_06
3	GPIO_01	4	GPIO_07
5	GPIO_02	6	GPIO_08
7	GPIO_03	8	GPIO_09
9	GPIO_04	10	GPIO_10
11	GPIO_05	12	GPIO_11
13	GND	14	VCC3

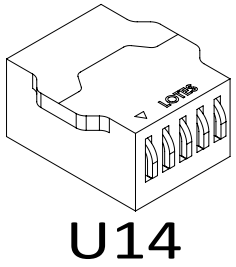


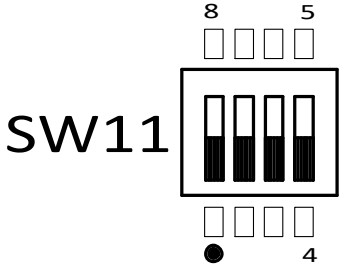
On carrier SPI socket (2nd boot BIOS)

The PCOM-C880 provides an 8-pin SOIC8 socket (U14) for an SPI flash, use SW11 to select the flash device to boot from.

➢ SW11

8	7	6	5
BSEL0	BSEL1	BSEL2	NC
1	2	3	4



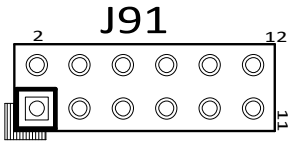


GP_SPI (General Purpose)

The PCOM-C880 provides an GP_SPI on header J91.

➢ J91

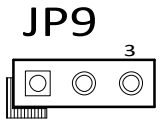
1	GP_SPI_MISO	2	GP_SPI_CS3#
3	GP_SPI_MOSI	4	GP_SPI_ALERT#
5	GP_SPI_CLK	6	GND
7	GP_SPI_CS0#	8	VCC3
9	GP_SPI_CS1#	10	3.3V Standby
11	GP_SPI_CS2#	12	PLTRST#

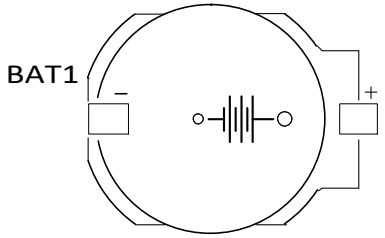


RTC Reset

The PCOM-C880 provides a holder BAT1 for attaching a CR2032 coin battery. The battery supplies power to the module RTC. To disconnect the RTC battery, set jumper JP9 to position [2-3].

- JP9 - RTC reset
  [1-2] Normal
  [2-3] Reset



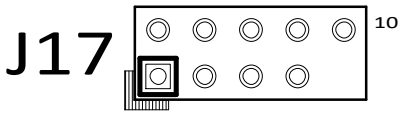


eSPI connector

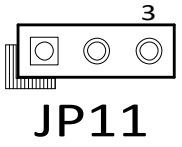
The PCOM-C880 provides eSPI signals on header J17.

- J17

1	eSPI_IO0	2	1.8V Standby
3	eSPI_IO1	4	eSPI_RST#
5	eSPI_IO2	6	eSPI_CS#
7	eSPI_IO3	8	eSPI_CLK
		10	GND



- JP11 - eSPI Voltage Selection
  [1-2] 1.8v
  [2-3] 3.3v



MIPI-CSI adaptor

The PCOM-C880 provides a MIPI-CSI adaptor on connector J88(mini-PCIe form factor) for signal measurement purpose.

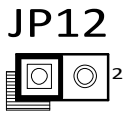
➢ J88

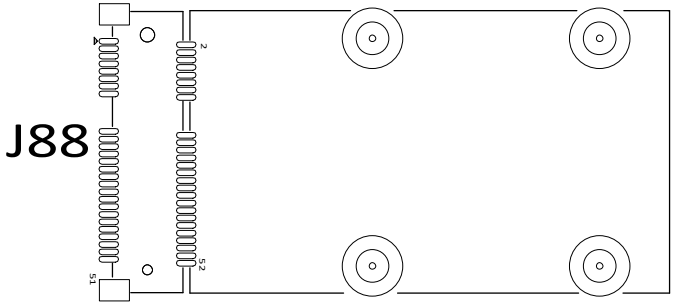
1	3	5	7	9	11	13	15	17
				GND	CSI_CLK-	CSI_CLK+	GND	
2	4	6	8	10	12	14	16	18
VCC3	GND				CSI_MCLK			GND

19	21	23	25	27	29	31	33	35
	GND	CSI_RX0-	CSI_RX0+	GND	GND	CSI_RX1-	CSI_RX1+	GND
20	22	24	26	28	30	32	34	36
CSI_ENA	CSI_RST#	VCC3	GND		CSI_I2C_CLK	CSI_I2C_DAT	GND	CSI_RX2-

37	39	41	43	45	47	49	51
GND	VCC3	VCC3	GND	CSI_RX3-	CSI_RX3+	GND	
38	40	42	44	46	48	50	52
CSI_RX2+	GND					GND	VCC3

➢ JP12 - CSI Port Selection
[1-2] CSI port 0
[open] CSI port 1





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6 Buttons and Others

- **Power button**

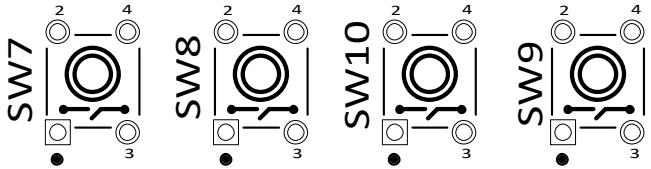
  When you press the power button SW10, it triggers the module's PWRBTN# signal. The triggered event usually initiates a transition from one power state to another (for example, from S5 to S0). However, the system's behavior depends on the ACPI settings of the operating system.

- **Reset button**

  When you press the reset button SW9, it triggers the module's SYS_RESET# signal. However, this behavior depends on the module reset signal design.

- **Sleep button**

  When you press the sleep button SW8, it triggers the module's SLEEP# signal. However, the system's behavior depends on the ACPI settings of the operating system.

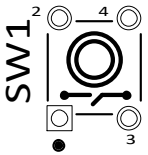


Lid button

When you press the lid button SW7, it triggers the module's LID# signal. However, the system's behavior depends on the ACPI settings of the operating system.

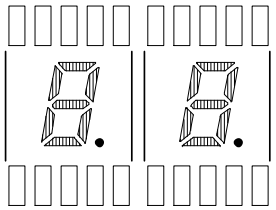
Rapid shutdown button

When you press the rapid shutdown button SW1, it triggers the module's RAPID_SHUTDOWN# signal. However, this behavior depends on the module rapid shutdown signal design.



Post code (80 port)

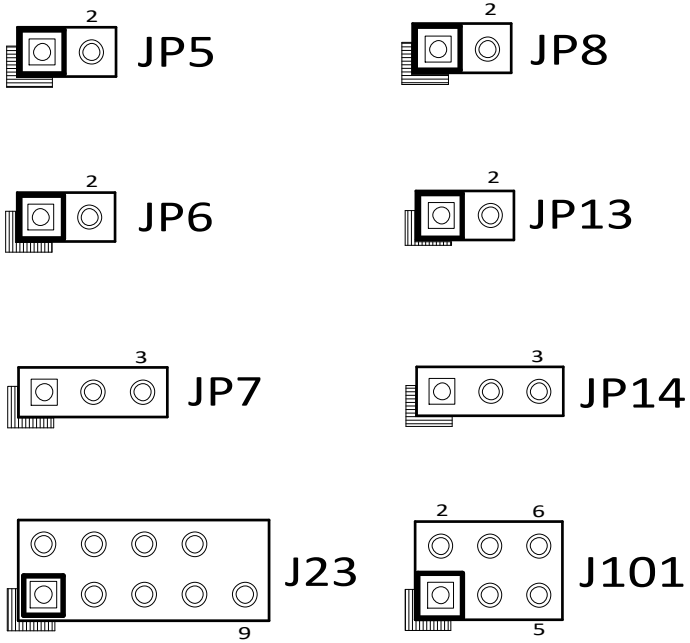
PCOM-C880 provides two 7-segment displays for post code or debug information.



Reserved Jumpers and Headers

The following jumpers and headers are reserved for Portwell internal debug only.

- JP5
- JP6
- JP7
- JP8
- JP13
- JP14
- J23
- J101



7 Packaging Information

PCOM-C880's packaging specification will follow the Portwell standard style.

Package	Appearance	Size
Anti-Static bubble bag		300x350mm
White Paper Box		390x310x58mm
Shipping Box (10 pcs White paper box)		620x405x330mm

Table 6 Packaging information

8 Industry Specifications

The list below provides links to industry specifications that apply to PORTWELL modules.

Low Pin Count Interface Specification
https://www.intel.com/content/www/us/en/design/technologies-and-topics/low-pin-count-interface-specification.html
Universal Serial Bus (USB) Specification, Revision 2.0 https://www.usb.org/
PCI Express Base Specification, Revision 5.0 https://pcisig.com/specifications
Serial ATA Specification, Revision 3.0 https://sata-io.org/
PICMG® COM-HPC® Overview https://www.picmg.org/openstandards/com-hpc/