

RUBY-D720VG2AR

Industrial Mainboard

User's Manual

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How to Use This Manual

The manual describes how to configure your RUBY-D720VG2AR system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Board Computer.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single board computer.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5 : Troubleshooting. Provides various useful tips to quickly get RUBY-D720VG2AR running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site : <http://www.portwell.com.tw/>.

Chapter 1

System Overview

1.1 Introduction

Powell Inc., a world-leading innovator in the Industrial PC (IPC) market and a member of the Intel® Communications Alliance, has launched its new RUBY-D720VG2AR in response to market demand for a simplified embedded system board (ESB) that combines a smaller footprint, lower power consumption, robust computing power and with longevity support.

Against the pre-generation chipset RUBY-D720VG2AR based on Q87 chipset, Q87 works with Intel 4th generation Core processor by LGA 1150 package, VGA, DVI-D, Display port, USB 3.0 and SATA III support which USB 3.0 is first integrated.

RUBY-D720VG2AR based on the latest 4th Gen Intel® Core Processor which offers 22nm Hi-K process technology with energy efficient architecture. RUBY-D720VG2AR adopts four channels DDR3 long DIMMs up to 32GB.

Desktop solution is still popular in the market of DVR and Factory Automation which can fulfill most of these applications; therefore, with high performance and high-end specifications, RUBY-D720VG2AR is our first choice with Q87 chip architecture on Micro ATX line.

1.2 Check List

The RUBY-D720VG2AR package should cover the following basic items

- ✓ One RUBY-D720VG2AR Micro-ATX Main Board
- ✓ One SATA Cable
- ✓ One I/O Shield bracket
- ✓ One Installation Resources CD-Title

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

- **Main Processor**
 - Intel® 4th Gen Dual Core/Quad Core LGA1150 processor
 - CPU clock bus: 1333/1600 MHz

- **Chipset**
 - Intel® Q87 chipset
- **System BIOS**
 - AMI BIOS
- **Main Memory**
 - Four 240-pin DDR3 Long-DIMM(non-ECC) socket support up to 16GB dual channel 1333/1600 MHz memory
- **Expansion Interface**
 - One PCIe x16
 - One PCIe x8
 - One PCIe x1 gold finger (include 1x PCIe x1 signal)
 - Two PCI slots
- **SATA Interface**
 - Five SATA 6Gb/s ports
 - One CFE (SATA 6Gb/s ports)
- **Serial Port**
 - Support five RS232 and one RS232/422/485
- **USB Interface**
 - Support twelve USB ports, four on rear I/O (USB 3.0) and eight on board header (USB 2.0) for internal devices
- **Audio Interface**
 - Connector for Mic-In, Line-In and Line-Out
- **Real Time Clock/Calendar (RTC)**
 - Support Y2K Real Time Clock/Calendar
- **Watch Dog Timer**
 - Support WDT function through software programming for enable/disable and interval setting
 - General system reset
- **On-board Ethernet LAN**
 - Two Gigabit Ethernet (10/100/1000 Mbits/sec) LAN ports using Intel WGI218-LM & WGI210-AT GbE Ethernet Controller
- **High Drive GPIO**
 - One pin-header for 8 bit GPIO (4bit in & 4bit out)
- **System Monitoring Feature**
 - Monitor system temperature and major power sources.
- **Outline Dimension (L x W)**
 - 243.8mm (9.6") X 243.8mm (9.6")

● Power Requirements

Item	Power ON	Full Loading 10Min	Full Loading 30Min
CPU +12V	1.39	1.53	1.55
System +12V	0.67	0.61	0.64
System +3.3V	0.56	0.66	0.67
System +5V	1.51	1.71	1.68
System+ Device +12V	2.79	2.78	2.76
System+ Device +5V	1.41	2.42	2.48
USB2.0 Loading Test	4.87~4.94 V/ 530 mA		
USB3.0 Loading Test	4.79 V/ 1060 mA		

● Configuration

CPU Type	Intel® Core™ i7-4770S Processor @ 3.90GHz L3 8 Mbytes Intel® Core™ i5-4590S Processor @ 3.70GHz L3 6 Mbytes
SBC BIOS	Portwell, Inc. RUBY-D720VG2AR-APK TEST BIOS
Memory	WARIS DDR3 UB-DIMM 1333 8GB*2 (Hynix)
VGA Card	Onboard Intel® HD Graphics
VGA Driver	Intel® HD Graphics Version: 10.18.10.3496
LAN Card	Onboard Realtek RTL8111F PCIe GBE Family Controller
LAN Driver	Realtek RTL8111F PCIe GBE Family Controller Version:
LAN Card	Onboard Realtek RTL8111F PCIe GBE Family Controller#2
LAN Driver	Realtek RTL8111F PCIe GBE Family Controller#2 Version:
Audio Card	Onboard Realtek ALC886 High Definition Audio
Audio Driver	Realtek ALC886 High Definition Audio Version: 6.0.1.7240
Chip Driver	Intel® H81 Chipset Device Software Version: 10.0.13
USB 3.0 Driver	Intel® USB3.0 eXtensible Host Controller
SATA HDD	Seagate ST3500411SV 500GB
CFEX	WARIS CFEX 8GB
CDROM	ASUS DRW-24D3ST
Power Supply	HG2-6350P 350W

● Operating Temperature

- °C ~ 60 °C

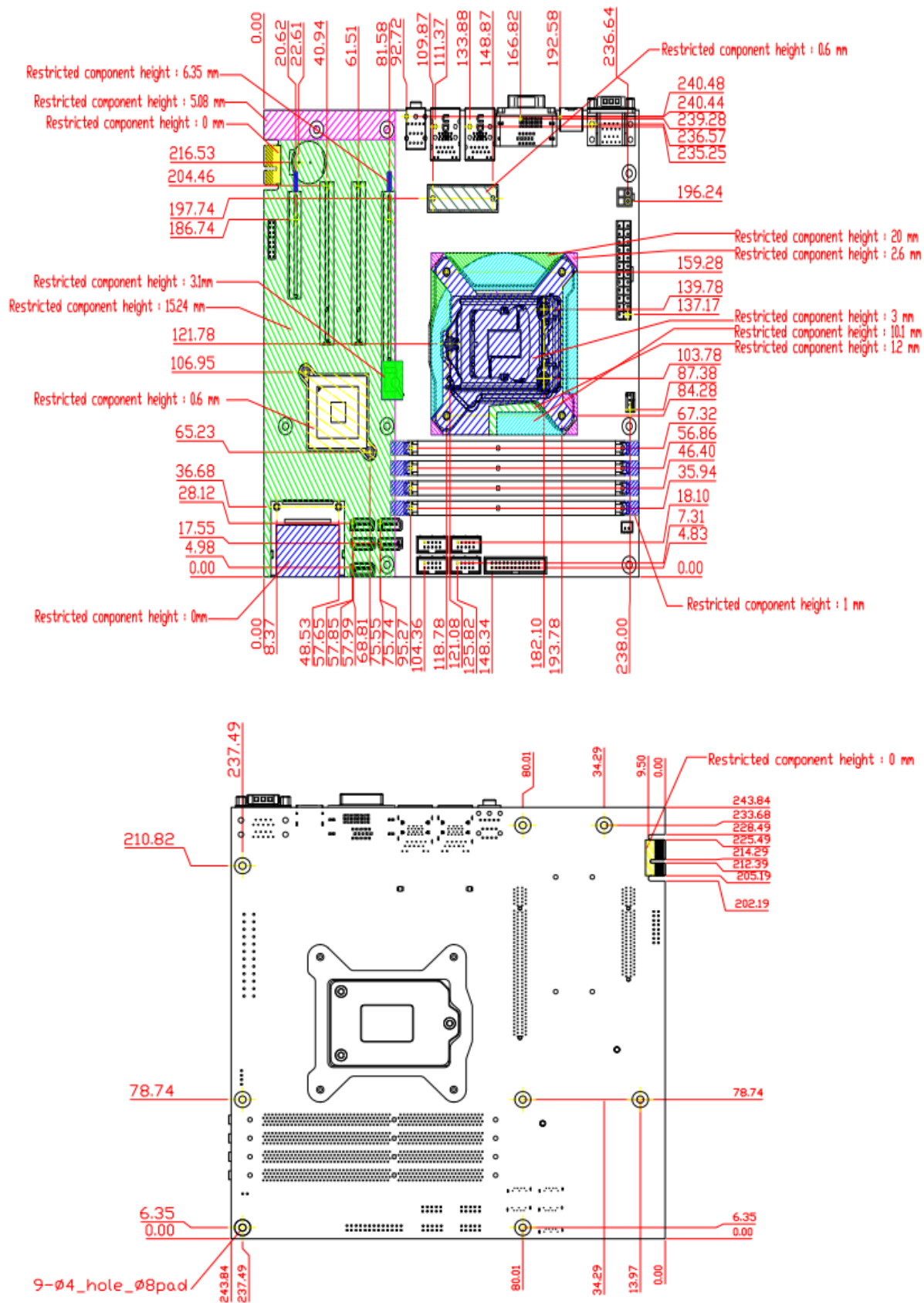
● Storage Temperature

-20 ~ 80 °C

● Relative Humidity

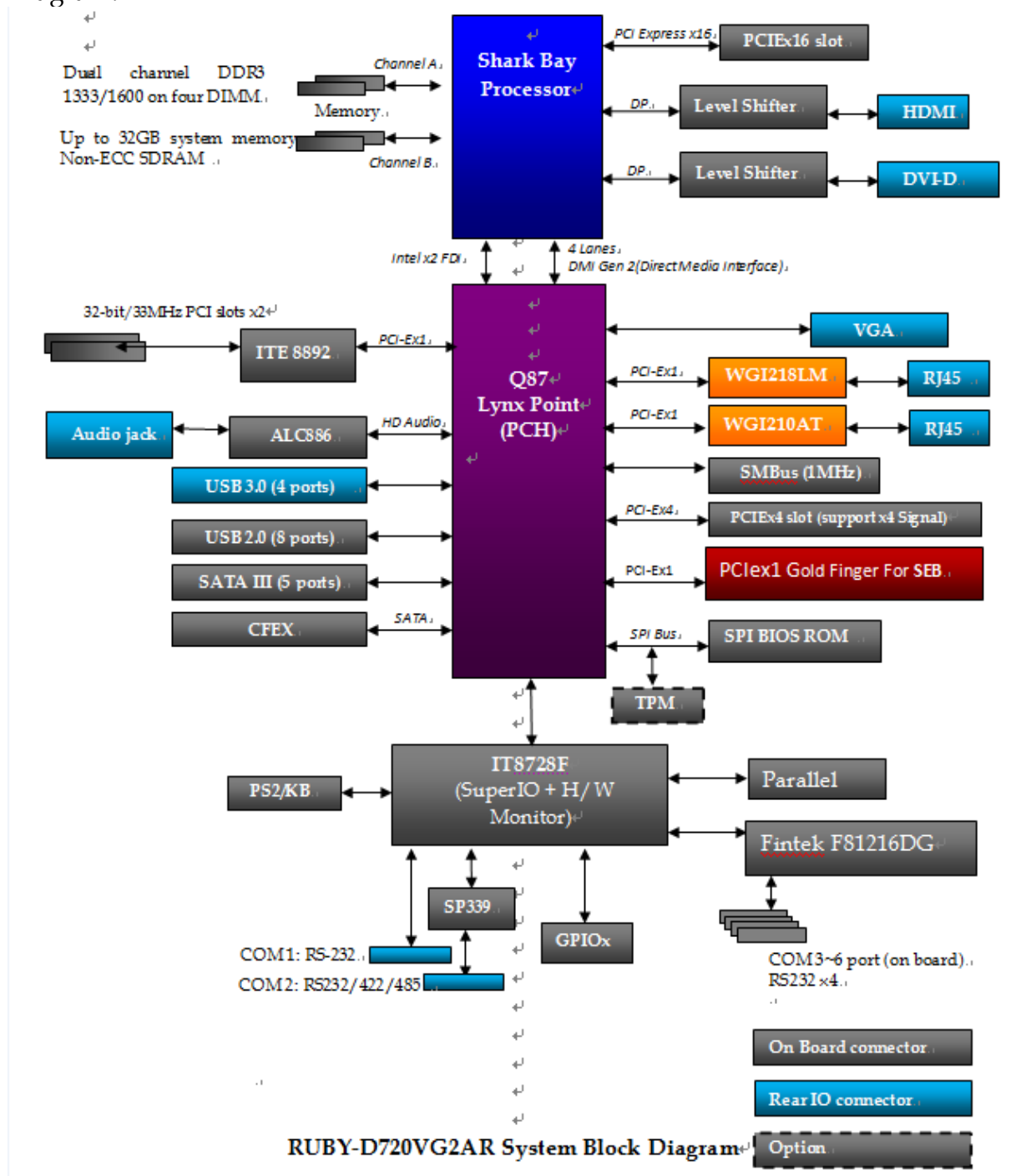
0% ~ 90%, non-condensing

1.3.1 Mechanical Drawing



1.4 System Architecture

All of details operating relations are shown in RUBY-D720VG2AR System Block Diagram.



Chapter 2 Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on Ruby-D720VG2AR are in the proper position. The default settings shipped from factory are marked with an asterisk (*).

2.1 Jumper

In general, jumpers on the single board computer are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for "Not Connect".

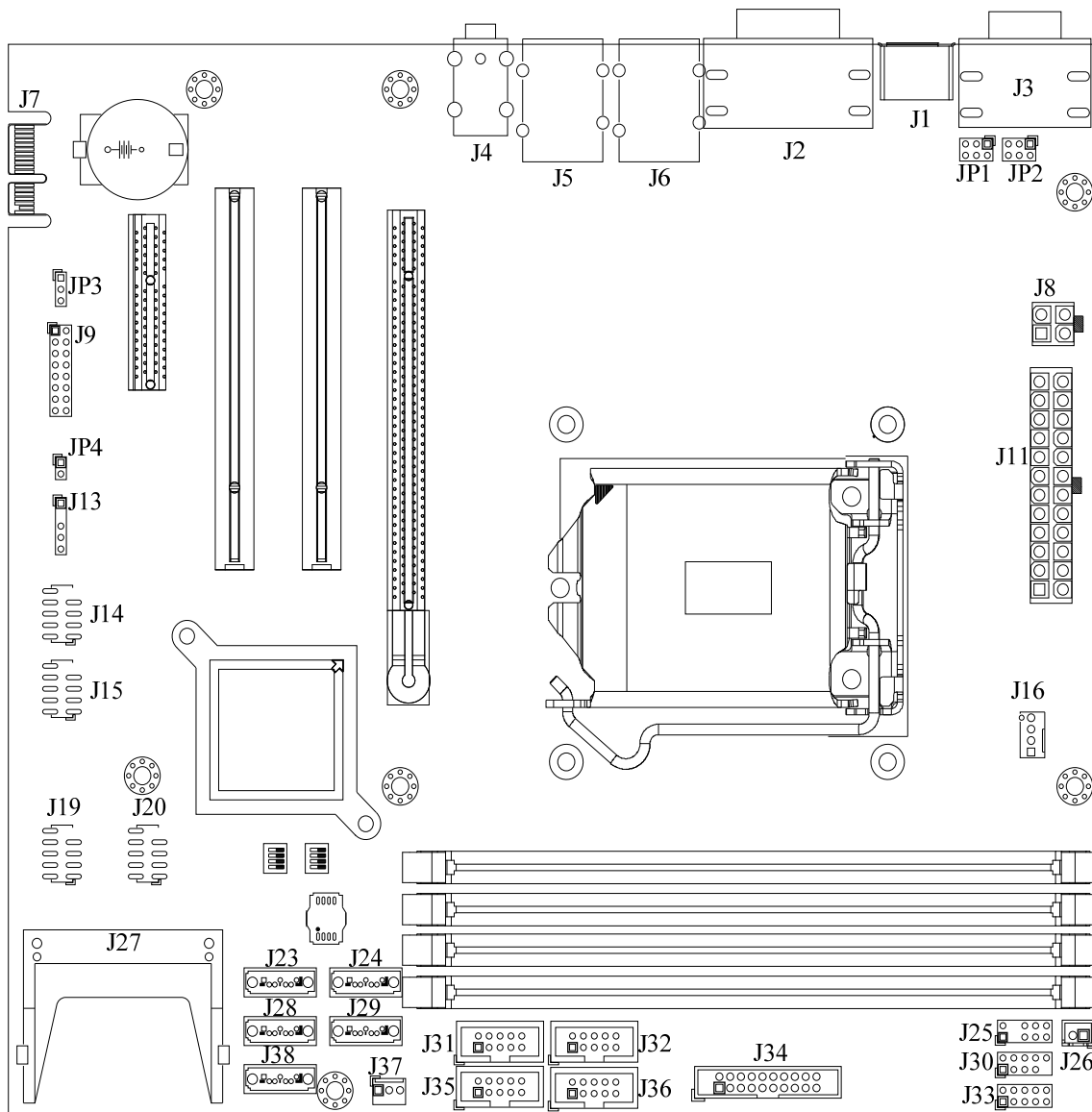
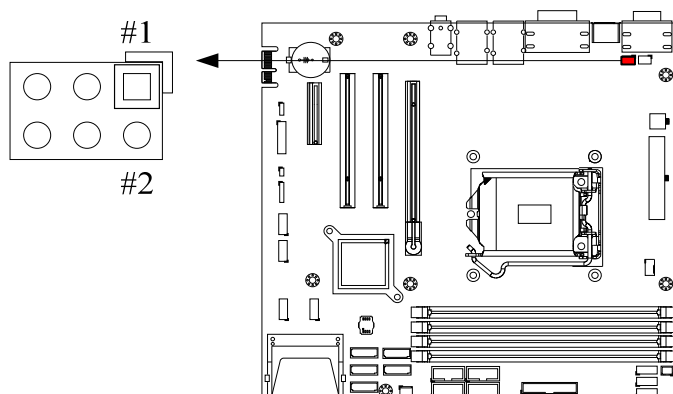


Figure 1-1 RUBY-D720VG2AR Top-side Jumper and Connector Locations

Pin Assignments of Connectors

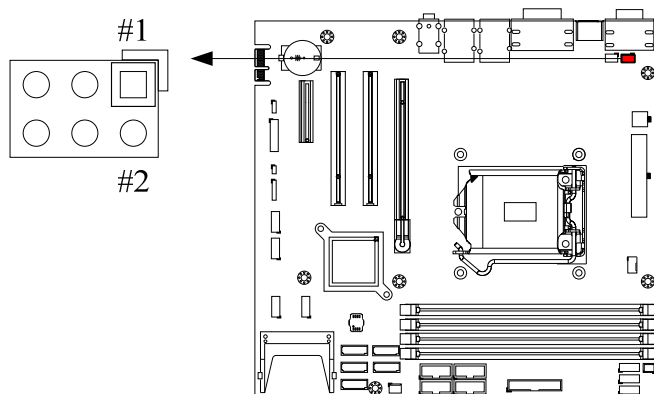
JP1: COM1 RI Function Selection

PIN No	Function
1-3 Short	+5V
3-4 Short	RI Signal
3-5 Short	+12V



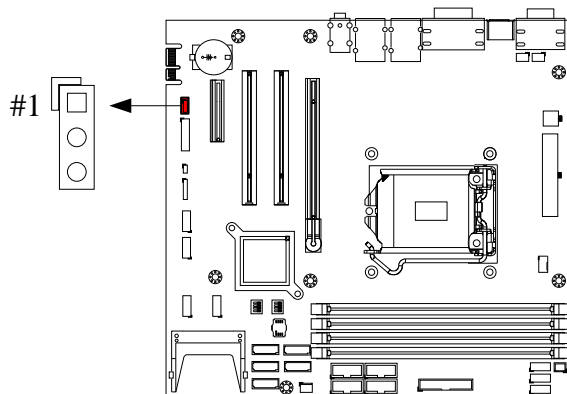
JP2: COM2 RI Function Selection

PIN No	Function
1-3 Short	+5V
3-4 Short	RI Signal
3-5 Short	+12V



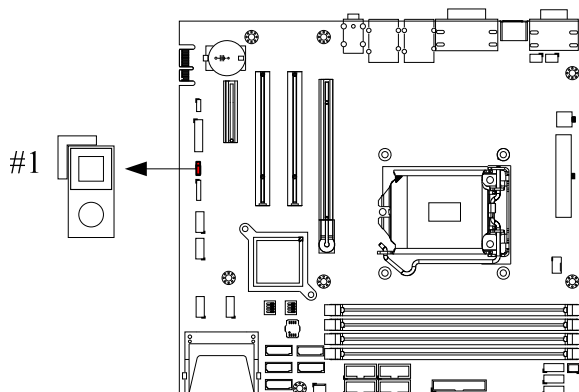
JP3: CMOS Clear

PIN No	Function
1-2 Short	Normal Operation
2-3 Short	Clear CMOS Contents



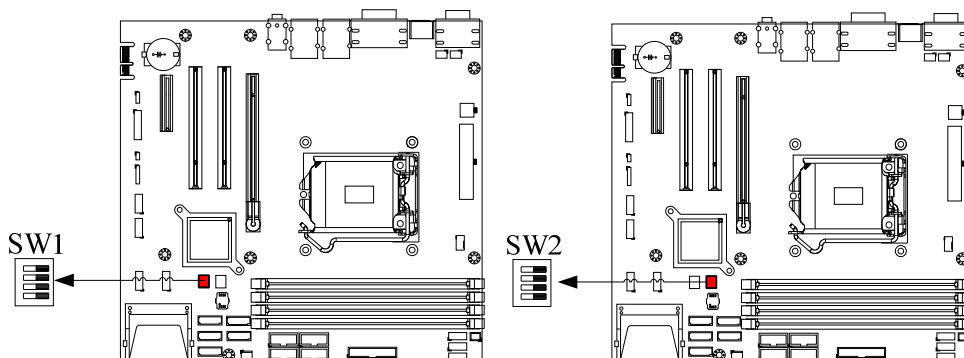
JP4: ATX Emulation AT Mode Selection

PIN No	Function
Short	ATX Emulation AT Mode
Open	ATX Mode



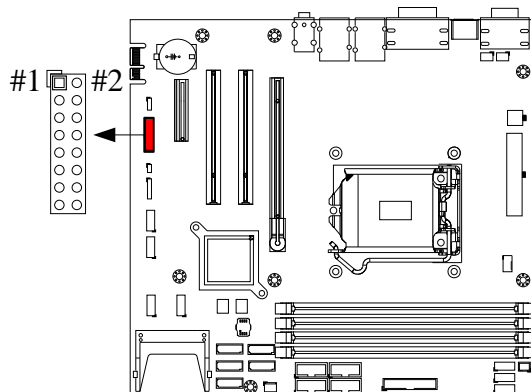
SW1/SW2: System Boot BIOS Selection

PIN No	Function
SW1_OFF , SW2_ON	Boot from main board
SW1_ON , SW2_OFF	Boot from CFEX



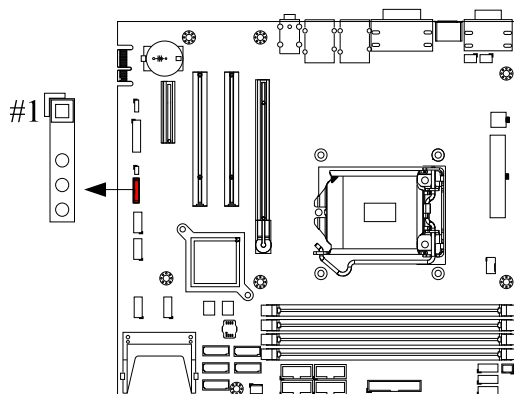
J9: Front Panel Pin HDR

PIN No.	Signal Description	PIN No.	Signal Description (Top Con.)
1	PWR_LED(+)	2	Speaker(+)
3	PWR_LED(-)	4	N/C
5	LAN1_ACT	6	N/C
7	LAN1_LINK	8	Speaker(-)
9	LAN2_LINK	10	Power On(-)
11	LAN2_ACT	12	Power On(+)
13	HDD_LED(+)	14	Reset (+)
15	HDD_LED(-)	16	Reset (-)



J13: SMBUS Connector

PIN No	Function
1	SMB_CLK
2	N/C
3	Ground
4	SMB_DAT
5	+5V

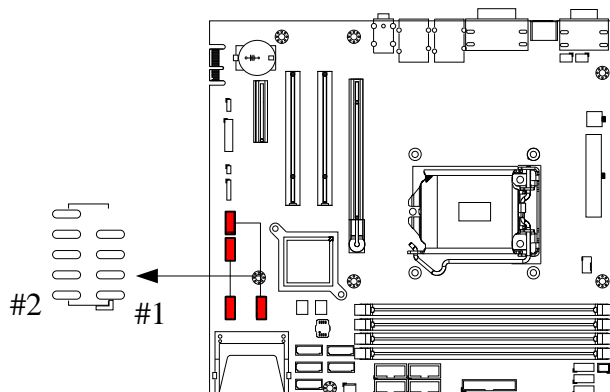


J14/J15/J19/J20: Internal USB Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	+5V	2	+5V
3	USB	4	USB
5	USB	6	USB
7	Ground	8	Ground
9	Key(no pin)	10	NC

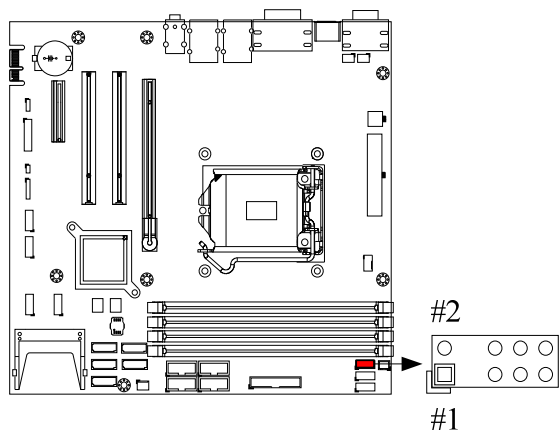
Note:

It's supplied by 5V VCC power source in normal operation mode .



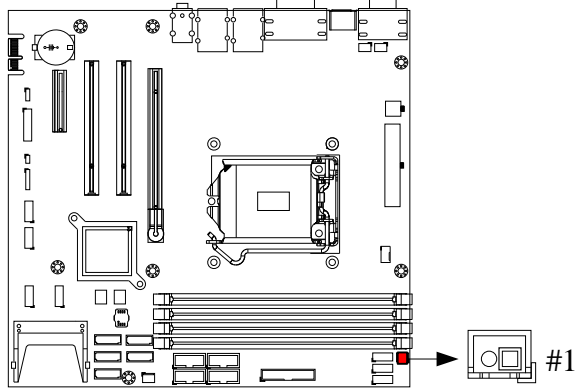
J25: Keyboard & Mouse Pin HDR

PIN No.	Signal Description	PIN No.	Signal Description
1	Mouse Data	2	Keyboard Date
3	Key(no pin)	4	Key(no pin)
5	Ground	6	Ground
7	+5V_Dual	8	+5V_Dual
9	Mouse Clock	10	Keyboard Clock



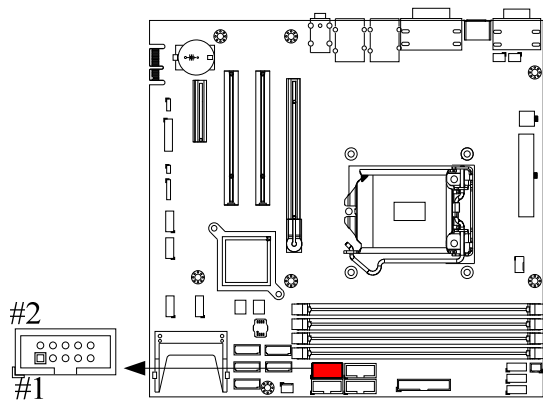
J26: CASEOPEN Connector

PIN No	Function
1	Ground
2	Signal



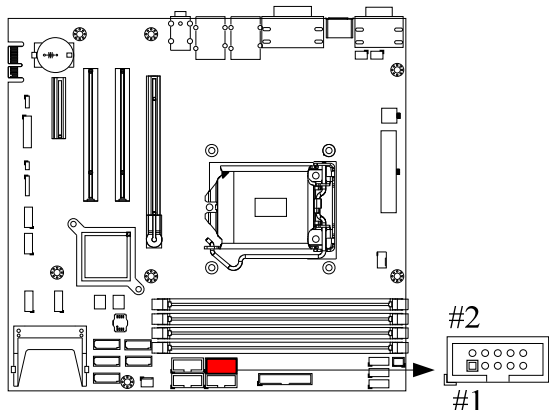
J31: COM6 Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	DCD	2	RXD
3	TXD	4	DTR
5	Ground	6	DSR
7	RTS	8	CTS
9	RI	10	N/C



J32: COM5 Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	DCD	2	RXD
3	TXD	4	DTR
5	Ground	6	DSR
7	RTS	8	CTS
9	RI	10	N/C

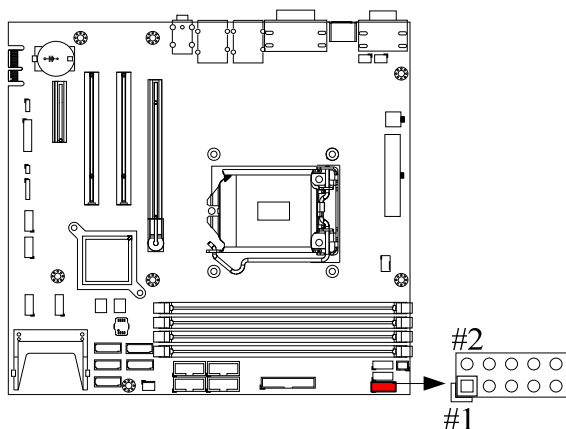


J33: General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO	2	GPIO
3	GPIO	4	GPIO
5	GPIO	6	GPIO
7	GPIO	8	GPIO
9	Ground	10	+5V

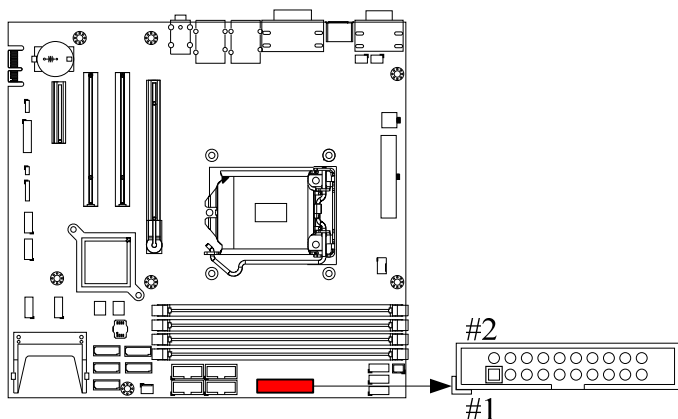
Note:

All General Purpose I/O ports can only apply to standard TTL $\pm 5\%$ signal level (0V/5V), and each Fan.



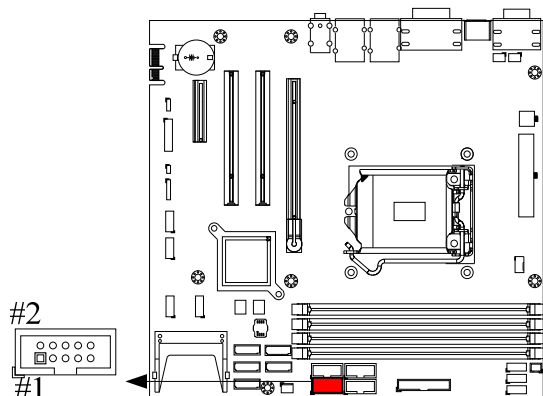
J34: Parallel Port Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Strobe#	14	Auto Form Feed#
2	Data0	15	Error#
3	Data1	16	Initialization#
4	Data2	17	GPIO
5	Data3	18	+5V
6	Data4	19	Printer Select IN#
7	Data5	20	Ground
8	Data6	21	Ground
9	Data7	22	Ground
10	Acknowledge#	23	Ground
11	Busy	24	Ground
12	Paper Empty	25	Ground
13	Printer Select	26	NC



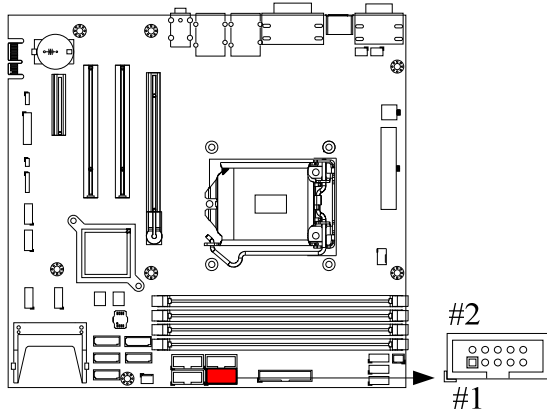
J35: COM3 Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	DCD	2	RXD
3	TXD	4	DTR
5	Ground	6	DSR
7	RTS	8	CTS
9	RI	10	N/C



J36: COM4 Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	DCD	2	RXD
3	TXD	4	DTR
5	Ground	6	DSR
7	RTS	8	CTS
9	RI	10	N/C



2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors.

Connector Function List

CONNECTOR	FUNCTION	REMARK
J1	HDMI Connector	
J2	VGA + DVI Connector	
J3	COM1 & 2 Connector	
J4	Audio Jack (Mic + Line_in + Line_out)	
J5	RJ45 + USB3.0 Connector	
J6	RJ45 + USB3.0 Connector	
J7	PCIe x 1 PCIE Goldfinger	
J8	+12V Power Connector	Connect to CPU
J9	Front Panel Pin HDR	
J10	PCIe x 4 signal , x8 Slot	
J11	ATX Power Connector	ATX 24P
J12	PCIe x 16 Slot	
J13	SMBUS Connector	5x1 pin header
J14/J15/J19/J20	Internal USB2.0 Connector	
J16	FAN (CPU FAN) Power Connector	
J17/J18/J21/J22	DDR3 Socket	
J23/J24/J28/J29/J38	SATA GEN3 Connector	
J25	Keyboard & Mouse Pin HDR	
J26	CASEOPEN#	
J27	CFEX	
J30	80 Port	
J31	COM6 Connector	
J32	COM5 Connector	
J33	General Purpose I/O Connector	
J34	Parallel Port Connector	
J35	COM3 Connector	
J36	COM4 Connector	
J37	FAN (SYSTEM FAN) Power Connector	
JP1	COM1 RI Function Selection	
JP2	COM2 RI Function Selection	
JP3	CMOS Clear	
JP4	ATX Emulation AT Mode Selection	
SW1/SW2	System Boot BIOS Selection	

Chapter 3

System Installation

This chapter provides the instructions to set up the system. The additional information is enclosed to help you set up onboard devices and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel® Dual Core/Quad Core processor

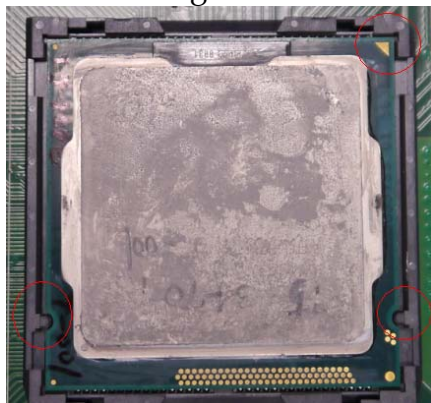
LGA-1150 CPU Socket

Pin1 corner of the CPU Socket



LGA-1150 CPU

Yellow Triangle Pin1 of the CPU



Alignment key

Notch

Please remember to locate the alignment keys on the CPU socket of the motherboard and the notches on the CPU.

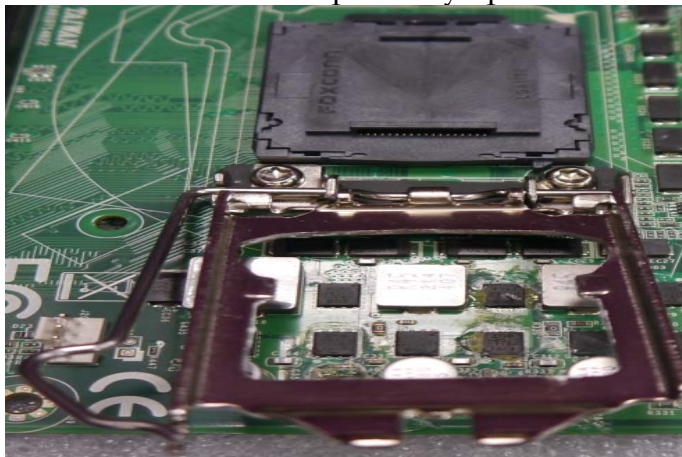
LGA-1150 CPU Installation Steps

Before install the CPU, please make sure to turn off the power first!!

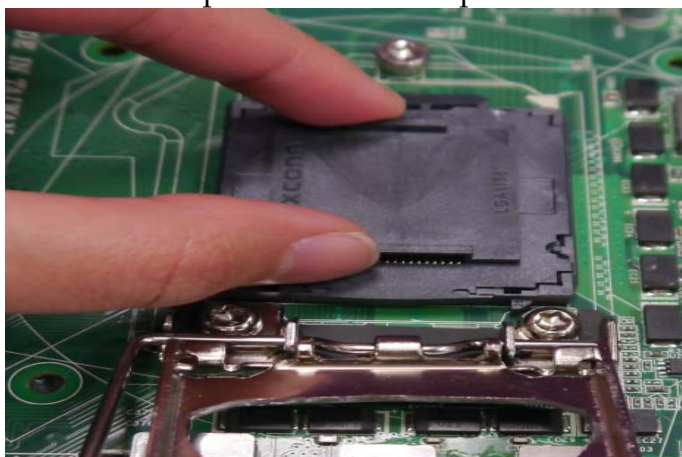
1. Open the load lever.



2. Lift the load lever up to fully open



3. Remove the plastic cap on the CPU socket. Before you install the CPU, always cover it to protect the socket pin.



4. After confirming the CPU direction for correct mating, put down the CPU in the socket housing frame. Note that alignment keys are matched.



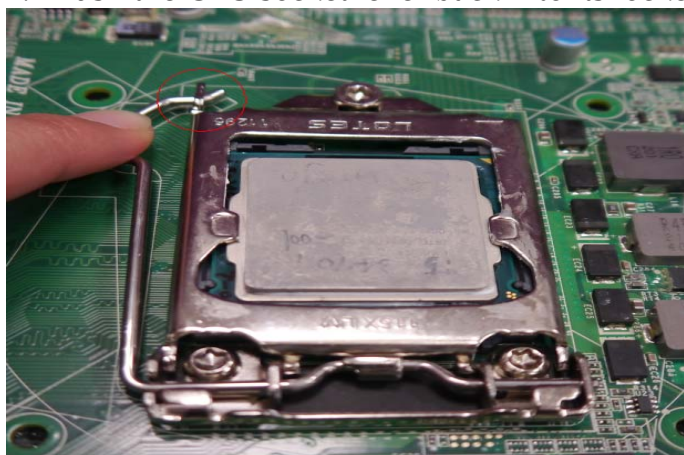
5. Make sure the CPU has been seated well into the socket. If not, take out the CPU and reinstall.



6. Engage the load lever while pressing down lightly onto the load plate.



7. Push the CPU socket lever back into its locked position.



8. Please make sure four hooks are in proper position before you install the core.

3.2 Main Memory

RUBY-D720 provide 4 x240 pin DIMM sockets (Dual Channel) which supports Dual channel 1333/1600 DDR3-SDRAM as main memory, non-register function. RUBY-D720 just supports Non-ECC memory. The maximum memory can be up to 32GB. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be set to either one double-sided DIMM in one DIMM socket or two single-sided DIMM in both sockets.

Beware of the connection and lock integrity from memory module to socket. Inserting improperly it will affect the system reliability.

Before locking, make sure that all modules have been fully inserted into the card slots

Note:

To insure the system stability, please do not change any of DRAM parameters in BIOS setup to modify system the performance without acquired technical information.

3.3 Installing the Single Board Computer

To install your RUBY-D720 into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position

Step 2 : Install and configure CPU and memory module at right position

Step 3 : Place RUBY-D720 into the dedicated position in the system

Step 4 : Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that SBC is properly inserted and fixed by mechanism.

Note

Please refer to section 3.3.1 to 3.3.7 to install INF/VGA/LAN/Audio / AMT drivers.

3.3.1 Chipset Component Driver

RUBY-D720 uses state-of-art Intel® Panther Point chipset. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for previous Windows Operating Systems such as Windows XP, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in RUBY-D720 CD-title.

Moreover, if using some old OS, the driver may not be supported anymore. We recommend changing the different OS to comply with this new chipset.

3.3.2 Intel® HD Graphics Family

With latest Intel® Core Ivy Bridge series structure, RUBY-D720 Intel® HD Graphic is built in with CPU. Therefore 2nd Generation Core and 3rd Generation Core CPUs provide HD integrated Graphic support sharing on board physical memories. RUBY-D716 has both internal VGA & DVI interface. This combination makes RUBY-D720 an excellent piece of multimedia hardware

With no additional video adaptor, this onboard video will usually be the system display output. By adjusting the BIOS setting to disable on-board VGA, an add-on PCI-Express Graphic card can take over the system display.

※To use Intel® Integrated HD Graphic, it's required to choose the CPU which has Integrated Graphic built-in. Otherwise there will be no display whatsoever.

3.3.3 Intel® PROSet Gigabit Ethernet Controller

Drivers Support

Please find Intel® WG1218LM and WG1210AT LAN driver in /Ethernet directory of RUBY-D720 CD-title. The driver supports Windows Win7 64-bits.

3.3.4 Audio Controller

Please find Intel® High Definition Audio driver form RUBY-D720 CD-title. The driver supports Windows Win7 64-bits.

3.3.5 Intel® Active Management Technology (Intel® AMT)

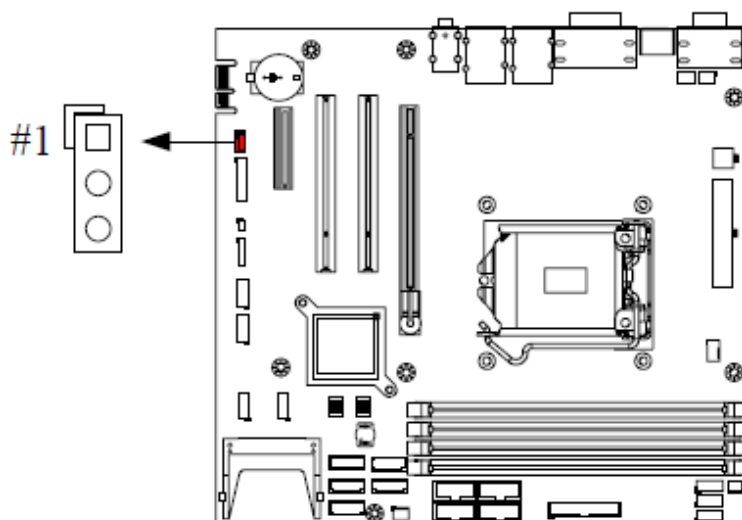
Please find the latest Intel®AMT 9.0 driver from RUBY-D720 CD-title. The driver supports Windows Win7 64-bits.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

JP3: CMOS Clear

JP3	Function
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS Contents



3.5 WDT Function

The Watchdog Timer of motherboard consists of 8-bit programmable time-out counter and a control and status register.

```
#include <stdio.h>
#include <conio.h>
#include <dos.h>

#define SIO_Port    0x2E
#define SIO_Port2 0x4E
#define GPIO_LDN   0x07

void Enter_IT872x_SIO() {
    outportb(SIO_Port, 0x87);
    outportb(SIO_Port, 0x01);
    outportb(SIO_Port, 0x55);
    outportb(SIO_Port, 0x55);
}

void Set_LDN(unsigned char LDN) {
    outportb(SIO_Port, 0x07);
    outportb(SIO_Port+1, LDN);
    printf("LDN=%x\n", LDN);
}

void Set_Register(unsigned char offset, unsigned char value) {
    outportb(SIO_Port, offset);
    outportb(SIO_Port+1, value);
    printf("Write offset:%x = %x\n", offset, value);
}

int main(void) {

    printf("test string\n");
    Enter_IT872x_SIO();
    Set_LDN(GPIO_LDN);

    Set_Register(0x72, 0xC0);
    Set_Register(0x73, 0x05);
    printf("System will reset in 5 seconds\n");

    return 0;
}
```

3.6 GPIO

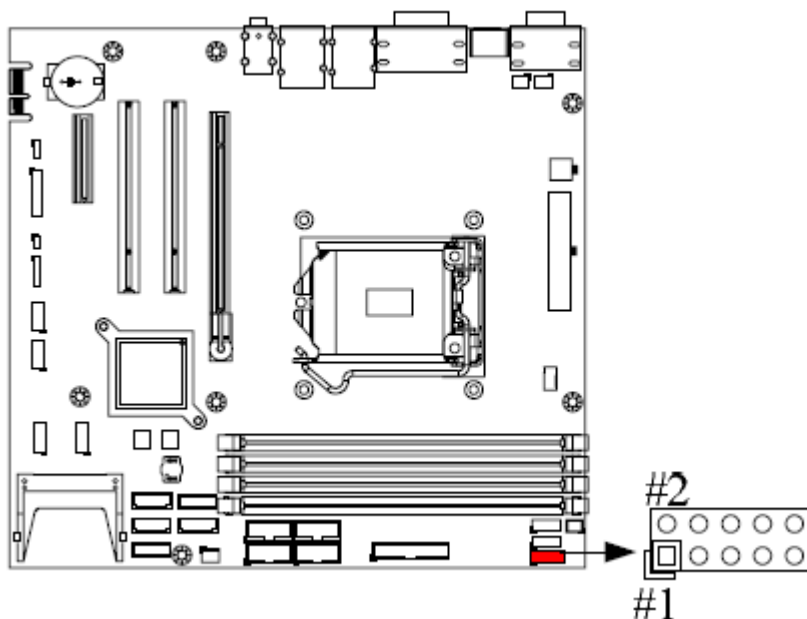
The motherboard provides 8 input / output ports that can be individually configured to perform a simple basic I/O function.

J33 : General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO	2	GPIO
3	GPIO	4	GPIO
5	GPIO	6	GPIO
7	GPIO	8	GPIO
9	Ground	10	+5V

Note:

All General Purpose I/O ports can only apply to standard TTL $\pm 5\%$ signal level (0V/5V), and each Fan.



```
/* This File was created by GPIO APP,Please don`t EDIT*/
/*****
Sample Code for ITE series SIO GPIO Access

SIO IO INDEX : 0x2E
GPIO IO BASE : 0x1818
GPIO PIN Define:
Pin 1 : GP15
Pin 2 : GP16
Pin 3 : GP47
Pin 4 : GP50
Pin 5 : GP14
Pin 6 : GP35
Pin 7 : GP36
Pin 8 : GP37
*****/

#include <stdio.h>
#include <conio.h>
#include <string.h>
#include <dos.h>

/*****
Common defines
*****/
#define HIGH 1
#define LOW 0
#define IN 1
#define OUT 0

/*=====

Prototype defines
=====*/

int Get_IT8728_GPIOBBase(
int IOINDEX
);

void Enter_IT8728_SIO(
int IOINDEX
);

void Exit_IT8728_SIO(
int IOINDEX
);
```

```
void Set_IT8728_LDN(
    int IOINDEX,
    int LDN
);

int Get_IT8728_Byte_Val(
    int IOINDEX,
    int offset
);

void Set_IT8728_Byte_Val(
    int IOINDEX,
    int offset,
    int Data
);

/*****
MAIN Code Start
*****/
int main()
{
    return;
}

/*****
Procedure Name : Get Super IO GPIO Base address
Check defines in config file name

input 1 : INT IOINDEX
return  : GPIO BASE
*****/
int Get_IT8728_GPIOBase(
    int IOINDEX
)
{
    int IODATA = IOINDEX + 1;
    int GPIOBASE;

    //SIO Enter Key
    Enter_IT8728_SIO(IOINDEX);
    //Change LDN to 7 (GPIO)
    Set_IT8728_LDN(IOINDEX,0x07);
    //Get GPIO BASE
    GPIOBASE = Get_IT8728_Byte_Val(IOINDEX,0x62) * 0x100;
    GPIOBASE = GPIOBASE + Get_IT8728_Byte_Val(IOINDEX,0x63);
```

```
return GPIOBASE;
}
```

```
/******
```

```
Procedure Name : Enter IT8728 Super IO
```

```
Check defines in config file name
```

```
input 1 : INT IOINDEX
```

```
*****/
```

```
void Enter_IT8728_SIO(
```

```
    int IOINDEX
```

```
)
```

```
{
```

```
int IODATA = IOINDEX + 1;
```

```
    outportb(IOINDEX,0x87);
```

```
    outportb(IOINDEX,0x01);
```

```
    outportb(IOINDEX,0x55);
```

```
    outportb(IOINDEX,0x55);
```

```
    return;
```

```
}
```

```
/******
```

```
Procedure Name : Exit IT8728 Super IO
```

```
Check defines in config file name
```

```
input 1 : INT IOINDEX
```

```
*****/
```

```
void Exit_IT8728_SIO(
```

```
    int IOINDEX
```

```
)
```

```
{
```

```
int IODATA = IOINDEX + 1;
```

```
    outportb(IOINDEX,0x02);
```

```
    outportb(IODATA ,0x02);
```

```
    return;
```

```
}
```

```
/******
```

```
Procedure Name : Change IT8728 LDN
```

```
Description      : Change Super IO Logical Device Number
```

```
input 1 : INT IOINDEX
```

```
input 2 : INT LDN(Logical Device Numbaer)
```

```
*****/
```

```
void Set_IT8728_LDN(
    int IOINDEX,
    int LDN
)
{
int IODATA = IOINDEX + 1;

outportb(IOINDEX,0x07);
outportb(IODATA, LDN);
return;
}

/*****
Procedure Name : Get IT8728 offset data
Description    : Get IT8728 offset byte data

input 1 : INT IOINDEX
input 2 : INT offset
return  : INT Data (Byte)
*****/
int Get_IT8728_Byte_Val(
    int IOINDEX,
    int offset
)
{
int Data;
int IODATA = IOINDEX + 1;

outportb(IOINDEX,offset);           //set offset of data read
Data = inportb(IODATA);             //Get Data from offset
return Data;
}

/*****
Procedure Name : Set IT8728 offset data
Description    : Set Byte data to IT8728 offset

input 1 : INT IOINDEX
input 2 : INT offset
input 3 : INT Data
*****/
void Set_IT8728_Byte_Val(
    int IOINDEX,
    int offset,
    int Data
)
}
```

```

{
int IODATA = IOINDEX + 1;

outportb(IOINDEX,offset);
outportb(IODATA, Data);
return;
}

```

```

/*****

```

Procedure Name : Set GPIO Pin 1 Mode & In/Out data

Description : Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will
dont care. and this function will return
read value.

Pin 1 : GP15

input 1 : INT GPIOMode

input 2 : INT Data

Out 1 : INT Data

```

*****/

```

```

int SET_GPIO_PIN1(

```

```

int GPIOMode,

```

```

int Data

```

```

)

```

```

{

```

```

    //GPIO Mode is Output

```

```

    if(GPIOMode = 0){

```

```

        Set_IT8728_Byte_Val(0x2E,0xC8,

```

```

Get_IT8728_Byte_Val(0x2E,0xC8) | (1<<5));

```

```

        //if Data is HIGH

```

```

        if(Data==1){

```

```

            outportb(0x1818 + 0, 1<<5);

```

```

        }

```

```

        //if Data is LOW

```

```

        if(Data==0){

```

```

            outportb(0x1818 + 0, (inportb(0x1818 + 0) & ~(1<<5) ));

```

```

        }

```

```

        return NULL;

```

```

    }

```

```

    //GPIO Mode is Input

```

```

    else if(GPIOMode = 1){

```

```

        Set_IT8728_Byte_Val(0x2E,0xC8,

```

```

Get_IT8728_Byte_Val(0x2E,0xC8) & ~(1<<5));

```

```

        Data = inportb(0x1818 + 0) & (1<<5);

```

```

        return Data;
    }

    return NULL;
}

/*****

```

Procedure Name : Set GPIO Pin 2 Mode & In/Out data

Description : Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will
 dont care. and this function will return
 read value.

Pin 2 : GP16

input 1 : INT GPIOMode

input 2 : INT Data

Out 1 : INT Data

*****/

```

int SET_GPIO_PIN2(
int GPIOMode,
int Data
)
{
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8728_Byte_Val(0x2E,0xC8,
Get_IT8728_Byte_Val(0x2E,0xC8) | (1<<6));

        //if Data is HIGH
        if(Data==1){
            outportb(0x1818 + 0, 1<<6 );
        }
        //if Data is LOW
        if(Data==0){

```



```

        outportb(0x1818 + 0, (inportb(0x1818 + 0) & ~(1<<6) ));
    }
    return NULL;
}
//GPIO Mode is Input
else if(GPIOMode = 1){
    Set_IT8728_Byte_Val(0x2E,0xC8,
Get_IT8728_Byte_Val(0x2E,0xC8) & ~(1<<6));

        Data = inportb(0x1818 + 0) & (1<<6);
        return    Data;
    }

    return NULL;
}

/*****

```

Procedure Name : Set GPIO Pin 3 Mode & In/Out data

Description : Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will
dont care. and this function will return
read value.

Pin 3 : GP47

input 1 : INT GPIOMode

input 2 : INT Data

Out 1 : INT Data

*****/

```

int SET_GPIO_PIN3(
int GPIOMode,
int Data
)
{
    //GPIO Mode is Output

```

```

        if(GPIOMode = 0){
            Set_IT8728_Byte_Val(0x2E,0xCB,
Get_IT8728_Byte_Val(0x2E,0xCB) | (1<<7));

            //if Data is HIGH
            if(Data==1){
                outportb(0x1818 + 3, 1<<7 );
            }
            //if Data is LOW
            if(Data==0){
                outportb(0x1818 + 3, (inportb(0x1818 + 3) & ~(1<<7) ) );
            }
            return NULL;
        }
        //GPIO Mode is Input
        else if(GPIOMode = 1){
            Set_IT8728_Byte_Val(0x2E,0xCB,
Get_IT8728_Byte_Val(0x2E,0xCB) & ~(1<<7));

            Data = inportb(0x1818 + 3) & (1<<7);
            return Data;
        }

        return NULL;
    }

/*****

```

Procedure Name : Set GPIO Pin 4 Mode & In/Out data

Description : Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will
dont care. and this function will return
read value.

Pin 4 : GP50

input 1 : INT GPIOMode

input 2 : INT Data

Out 1 : INT Data

```

*****/

int SET_GPIO_PIN4(
int GPIOMode,
int Data
)
{
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8728_Byte_Val(0x2E,0xCC,
Get_IT8728_Byte_Val(0x2E,0xCC) | (1<<0));

        //if Data is HIGH
        if(Data==1){
            outputb(0x1818 + 4, 1<<0);
        }
        //if Data is LOW
        if(Data==0){
            outputb(0x1818 + 4, (inportb(0x1818 + 4) & ~(1<<0) ));
        }
        return NULL;
    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){
        Set_IT8728_Byte_Val(0x2E,0xCC,
Get_IT8728_Byte_Val(0x2E,0xCC) & ~(1<<0));

        Data = inportb(0x1818 + 4) & (1<<0);
        return Data;
    }
    return NULL;
}

/*****

```

Procedure Name : Set GPIO Pin 5 Mode & In/Out data

Description : Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will

dont care. and this function will return

read value.

Pin 5 : GP14

input 1 : INT GPIOMode

input 2 : INT Data

Out 1 : INT Data

***** /

```

int SET_GPIO_PIN5(
int GPIOMode,
int Data
)
{
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8728_Byte_Val(0x2E,0xC8,
Get_IT8728_Byte_Val(0x2E,0xC8) | (1<<4));

        //if Data is HIGH
        if(Data==1){
            outportb(0x1818 + 0, 1<<4 );
        }
        //if Data is LOW
        if(Data==0){
            outportb(0x1818 + 0, (inportb(0x1818 + 0) & ~(1<<4) ) );
        }
        return NULL;
    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){
        Set_IT8728_Byte_Val(0x2E,0xC8,
Get_IT8728_Byte_Val(0x2E,0xC8) & ~(1<<4));

        Data = inportb(0x1818 + 0) & (1<<4);
        return Data;
    }
    return NULL;
}

```

```

/*****

```

Procedure Name : Set GPIO Pin 6 Mode & In/Out data

Description : Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will
 dont care. and this function will return
 read value.

Pin 6 : GP35

input 1 : INT GPIOMode

input 2 : INT Data

Out 1 : INT Data

```

*****/

```

```

int SET_GPIO_PIN6(
int GPIOMode,
int Data
)
{
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8728_Byte_Val(0x2E,0xCA,
Get_IT8728_Byte_Val(0x2E,0xCA) | (1<<5));

        //if Data is HIGH
        if(Data==1){
            outputb(0x1818 + 2, 1<<5);
        }
        //if Data is LOW
        if(Data==0){
            outputb(0x1818 + 2, (inportb(0x1818 + 2) & ~(1<<5) ) );
        }
        return NULL;
    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){

```

```

        Set_IT8728_Byte_Val(0x2E,0xCA,
Get_IT8728_Byte_Val(0x2E,0xCA) & ~(1<<5));

        Data = inportb(0x1818 + 2) & (1<<5);
        return    Data;
    }
    return NULL;
}

```

```

/*****

```

Procedure Name : Set GPIO Pin 7 Mode & In/Out data

Description : Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will
dont care. and this function will return
read value.

Pin 7 : GP36

input 1 : INT GPIOMode

input 2 : INT Data

Out 1 : INT Data

```

*****/

```

```

int SET_GPIO_PIN7(
int GPIOMode,
int Data
)
{
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8728_Byte_Val(0x2E,0xCA,
Get_IT8728_Byte_Val(0x2E,0xCA) | (1<<6));

        //if Data is HIGH
        if(Data==1){
            outportb(0x1818 + 2, 1<<6);

```

```

        }
        //if Data is LOW
        if(Data==0){
            outportb(0x1818 + 2, (inportb(0x1818 + 2) & ~(1<<6) ));
        }
        return NULL;
    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){
        Set_IT8728_Byte_Val(0x2E,0xCA,
        Get_IT8728_Byte_Val(0x2E,0xCA) & ~(1<<6));

        Data = inportb(0x1818 + 2) & (1<<6);
        return Data;
    }
    return NULL;
}

/*****

```

Procedure Name : Set GPIO Pin 8 Mode & In/Out data

Description : Set GPIO Pin I/O Mode

if GPIOMode is Input , input 2 data will
dont care. and this function will return
read value.

Pin 8 : GP37

input 1 : INT GPIOMode

input 2 : INT Data

Out 1 : INT Data

*****/

```

int SET_GPIO_PIN8(
int GPIOMode,
int Data
)

```

```
{
    //GPIO Mode is Output
    if(GPIOMode = 0){
        Set_IT8728_Byte_Val(0x2E,0xCA,
Get_IT8728_Byte_Val(0x2E,0xCA) | (1<<7));

        //if Data is HIGH
        if(Data==1){
            outportb(0x1818 + 2, 1<<7 );
        }
        //if Data is LOW
        if(Data==0){
            outportb(0x1818 + 2, (inportb(0x1818 + 2) & ~(1<<7) ) );
        }
        return NULL;
    }
    //GPIO Mode is Input
    else if(GPIOMode = 1){
        Set_IT8728_Byte_Val(0x2E,0xCA,
Get_IT8728_Byte_Val(0x2E,0xCA) & ~(1<<7));

        Data = inportb(0x1818 + 2) & (1<<7);
        return Data;
    }
    return NULL;
}
/* This File was created by GPIO APP,Please don't ED
```


Chapter 4

BIOS Setup Information

RUBY-D720 is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, RUBY-D720 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

4.1 Entering Setup -- Launch System Setup

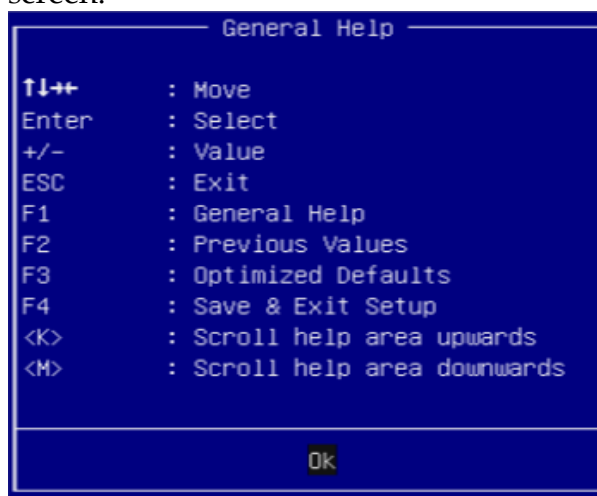
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press key will enter BIOS setup screen.

Press to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

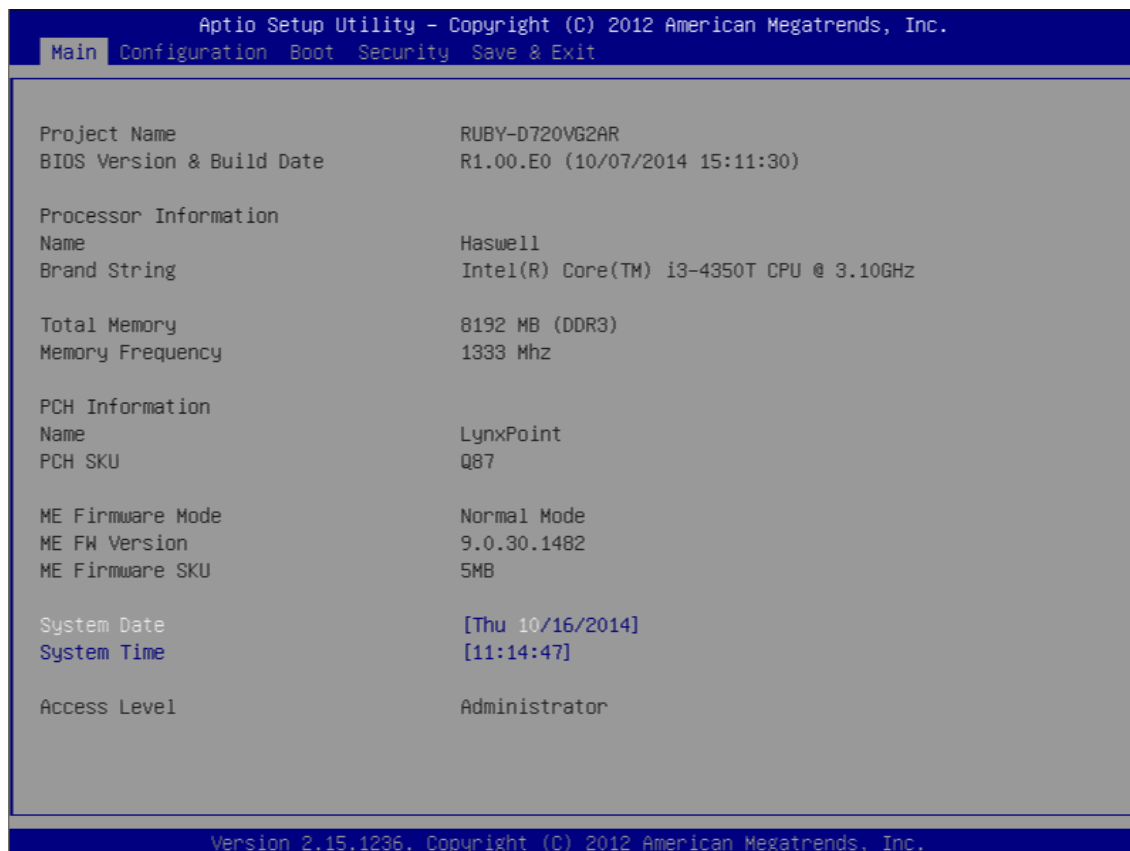
Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



4.2 Main

Use this menu for basic system configurations, such as time, date etc.



BIOS Information, Memory Information

These items show the firmware and memory specifications of your system. Read only.

System Date

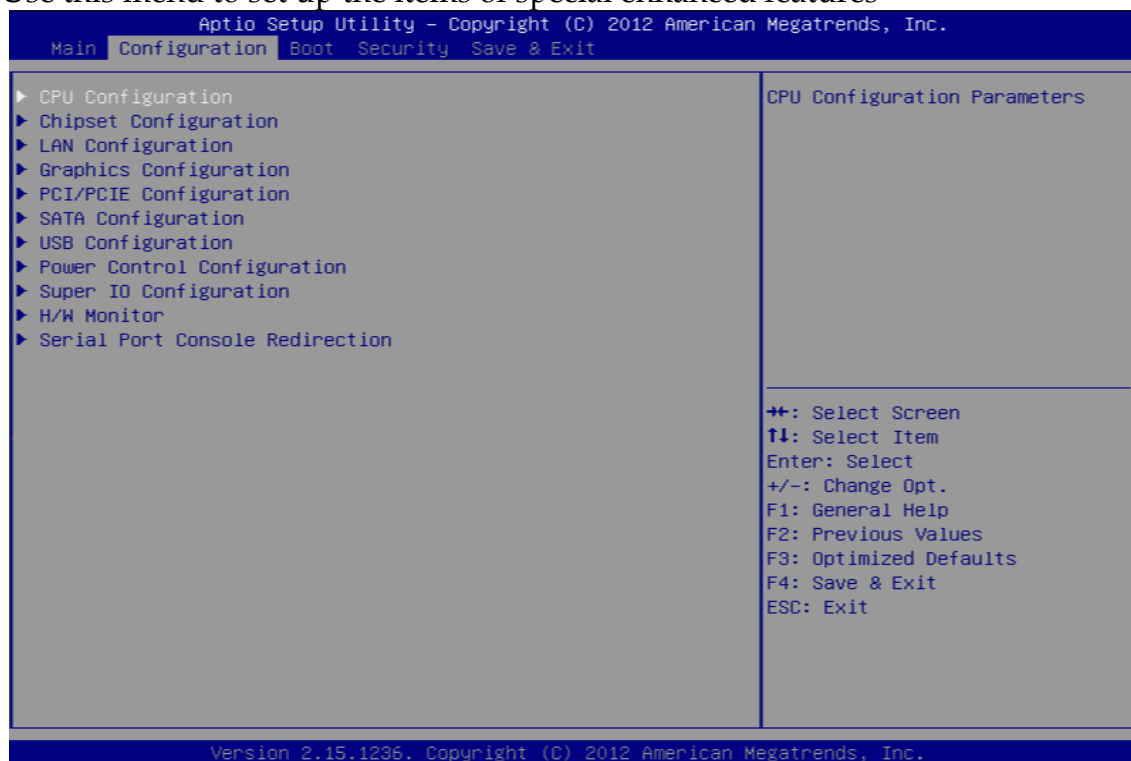
The date format is <Day>, <Month> <Date> <Year>. Use [+] or [-] to configure system Date.

System Time

The time format is <Hour> <Minute> <Second>. Use [+] or [-] to configure system Time.

4.3 Configuration

Use this menu to set up the items of special enhanced features



CPU configuration

CPU Configure the specific active core(s) and advanced processor management technologies.



Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When disabled only one thread per enabled core is enabled.

The choice: Disabled. Enabled.

Active Processor Cores

Number of cores to enable in each processor package.

The choice: All, 1.

Intel Virtualization Cores

When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology.

The choice: Disabled. Enabled.

EIST

Enable/Disable Intel Speed Step.

The choice: Disabled. Enabled.

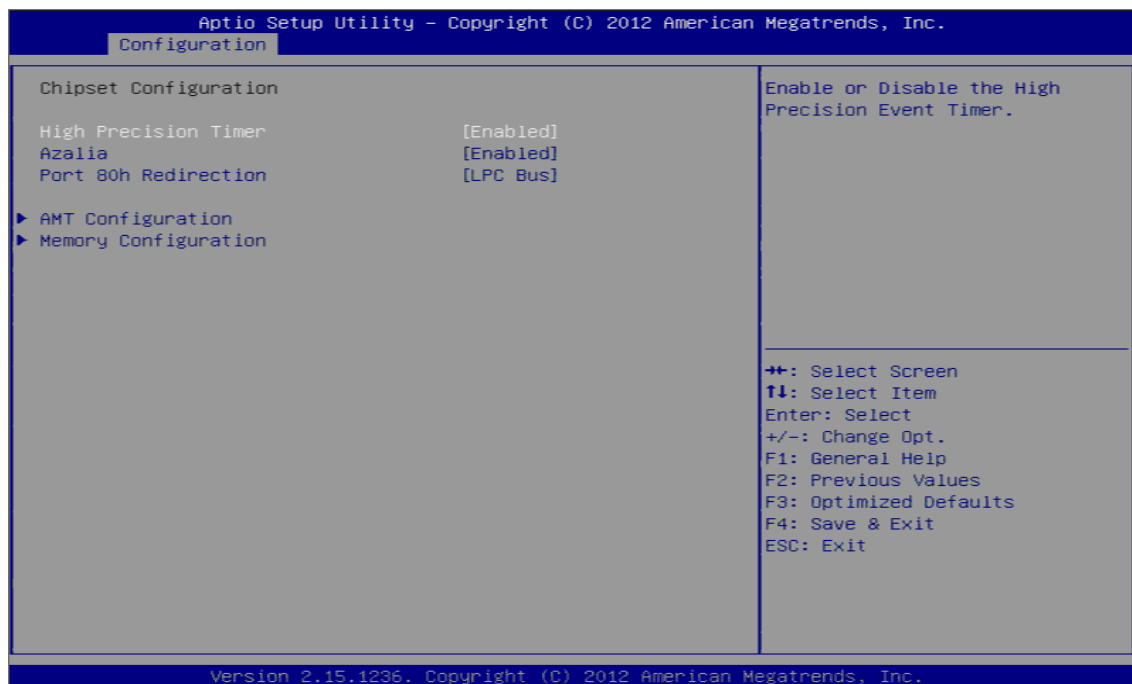
C-States

Enable or Disable the CPU C-States.

The choice: Disabled. Enabled.

Chipset Configuration

Configuration Chipset feature.



High Precision Timer

Enable or Disable the High Precision Event Timer.

The choice: Disabled. Enabled.

Azalia

Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled. Enabled = Azalia will be unconditionally Enabled.

The choice: Disabled. Enabled.

Port 80h Redirection

Control where the Port 80h cycles are sent. [LPC Bus] Forward I/O Port 80 to LPC. [PCIE Bus] Forward I/O Port 80 to PCIE Subtractive device.

The choice: LPC Bus, PCIE Bus.

AMT Configuration

Configure Intel Active Management Technology Parameters.

Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc.	
Configuration	
<p>AMT Configuration</p> <p>Intel AMT [Enabled]</p> <p>Un-Configure ME [Disabled]</p> <p>Disable ME [Disabled]</p>	<p>Enable/Disable Intel (R) Active Management Technology BIOS Extension.</p> <p>Note : iAMT H/W is always enabled.</p> <p>This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device</p> <hr/> <p> ++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit </p>
Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.	

Intel AMT

Enable/Disable Intel (R) Active Management Technology BIOS Extension Note: iAMT H/W is always enabled. The option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

The choice: Disabled. Enabled.

Un-Configure ME

OEMF lag Bit 15: Un-Configure ME without password.

The choice: Disabled. Enabled.

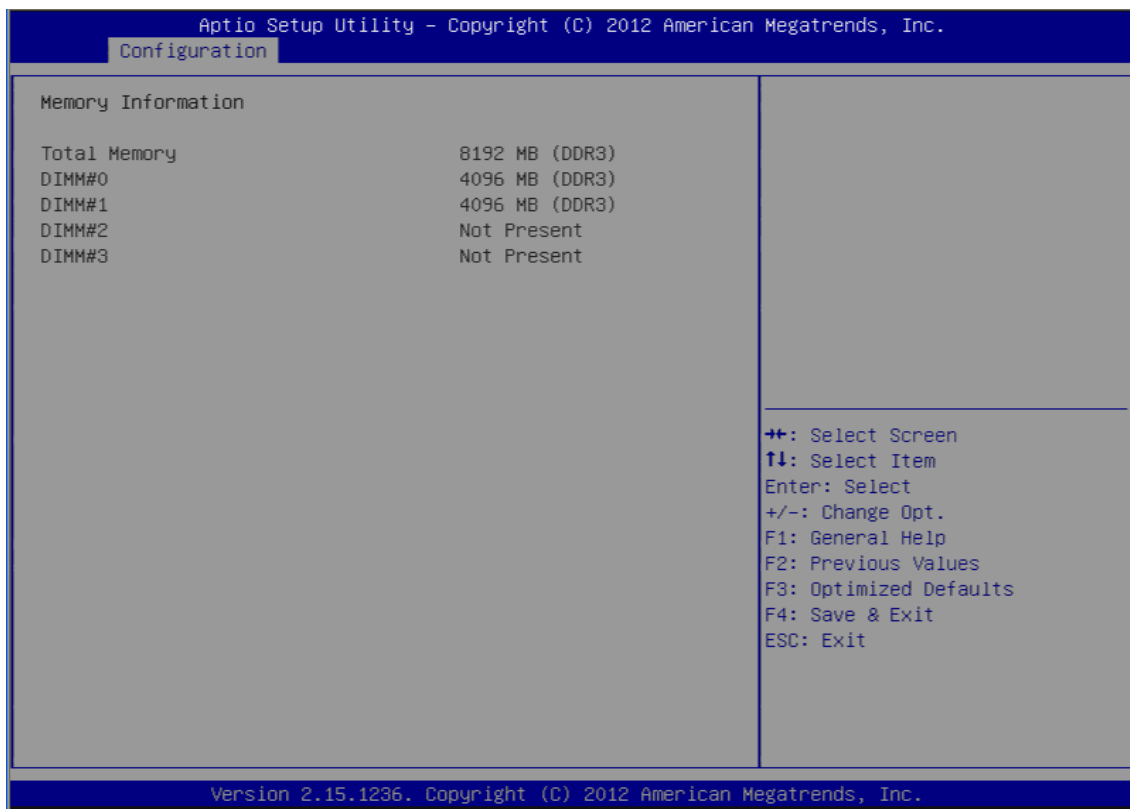
Disable ME

Set ME to Soft Temporary Disabled.

The choice: Disabled. Enabled.

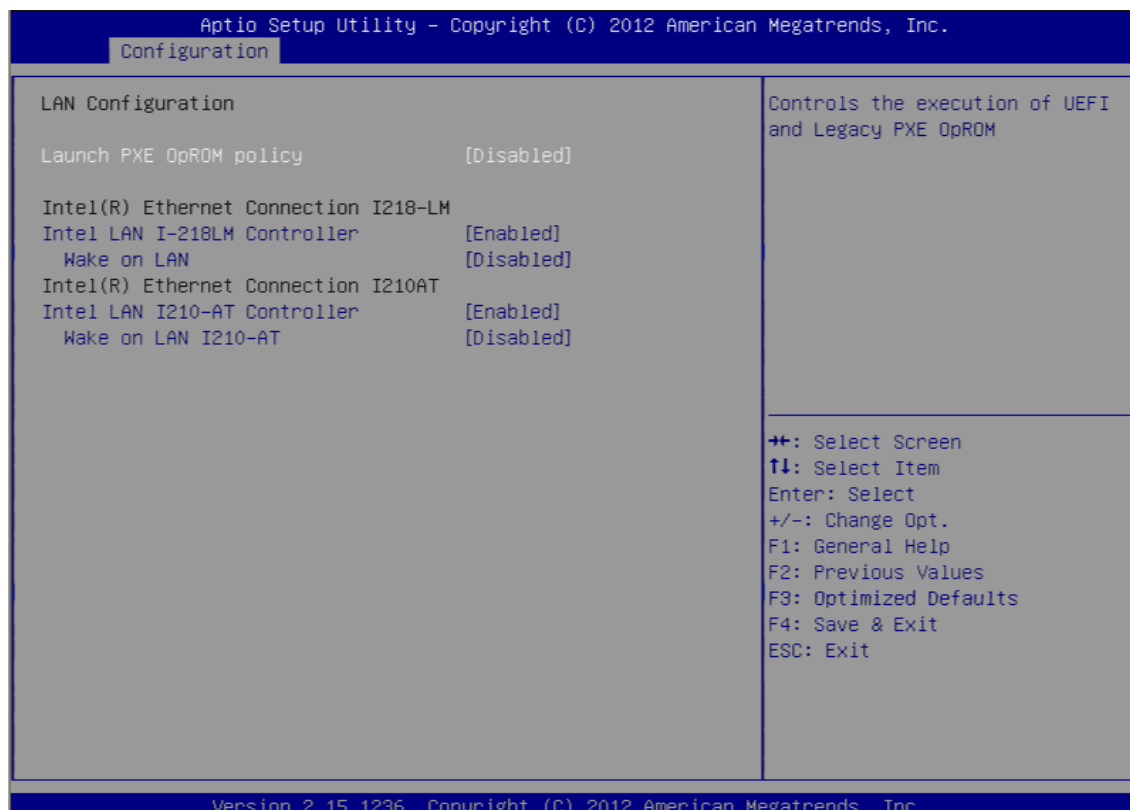
Memory Information

Memory Information Parameters.



LAN Configuration

Configuration on board LAN device.



Launch PXE OpROM policy

Controls the execution of UEFI and Legacy PXE OpROM.

The choice: Disabled. UEFI Only, Enabled.

Intel LAN I-218LM Controller

Enable or Disable onboard NIC.

The choice: Disabled. Enabled.

Wake on LAN

Enable or Disable integrated LAN to wake the system. (The wake On LAN cannot be disabled if ME is on at Sx state.)

The choice: Disabled. Enabled.

Intel LAN I-210-AT Controller

Enable or Disable onboard NIC.

The choice: Disabled. Enabled.

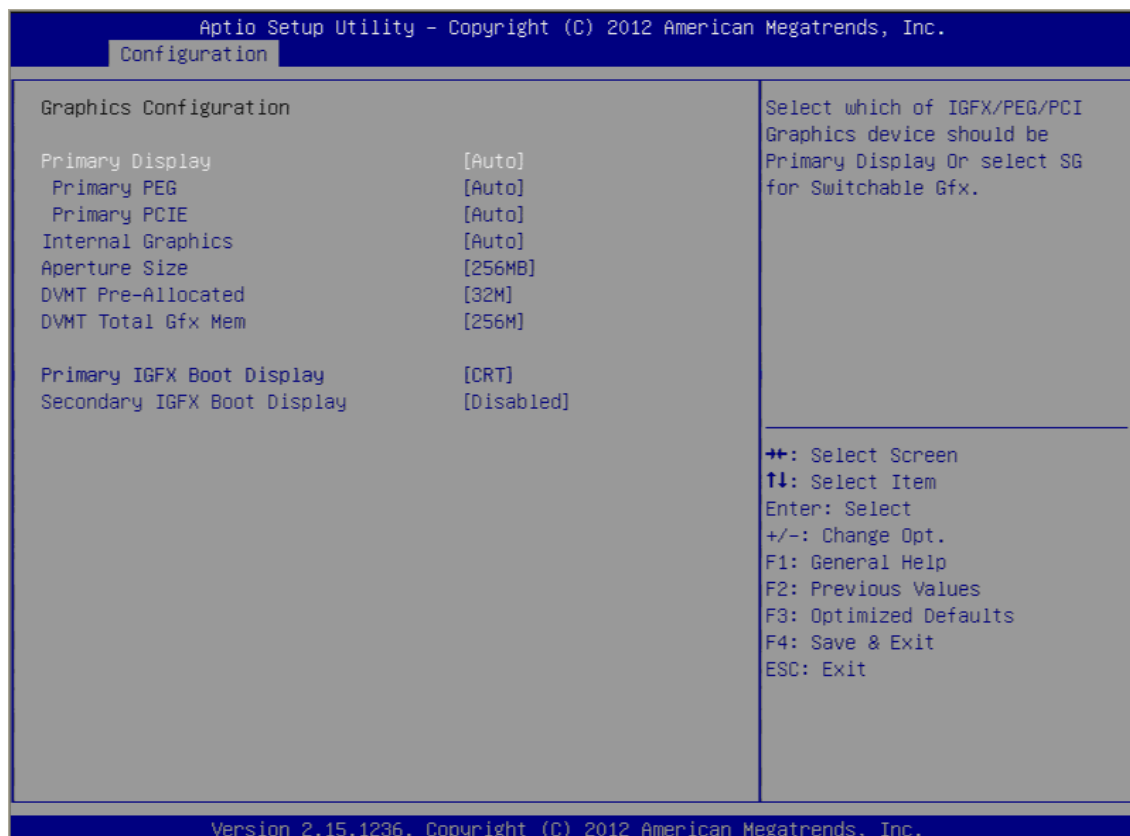
Wake on LAN I210AT

Enable or Disable integrated LAN to wake the system. (The wake On LAN cannot be disabled if ME is on at Sx state.)

The choice: Disabled. Enabled.

Graphic Configuration

Configure Graphics Setting.



Primary Display

Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for Switch able Gfx.

Choices: Auto, IGFX, PEG, PCI.

Primary PEG

Select PEG0/ PEG1/PEG2/PEG3 Graphics device should be Primary PEG.

Choices: Auto, PEG11, PEG12.

Primary PCIE

Select PCIE0/PCIE1/PCIE2/PCIE3/PCIE4/PCIE5/PCIE6/PCIE7 Graphics device should be Primary PCIE.

Choices: Auto, PCIE1, PCIE2, PCIE3, PCIE4, PCIE5, PCIE6, PCIE7.

Internal Graphics

Keep IGD Enabled based on the setup options.

Choices: Auto, Disabled, Enabled.

Aperture Size

Select the Aperture Size..

Choices: 128MB, 256MB, 512MB.

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the internal Graphic Device.

Choices: 32M, 64M, 96M, 128M, 160M, 192M, 224M, 256M, 288M, 320M, 352M, 384M, 416M, 448M, 480M, 512M, 1024M.

DVMT Total Gfx Mem

Select DVMT 5.0 Total Graphic Memory size used by the internal Graphic Device.

Choices: 128MB, 256MB, MAX.

Primary IGFX Boot Display

Select the Video Device which will be activated during POST. This has no effect if external graphics are present. Secondary will appear based on your Selection. VGA modes will be supported only on primary display.

Choices: CRT, DVI, HDMI.

Secondary IGFX Boot Display

Select Secondary Display Device.

Choices: Disabled, CRT, DVI, HDMI.

PCI/PCIE Configuration

PCI , PCI -X and PCI Express Setting.



PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

The choice: 32, 64, 96, 128, 160, 192, 224, 248 PCI Bus Clocks.

Maximum Payload

Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

The choice: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes.

Maximum Read Request

Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

The choice: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes.

CPU PCI Express Configuration

CPU PCI Express Configuration setting.

**PEG0 - Gen X**

Configure PEG0 B0:D0:F0 Gen1- Gen3.

Choices: Auto, Gen1, Gen2, Gen3.

PEG0 - ASPM

Control ASPM support for the PEG Device. This has no effect if PEG is not the currently active device.

Choices: Disabled, Auto, ASPM L0s, ASPM L1, ASPM L0sL1.

PEG1 - Gen X

Configure PEG1 B0:D0:F1 Gen1- Gen3.

Choices: Auto, Gen1, Gen2, Gen3.

PEG1 - ASPM

Control ASPM support for the PEG Device. This has no effect if PEG is not the currently active device.

Choices: Disabled, Auto, ASPM L0s, ASPM L1, ASPM L0sL1.

FEG2 - Gen X

Configure PEG2 B0:D0:F2 Gen1- Gen3.

Choices: Auto, Gen1, Gen2, Gen3.

PEG2 - ASPM

Control ASPM support for the PEG Device. This has no effect if PEG is not the currently active device.

Choices: Disabled, Auto, ASPM L0s, ASPM L1, ASPM L0sL1.

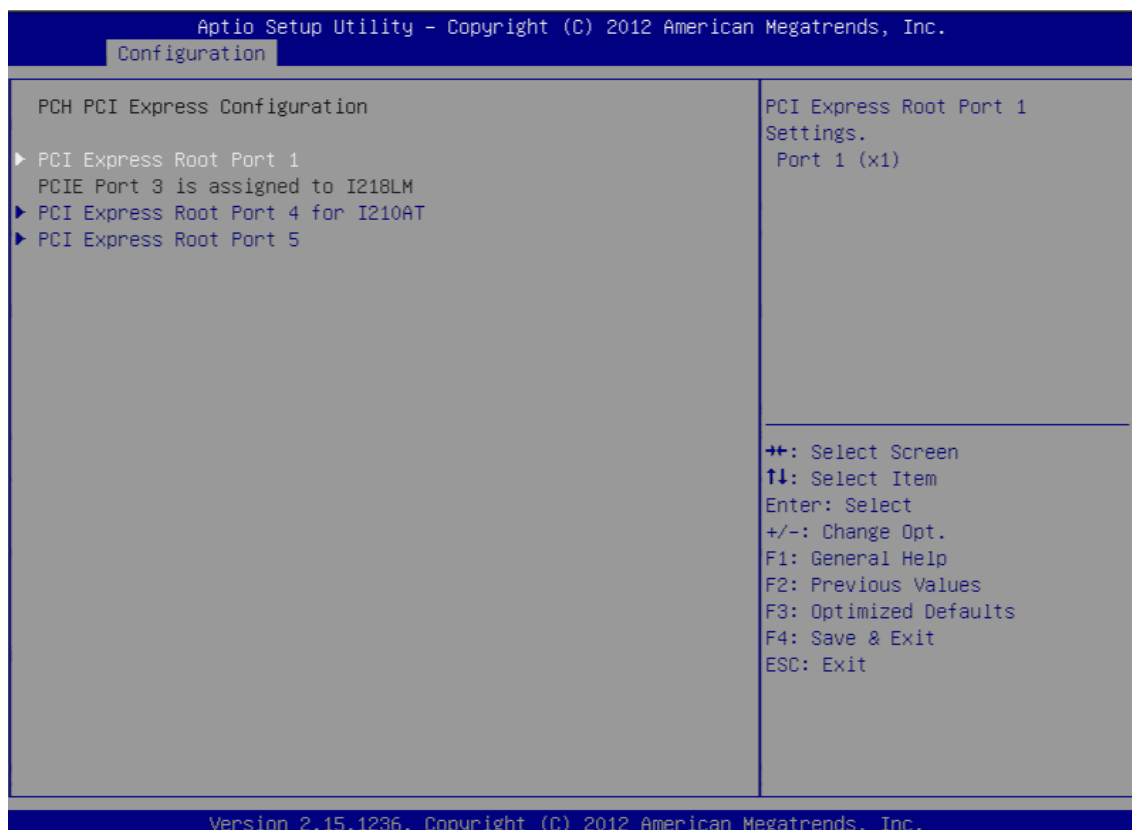
Enable PEG

To enable or disable the PEG.

Choices: Disabled, Enabled, Auto.

PCH PCI Express Configuration

PCH PCI Express Configuration setting.



PCI Express Root Port 1

PCI Express Root Port 1 Setting. Port 1(X1)



PCI Express Root Port 1

Control the PCI Express Root Port.

Choices: Disabled, Enabled.

ASPM

PCI Express Active State power Management settings.

Choices: Disabled, L0s, L1, L0sL1, Auto.

PCIe Speed

Select PCI Express Port Speed.

Choices: Auto, Gen1, Gen2.

PCI Express Root Port 4 for I210AT
 PCI Express Root Port 4 Setting. Port 1(X1)



Intel LAN I210-AT Controller
 Enable or Disable onboard NIC.

The choice: Disabled. Enabled.

ASPM
 PCI Express Active State power Management settings.

Choices: Disabled, L0s, L1, L0sL1, Auto.

PCIe Speed
 Select PCI Express Port Speed.

Choices: Auto, Gen1, Gen2.

PCI Express Root Port 5

PCI Express Root Port 5 Setting. Port 5 (x4), Ports 6-8 (disabled)



PCI Express Root Port 5

Control the PCI Express Root Port.

Choices: Disabled, Enabled.

ASPM

PCI Express Active State power Management settings.

Choices: Disabled, L0s, L1, L0sL1, Auto.

PCIe Speed

Select PCI Express Port Speed.

Choices: Auto, Gen1, Gen2.

PCI Express Root Port 6

PCI Express Root Port 6 Setting.



PCI Express Root Port 6

Control the PCI Express Root Port.

Choices: Disabled, Enabled.

ASPM

PCI Express Active State power Management settings.

Choices: Disabled, L0s, L1, L0sL1, Auto.

PCIe Speed

Select PCI Express Port Speed.

Choices: Auto, Gen1, Gen2.

PCI Express Root Port 7

PCI Express Root Port 7 Setting.



PCI Express Root Port 7

Control the PCI Express Root Port.

Choices: Disabled, Enabled.

ASPM

PCI Express Active State power Management settings.

Choices: Disabled, L0s, L1, L0sL1, Auto.

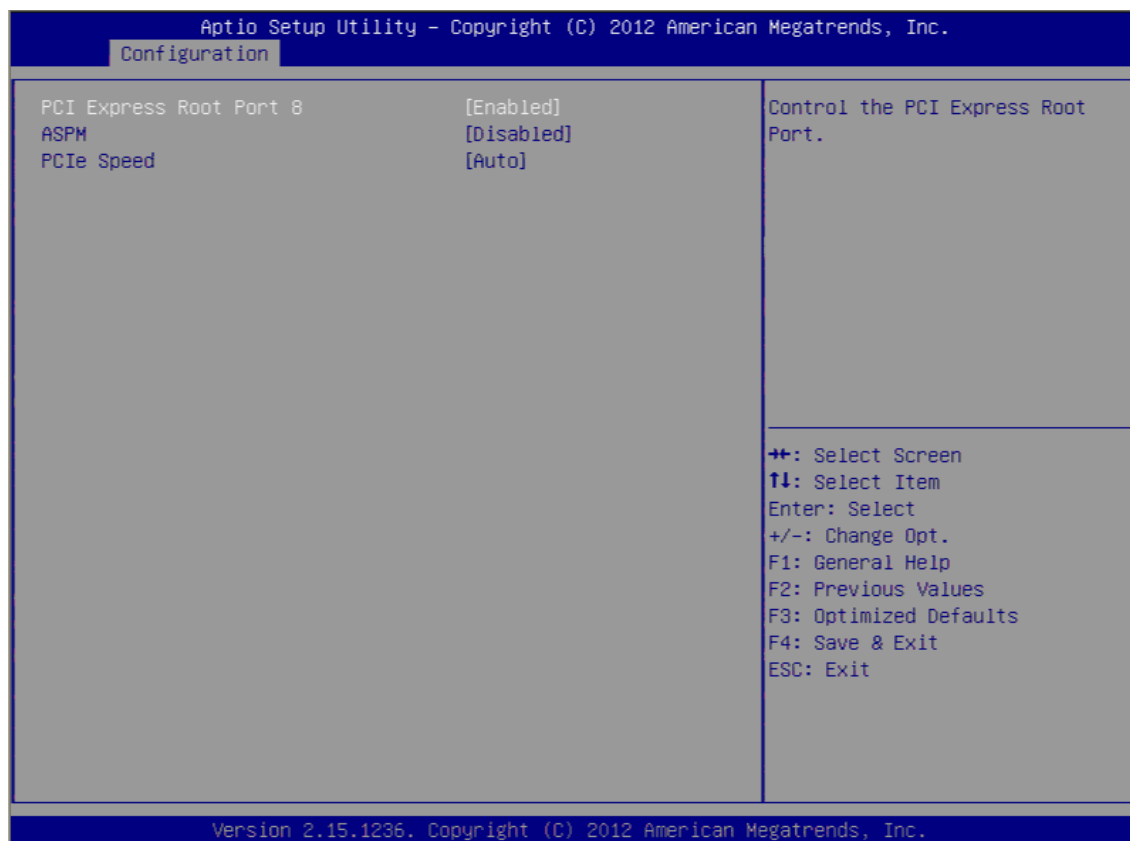
PCIe Speed

Select PCI Express Port Speed.

Choices: Auto, Gen1, Gen2.

PCI Express Root Port 8

PCI Express Root Port 8 Setting.



PCI Express Root Port 8

Control the PCI Express Root Port.

Choices: Disabled, Enabled.

ASPM

PCI Express Active State power Management settings.

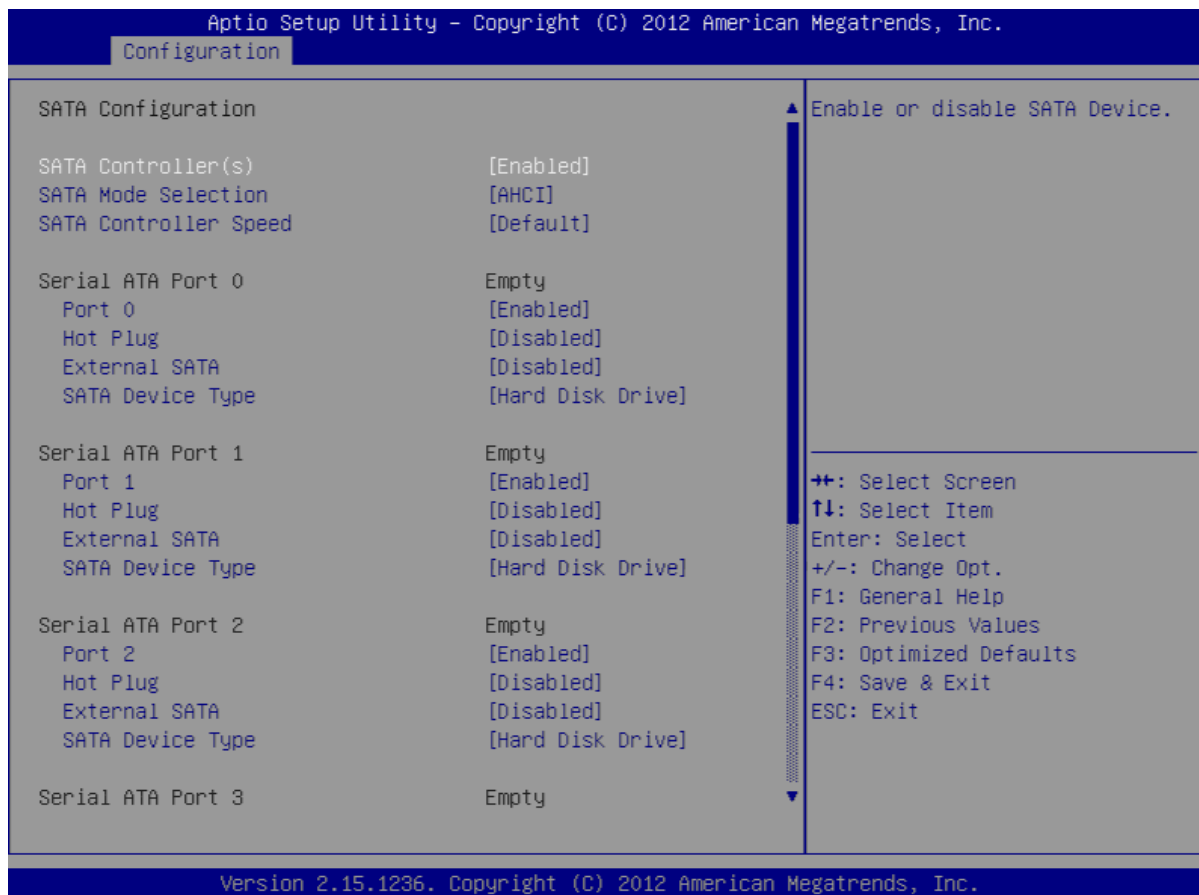
Choices: Disabled, L0s, L1, L0sL1, Auto.

PCIe Speed

Select PCI Express Port Speed.

Choices: Auto, Gen1, Gen2.

SATA Configuration
SATA device Options setting.



SATA Controller (s)

Enable or Disable SATA Device.

Choices: Disabled, Enabled.

SATA Mode

Determines how SATA controllers (s) operate.

Choices: Disabled, IDE, AHCI, RAID.

SATA Controller Speed

Indicates the maximum speed the SATA controller can support.

Choices: Default, Gen1, Gen2, Gen3.

Serial ATA Port 0 - Serial ATA Port 5

Display the identity of the device attached.

Choices: Empty.

Port 0 – Port 5

Enabled or Disabled SATA Port.

Choices: Disabled, Enabled.

Hot Plug

Designates this port as Hot Pluggable.

Choices: Disabled, Enabled.

External SATA

External SATA Support.

Choices: Disabled, Enabled.

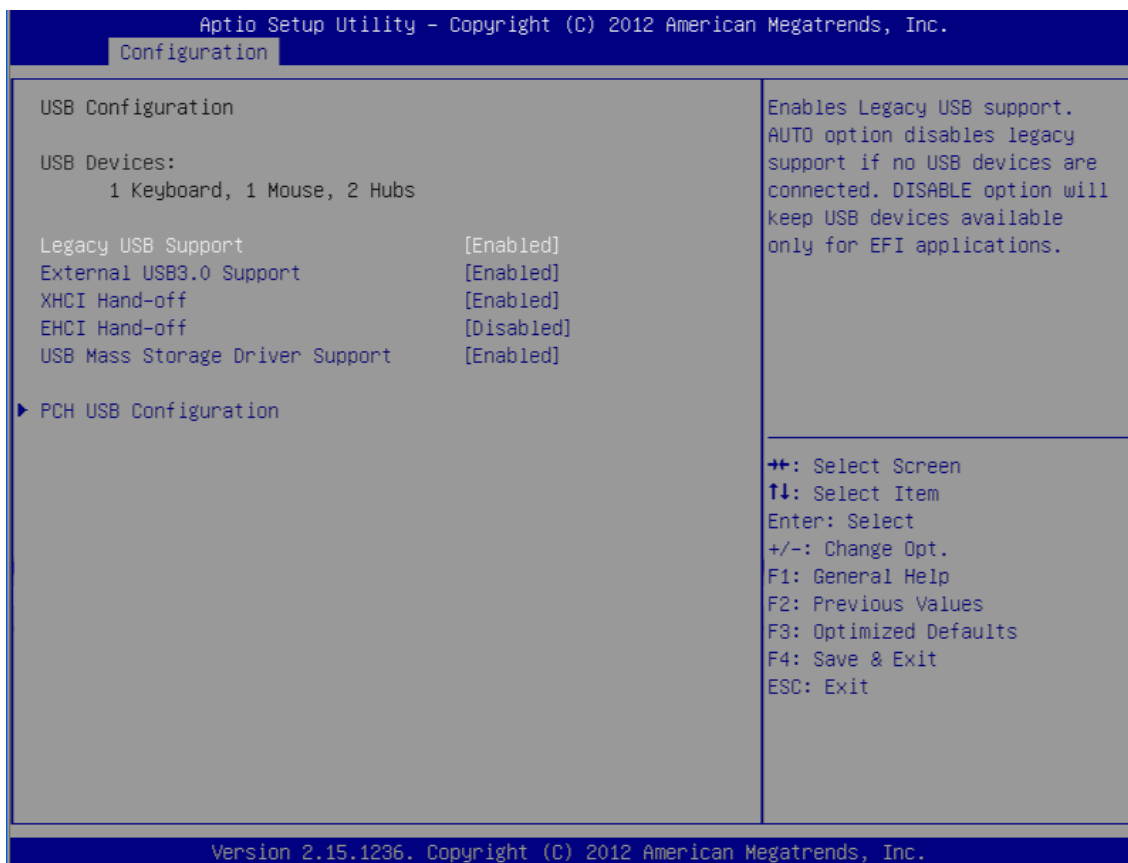
SATA Device Type

Identify the SATA port is connected to solid state Drive or Hard Disk Driver.

Choices: Hard Disk Driver, Solid State Driver.

USB Configuration

USB Configuration Parameters.



Legacy USB Support

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

Choices: Enabled, Disabled, Auto.

External USB3.0 Support

External Enable/Disable USB3.0 (XHCI) Controller support.

Choices: Enabled, Disabled.

XHCI Hand-off

This is a workaround for Oses without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

Choices: Enabled, Disabled.

EHCI Hand-off

This is a workaround for Oses without EHCI hand-off support. The XHCI ownership change should be claimed by EHCI driver.

Choices: Enabled, Disabled.

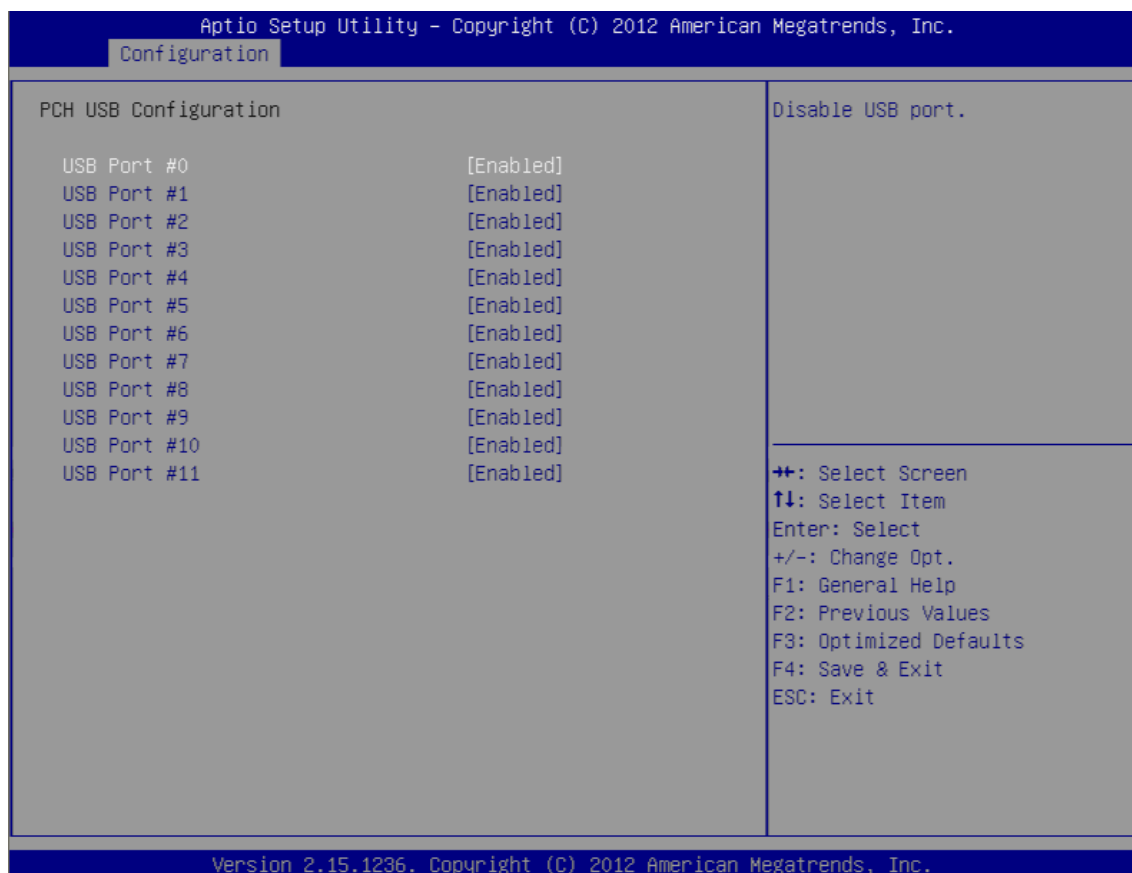
USB Mass storage Driver Support

Enable/Disable USB Mass storage Driver Support.

Choices: Enabled, Disabled.

PCH USB Configuration

PCH USB Configuration settings.



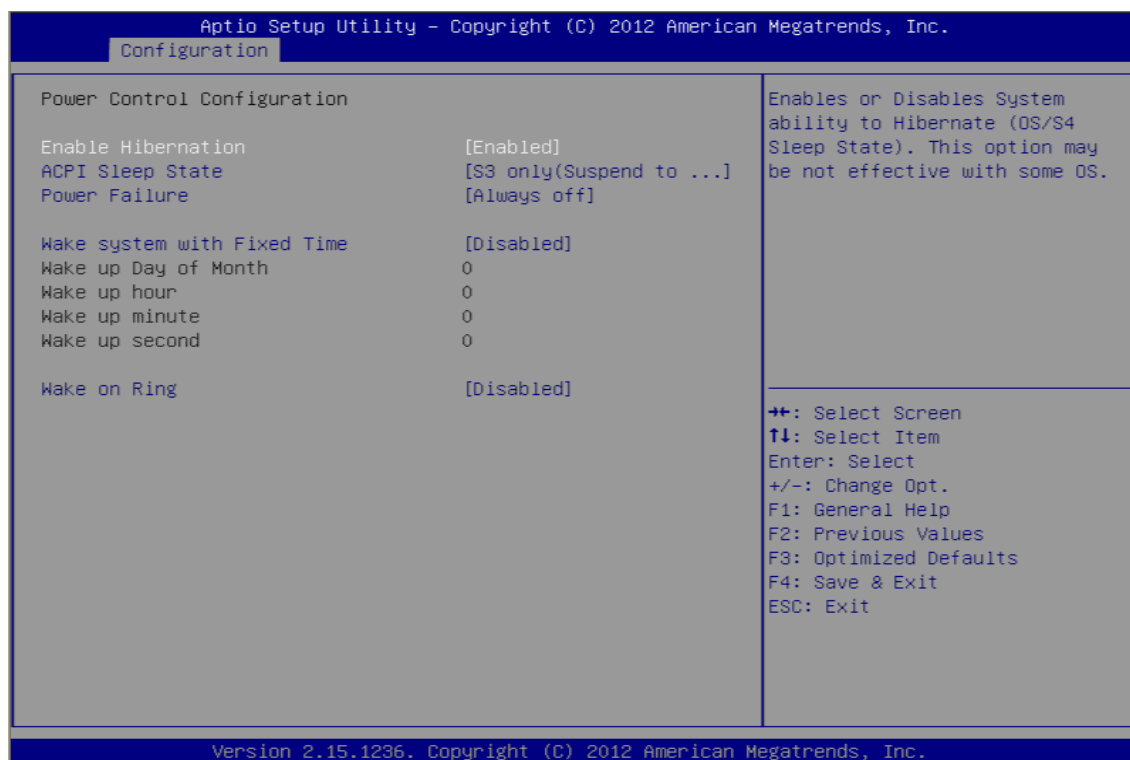
USB Ports #0 - USB Ports #11

Disable USB ports.

Choices: Enabled, Disabled.

Power Control Configuration

System Power Control Configuration Parameters.



Enable Hibernation

Enable or disable System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

Choices: Disabled, Enabled.

ACPI Sleep State

Select ACPI sleep state the system will enter when the SUSPEND button is pressed.

Choices: S3 only (Suspend to RAM)

Power Failure

Power Failure Enabled.

Choices: Keep last. State, Always on, Always off.

Wake system with Fixed Time

Enable or disable system wake on alarm event. When enabled, System will wake on the hr::min::sec specified.

Choices: Disabled, Enabled

Wake up Day of Month

Select 0 for daily system wake up 1-31 for which day of the month that you would like the system to wake up.

Choices: 1-31.

Wake up hour

Select 0-23 for example enters 3 for 3am and 15 for 3pm.

Choices: 0-23.

Wake up minute

0-59.

Choices: 0-59.

Wake up second

0-59.

Choices: 0-59.

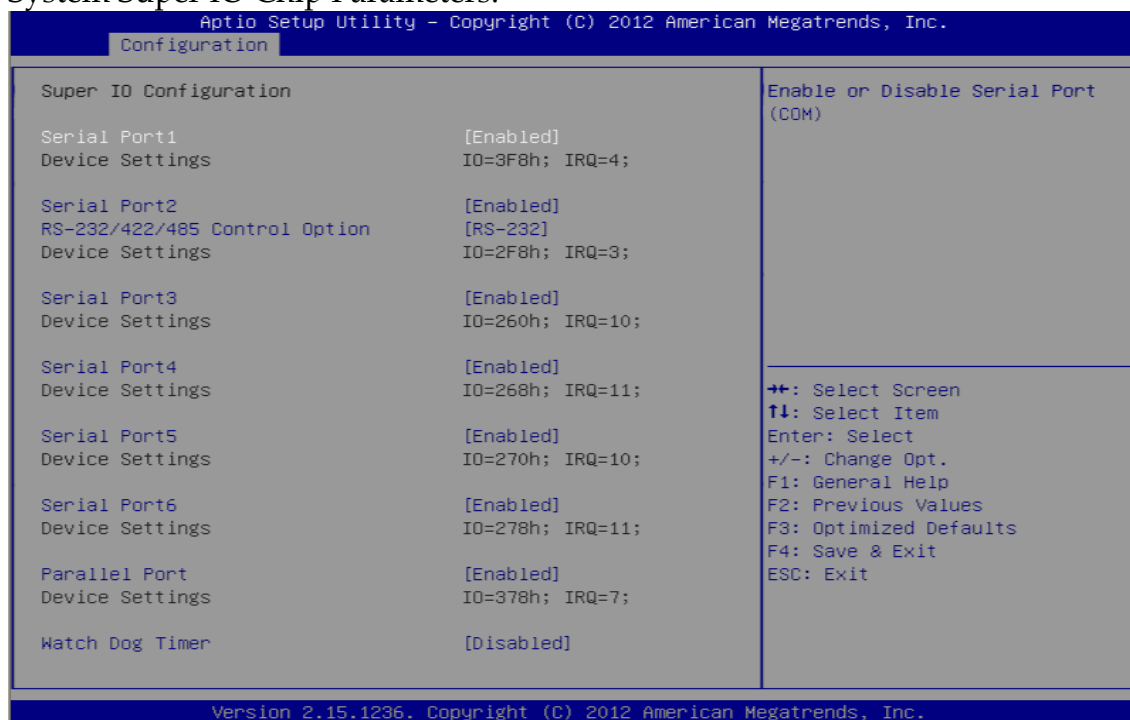
Wake on Ring

Enable or disable system wake on Ring from S5 mode.

Choices: Disabled, Enabled.

Super IO Configuration

System Super IO Chip Parameters.



Serial Port 1

Enable or Disable Serial Port (COM) IO=3F8H; IRQ=4.

Choices: Disabled, Enabled.

Serial Port 2

Enable or Disable Serial Port (COM) IO=2F8H; IRQ=3.

Choices: Disabled, Enabled.

RS-232/422/485 Control Option (Serial Port 2 only)

Serial Port 2 RS-232/422/485 Control Option.

Choices: RS-232, RS-422, RS-485, Loopback.

Serial Port 3

Enable or Disable Serial Port (COM) IO=260H; IRQ=10.

Choices: Disabled, Enabled.

Serial Port 4

Enable or Disable Serial Port (COM) IO=268H; IRQ=11.

Choices: Disabled, Enabled.

Serial Port 5

Enable or Disable Serial Port (COM) IO=270H; IRQ=10.

Choices: Disabled, Enabled.

Serial Port 6

Enable or Disable Serial Port (COM) IO=278H; IRQ=11.

Choices: Disabled, Enabled.

Parallel Port

Enable or Disable Parallel Port (LPT/LPTE) IO=378H; IRQ=7.

Choices: Disabled, Enabled.

Watch Dog Timer Select

Set watchdog timer value.

Choices: Disabled, Enabled.

Timer value

Set WDT Timer value Seconds/Minutes.

Choices: 10-255 Seconds.

Hardware Monitor

Monitor hardware status.



Smart CPU Fan Control

Fan1 Start Temperature.

Choices: Disabled, Enabled.

Smart CPU Fan Start

Fan will work when temperature higher this limit.

Choices: 0 - 127.

CPU Fan Full Speed

Fan Full Speed temperature.

Choices: 0 - 127.

Smart CPU Fan2 Control

Fan2 Start Temperature.

Choices: Disabled, Enabled.

Smart CPU Fan2 Start

Fan will work when temperature higher this limit.

Choices: 0 - 127.

CPU Fan2 Full Speed

Fan Full Speed temperature.

Choices: 0 - 127.

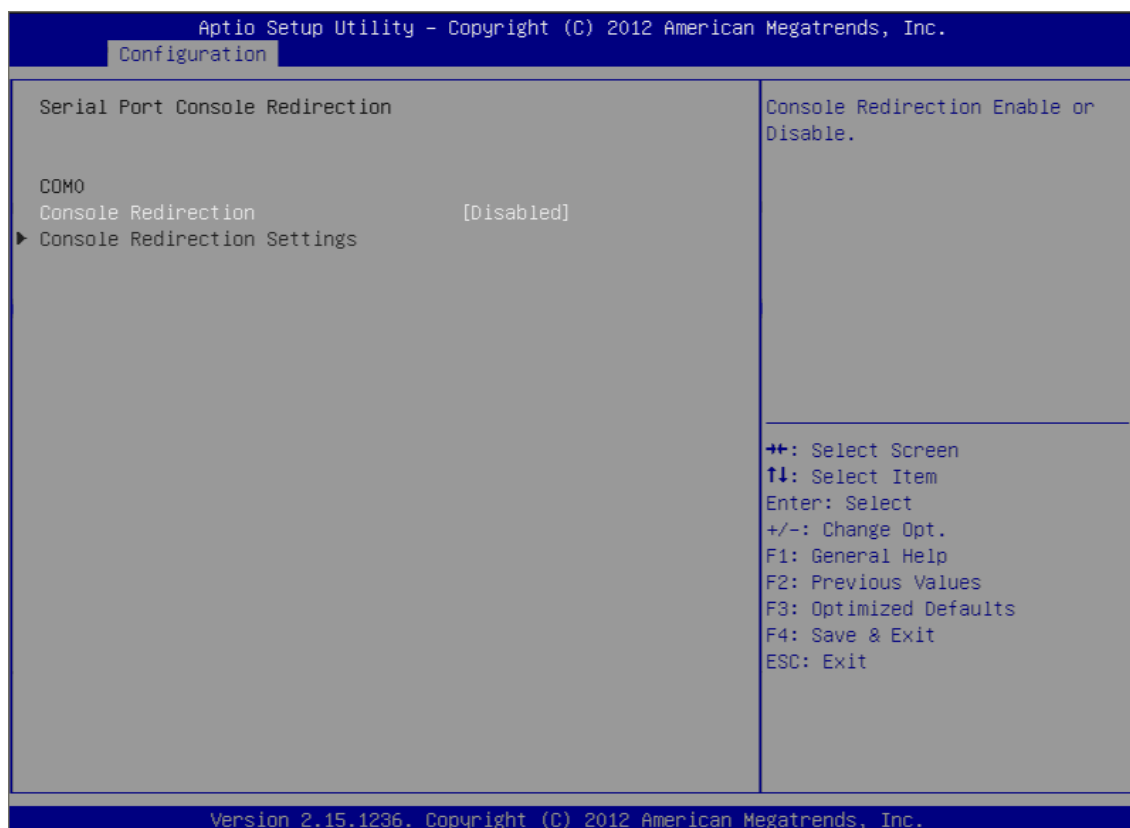
Case Open Warning

Support Case Open Warning Beep.

Choices: Disabled, Enabled.

Serial Port Console Configuration

Serial port Console Redirection.



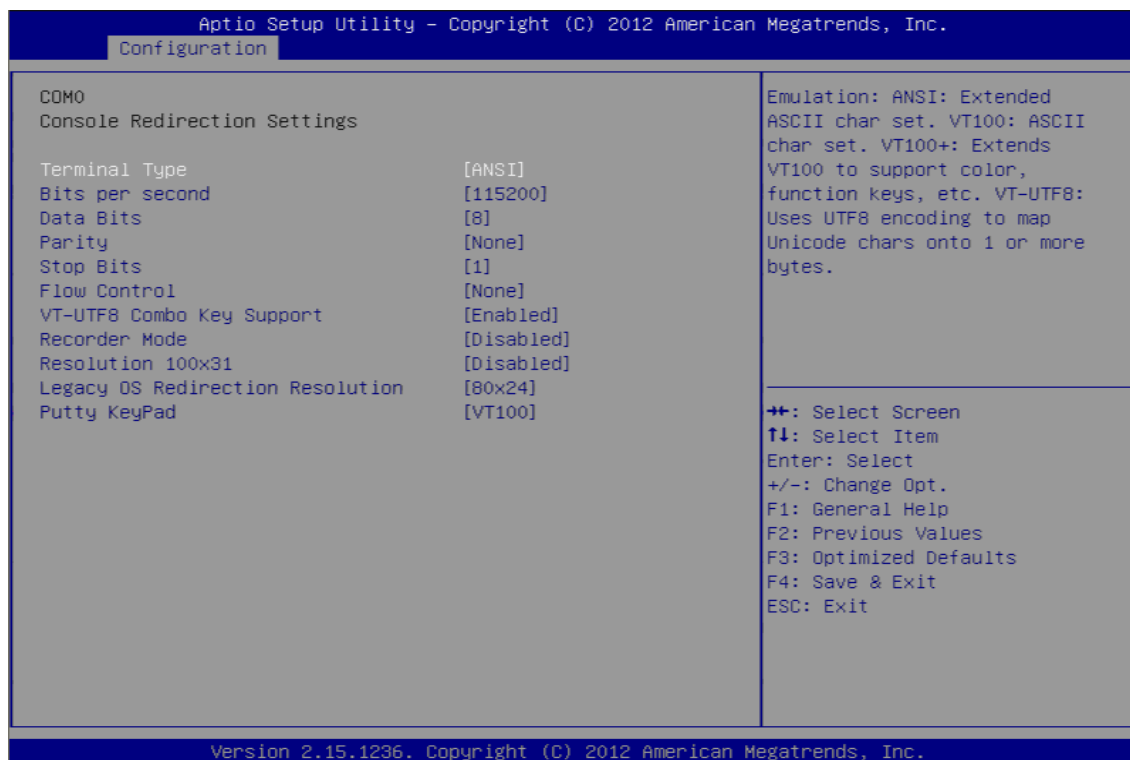
Console Redirection

Console Redirection Enable/Disable.

Choices: Enabled, Disabled

Console Redirection Settings

The Setting specify how the host computer and the remote computer (which the user ie using) will exchange data. Both computers should have the same or compatible settings.



Terminal Type

Emulation : ANSI : Extended ASCII char set. VT100 : ASCII char set. V100+ : Extends V100 to support color, function keys, ect. VT-UTF8 : user UTF8 encoding to map unicode chars onto 1 or more bytes.

Choices: VT100, VT100+, VT-UTF8, ANSI.

Bits per second

Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

Choices: 9600, 19200, 38400, 57600, 115200.

Data Bits

Data Bits.

Choices: 7, 8.

Parity

A parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if num of 1 'S in the data bits is Odd. Mark : parity nit is always 1. Space : parity bit is always 0. Mark and Space parity do not allow for error detection.

Choices: None, Even, Odd, Mark, Space.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicate the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

Choices: 1, 2.

Flow control

Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to atop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardward flow control uses two wires to send start/stop signals.

Choices: None, Hardware RTS/CTS.

VT-UTFB Combo Key Support

Enabled VT-UTF8 Combination key Support for ANSI/VT100 teminals.

Choices: Disabled, Enabled.

Recorder Mode

On this mode enabled only text will be send. This is to capture terminal data.

Choices: Disabled, Enabled.

Resolution 100x31

Enabled or Disabled extended terminal resolution.

Choices: Disabled, Enabled.

Legacy OS Redirection Resolution

On Legacy OS, the Number of Rows and Columns supported redirection.

Choices: 80X24, 80X25.

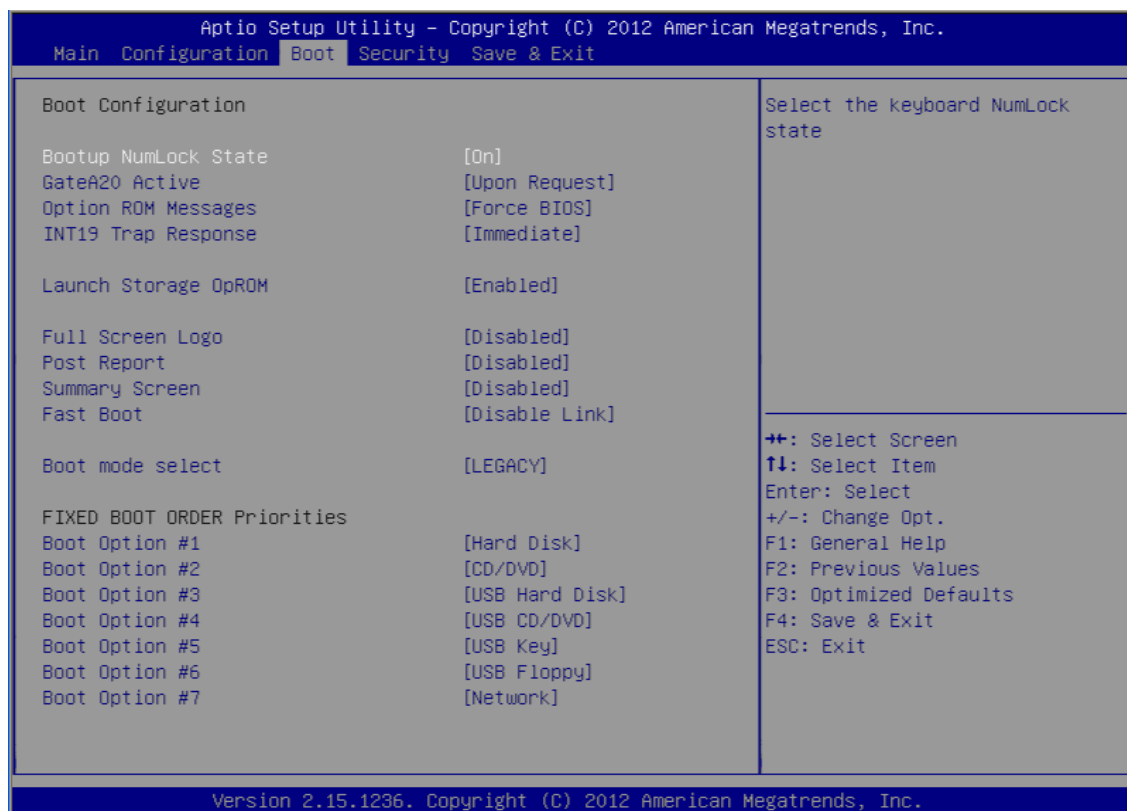
Putty keyPad

Select Functionkey and keyPad on Putty.

Choices: VT100, LINUX, XTERMR6, SCO, ESCN, VT400.

4.4 Boot

Use this menu to specify the priority of boot devices.



Bootup NumLock state

Select the keyboard NumLock state.

Choices: On, Off.

GateA20 Active

UPON REQUEST - GA20 can be disabled using BIOS services. ALWAYS - do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Choices: Upon Request, Always.

Option ROM Messages

Set display mode for Option ROM.

Choices: Force BIOS, Keep Current.

INT19 Trap Response

BIOS reaction on INT19 trapping by Option ROM: IMMEDIATE – execute the trap right away; POSTPONED – execute the trap during legacy boot.

Choices: Immediate, Postponed.

Launch Storage OpROM

Controls the of storage OpROM Enabled / Disabled..

Choices: Disabled, Enabled.

Full Screen Logo

Enables or Disables Quiet Boot option and Full screen Logo.

Choices: Disabled, Enabled.

Post Report

Post Report Support Enabled/Disabled.

Choices: Disabled, Enabled.

Summary Screen

Summary Screen Support Enabled/Disabled.

Choices: Disabled, Enabled.

Fast Boot

Enables or Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Choices: Disable Link, Enabled.

Boot mode select

Select boot mode LEGACY/UEFI.

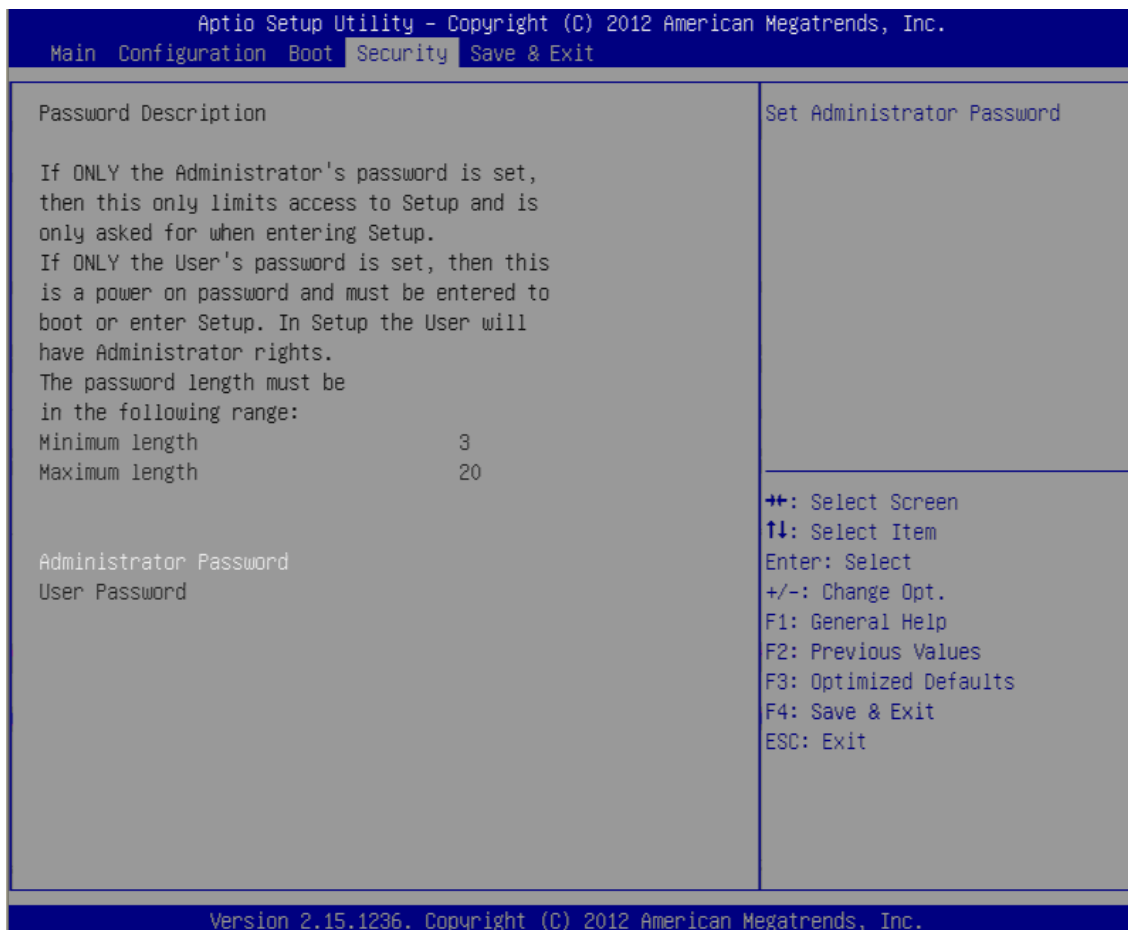
Choices: LEGACY, UEFI.

Boot Option #1-7

Sets the system boot order

Choices: Hard Disk, CD/DVD, USB Hard Disk, USB CD/DVD, USB Key, USB Floppy, Network, Disabled.

4.5 Security



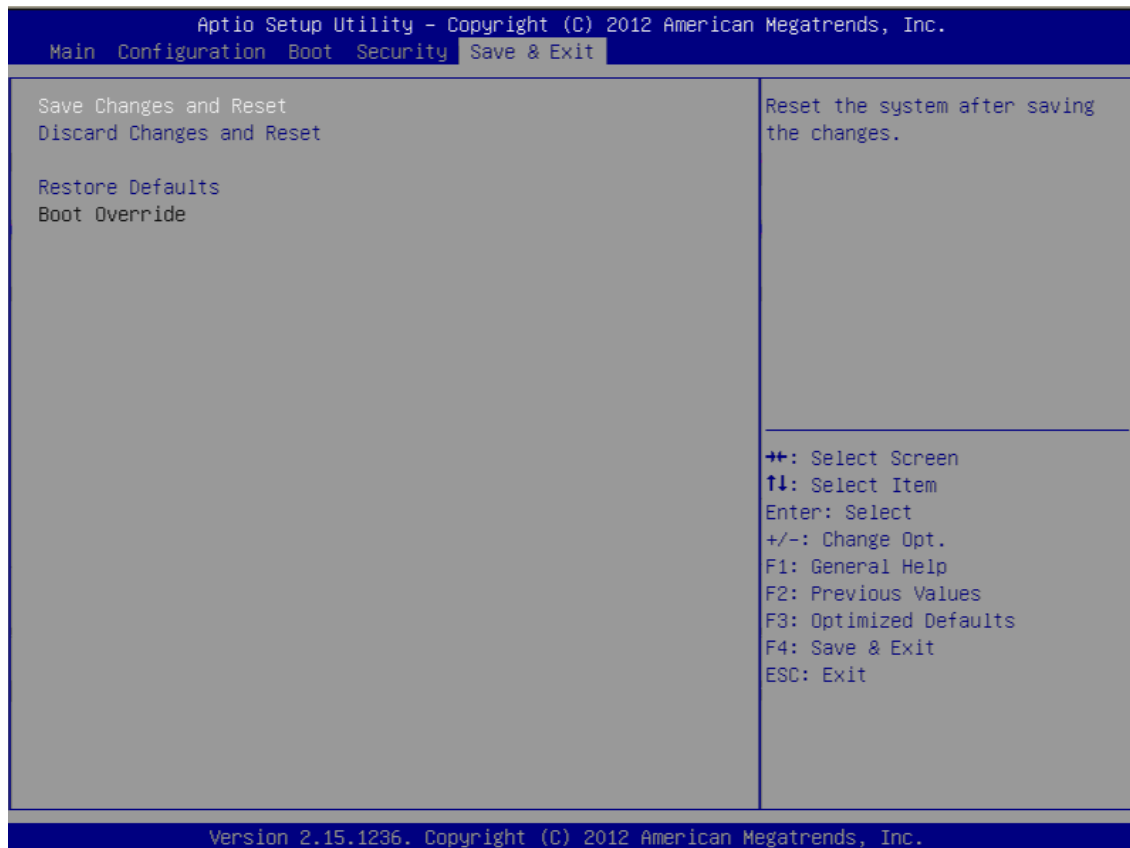
Administrator Password

Set Setup Administrator Password

User Password

Set User Password

4.6 Save & Exit



Save Changes and Reset

Reset the system after saving the changes.

Pressing <Enter> on this item asks for confirmation: Save configuration and reset.

Discard Changes and Exit

Reset system setup without saving any changes.

Restore Defaults

Restore/Load Default values for all the setup options.

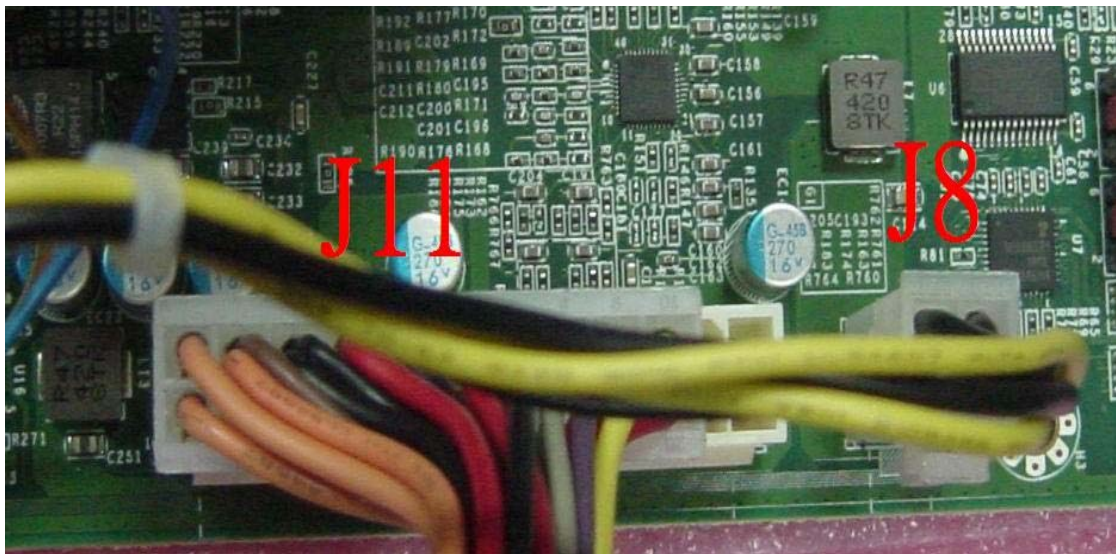
Chapter 5

Troubleshooting

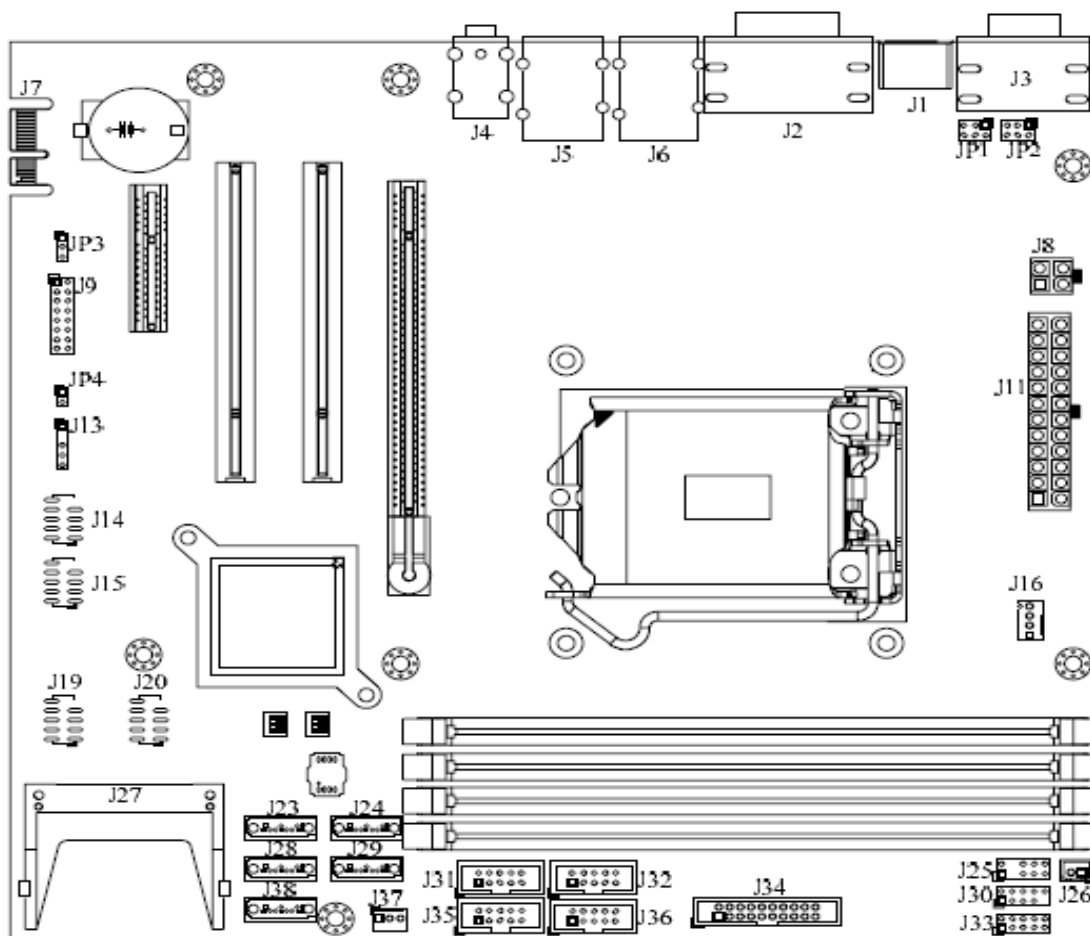
This chapter provides a few useful tips to quickly get RUBY-D720 running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

ATX Power Setting

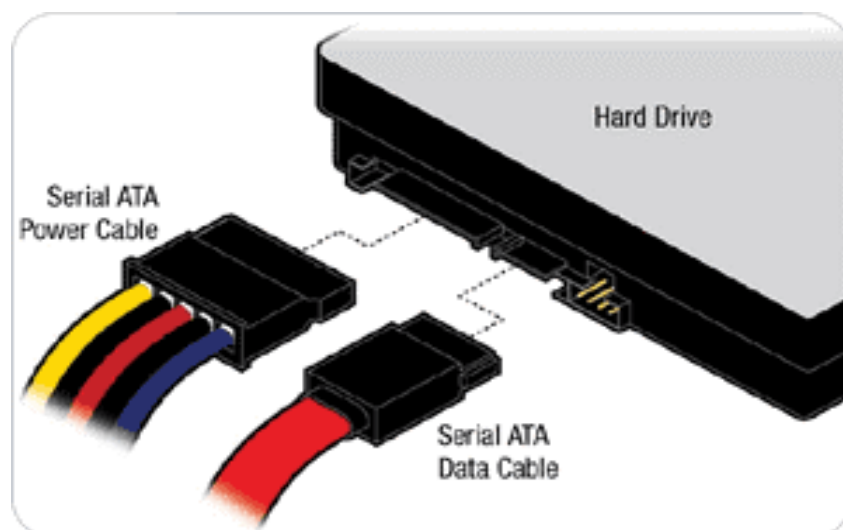


RUBY-D720 supports ATX. Therefore, there is no other setting that really needs to be set up. However, there are only two connectors that must be connected – J8 (4 pins CPU +12V main power connector) & J11 (24 pins ATX Power Connector)



Serial ATA Hard Disk Setting for IDE/RAID/AHCI

Unlike IDE bus, each Serial ATA channel can only connect to one SATA hard disk at a time; there are total six connectors, SATA1~6 port. The installation of Serial ATA is simpler and easier than IDE, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation. All you need to operate IDE, RAID (0/1/5/10) and AHCI application for system, please follow up setting guide in BIOS setup utility



5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power. CPU, CPU Fan, 204-pin DDR3 memory, keyboard, mouse, floppy drive, SATA hard disk, DVI-I connector, but it only can use on DVI-D function, doesn't support DVI-I function, device power cables,

ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with RUBY-D720, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the BIOS setup menu, please switch to the "Save & Exit" page then select "Restore Defaults", press "Enter" and select "Yes" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the COM1/COM2 ports, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

Disable COM1 serial port to release IRQ #4

Disable COM2 serial port to release IRQ #3

Etc...

A quick review of the basic IRQ mapping is given below for your reference.

Interrupt Request Lines IRQ		
IRQ#	<i>Current Use</i>	<i>Default Use</i>
IRQ 0	Unused	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	【Unassigned】	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	【Unassigned】	Usable IRQ

IRQ 6	System ROM	Diskette Event
IRQ 7	Unused	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	【Unassigned】	Usable IRQ
IRQ 10	【Unassigned】	Usable IRQ
IRQ 11	【Unassigned】	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	【Unassigned】	Usable IRQ

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

5.3 FAQ

Installation Problem

Question: How to update the BIOS file of the RUBY-D720?

Answer:

1. Please visit our [Portwell Download Center](http://www.portwell.com.tw/support/download_center.php) as below hyperlink:

http://www.portwell.com.tw/support/download_center.php

But you must register an account first. (The E-Mail box should be an existing Company email address that you check regularly.)

<http://www.portwell.com.tw/member/newmember.php>

2. Input your User name and password to log in the download center.

3. Select the **“Search download”** to input the keyword **“RUBY-D720”**.

4. Find the **“BIOS ”** page to download the ROM file and flash utility.

5. Execute the zip file to root of the bootable USB pen drive. You can get the **“Readme.txt”**, **“Update.efi”** two files.

Note:

Please visit our Portwell Download Center to get the Catalog, User manual, BIOS, and O/S drivers.

http://www.portwell.com.tw/support/download_center.php

If you have other additional technical information or request which is not covered in this manual, please fill in the technical request form as below hyperlink.

http://www.portwell.com.tw/support/download_center.php

We will do our best to provide a suggestion or solution for you.

Thanks.