PCOM-C701_ZR1

Jumper Setting

Chapter 1
Hardware Description

This chapter gives the definitions and shows the positions of jumpers, headers and connector. All of the configuration jumpers on Portwell evaluative Carrier PCOM-C701 are in the proper position. The default settings shipped from factory are marked with a star (★).

1.1 Connector Allocation

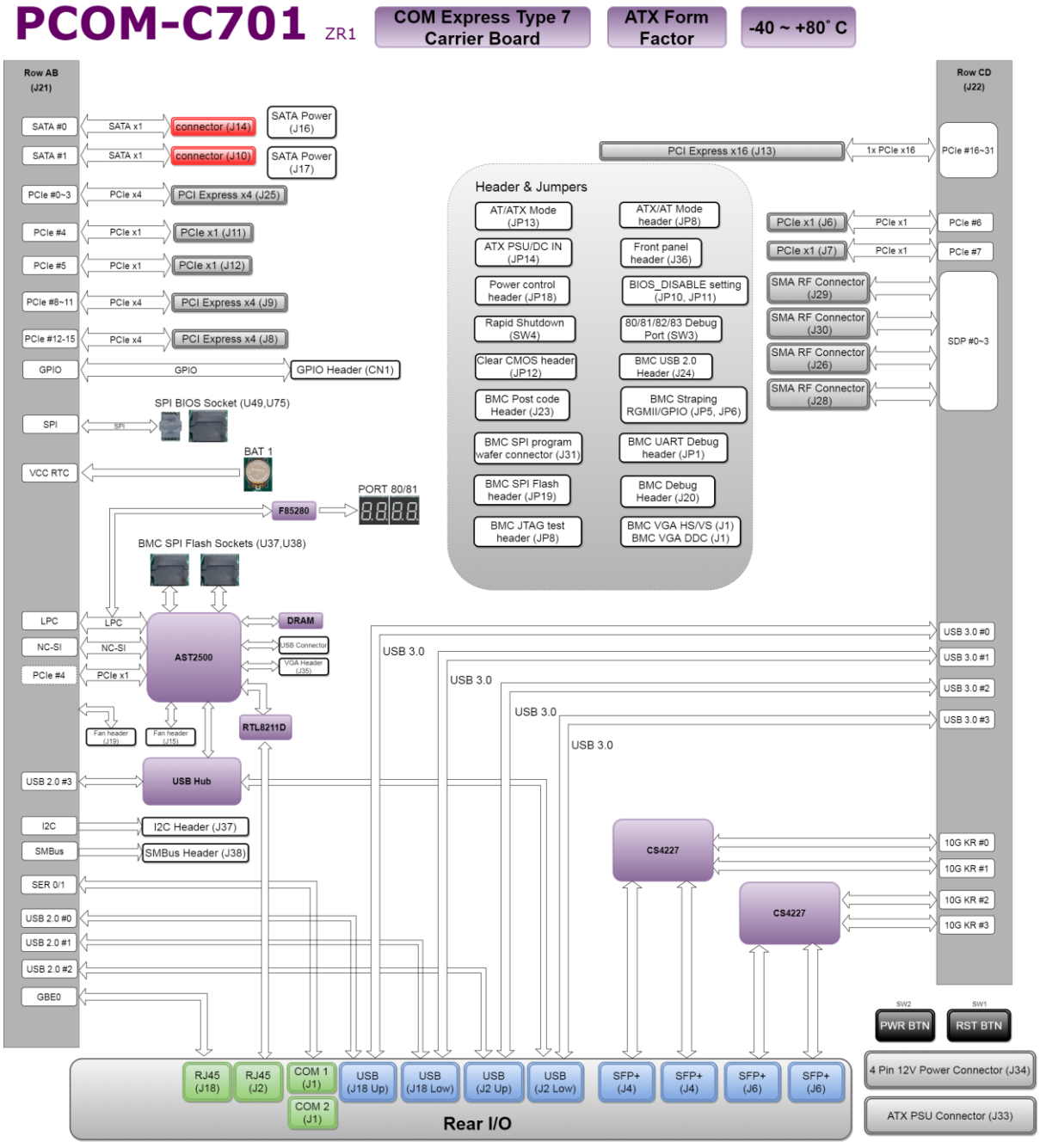

Figure 1-1 PCOM-C701 ZR1 Block Diagram

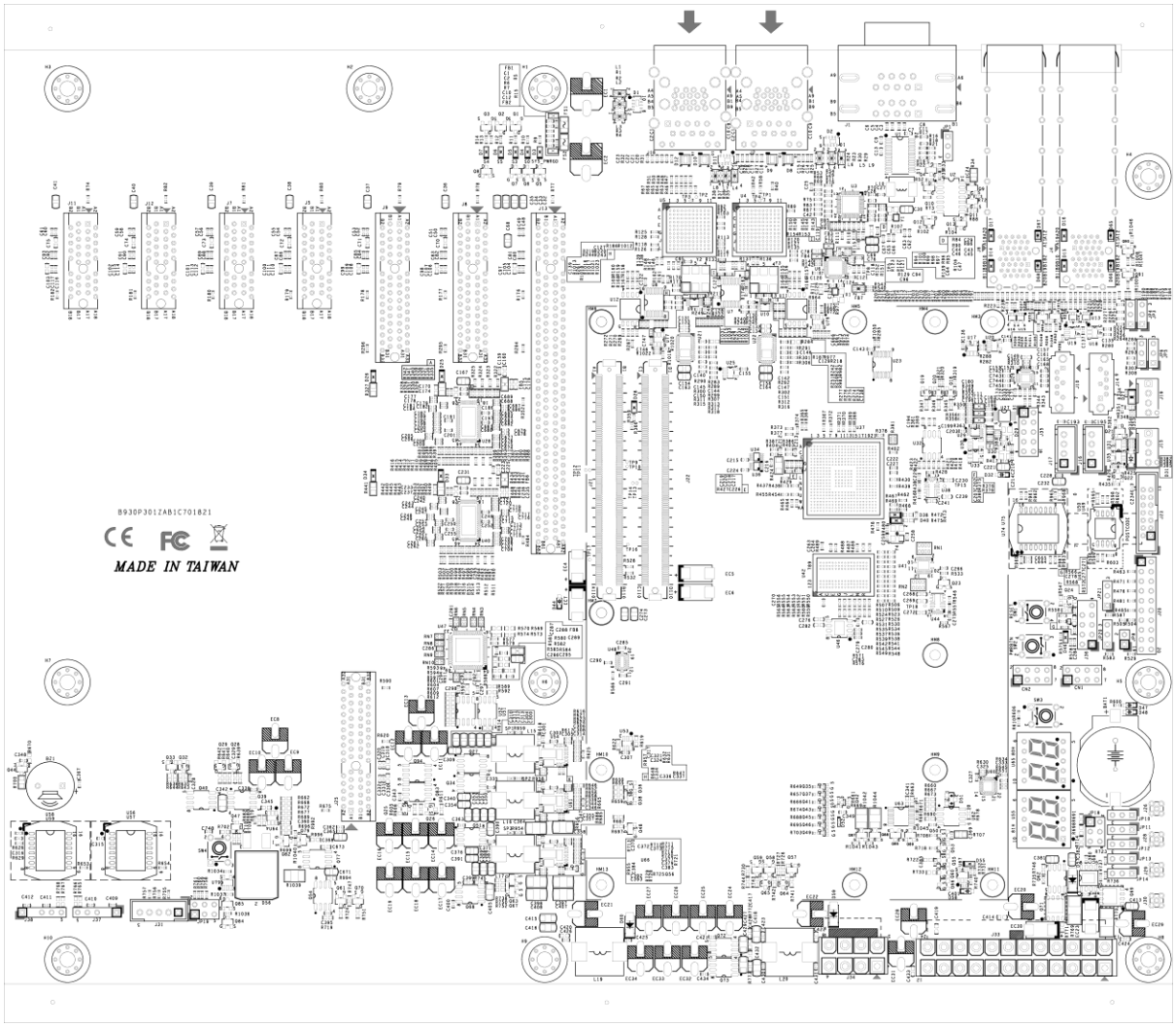

Figure 1-2 PCOM-C701 ZR1 Jumper & Connector Location

Pin Header Function List

Jump	Function	Remark
J1	D-SUB Connector (Module EC Serial Port)	
J2, J18	RJ45+2xUSB3.0 Port	
J4, J6	10 GbE SFP+ Cage	
J5, J7, J11, J12	PCIe x1 slot	
J8, J9, J25	PCIe x4 slot	
J13	PCIe x16 slot	
J10, J14	SATA Connector	
J15	BMC Fan Connector	
J16, J17	SATA Power Connector	
J19	Fan Connector	
J20	BMC JTAG Debug Header	
J21, J22	COM Express Connector	
J23	BMC POSTCODE Header	
J26, J28, J29, J30	SMA Connector	
J31	BMC SPI Flash Program Wafer	
J33	ATX PSU Connector	
J34	8 Pin 12V Power Connector	
J35	BMC VGA Connector	
J36	Front Panel Header	
J37	I2C Header	
J38	SMBus Header	
CN1	LPC Debug Header	
CN2	Module GPIO Header	
JP1	BMC UART Debug Header	
JP3, JP4	PHY mode Setting	
JP5	BMC SuperIO address selection	
JP6	BMC ACPI function selection	
JP8	BMC JTAG test reset Setting	
JP10, JP11	Setting BIOS Header	
JP12	Clear CMOS Setting	
JP13	ATX/AT Mode selection	
JP14	ATX PSU/DCIN Mode selection	
JP18	BMC Power control	
JP19	BMC SPI Flash selection	
JP20	PCIe#4 to BMC/PCIe slot selection	
JP21	BMC Debug I2C header	

SW1	Reset Bottom	
SW2	Power Button	
SW3	Showing 80 port previous data button	
SW4	Rapid Shutdown test button	
U49, U75	Carrier board SPI Socket (8/16 Pin)	
U57, U59	BMC FW Flash Socket	

JP1：BMC UART Debug Header

1	GND
2	Bmc_UART_RXD5
3	Bmc_UART_TXD5

JP3, JP4：PHY mode Setting

1-2	MDIO mode only
*2-3	I2C or MDIO mode

JP5：BMC SuperIO address selection

*1-2	Decode SuperIO 0x4E address
2-3	Decode SuperIO 0x2E address

JP6：BMC ACPI function selection

*1-2	Enable BMC ACPI function
2-3	Disable BMC ACPI function

JP8：BMC JTAG test reset

*Open	Normal
1-2	Enable JTAG test reset

JP10, JP11：Setting BIOS Header

1-2, 1-2	Module SPI Boot
1-2, 2-3	Module SPI Boot
2-3, 1-2	Carrier SPI Boot
*2-3, 2-3	Module SPI Boot

JP12：Clear CMOS Setting

*1-2	Normal
2-3	Clear CMOS

JP13：ATX/AT Mode Setting

1-2	ATX Mode
*2-3	AT Mode

JP14：ATX PSU/DCIN Mode selection

1-2	Single DCIN Mode (8Pin 12V Power)
*2-3	ATX PSU Mode(ATX PSU + 4Pin 12V Power)

JP18：BMC Power control

*1-2; 3-4; 5-6	Normal
All Open	Power controlled by BMC

JP19：BMC SPI Flash selection

*1-2	CS0#
3-4	CS1#

JP20：PCIe#4 to BMC/PCIe slot selection

*1-2	Controlled by Module GPO0
2-3	PCIe#4 to PCIe slot
Open	PCIe#4 to BMC

JP21：BMC Debug I2C header

1	SCL6
2	SDA6
3	GND

J16, J17：SATA Power Connector

1	+12V
2	GND
3	GND
4	+5V

J15：BMC FAN Control

1	GND
2	12V
3	Bmc_TACH0
4	Bmc_PWM0

J19：FAN Control

1	GND
2	12V
3	FAN_TACHIN
4	FAN_PWMOUT

J20：BMC JTAG Debug Header

1	3V_DUAL
2	3V_DUAL
3	ARM_nTRST
4	GND
5	ARM_TDI
6	GND
7	ARM_TMS
8	GND
9	ARM_TCK
10	GND
11	ARM_RTCK
12	GND
13	ARM_TDO
14	GND
15	SRST#
16	GND
17	GND
18	GND
19	GND
20	GND

J23：BMC POSTCODE Header

1	LED_POSTCODE_0
2	LED_POSTCODE_1
3	LED_POSTCODE_2
4	LED_POSTCODE_3
5	LED_POSTCODE_4
6	LED_POSTCODE_5
7	LED_POSTCODE_6
8	LED_POSTCODE_7
9	DEBUG_PORT_UART_TX
10	DEBUG_PORT_UART_RX
11	BMC_RST_BTN_IN_IN
12	FM_UART_SWITCH_N
13	GND
14	VCC

J31：BMC SPI Program Wafer

1	FWSPI_CS0
2	FWSPICK
3	FWSPIMOSI
4	FWSPIMISO
5	GND

J35：BMC VGA Connector

1	DACROA
2	DAC_DDCCLK
3	DACGOA
4	GND
5	DACBOA
6	DAC_DDCDAT
7	DACVS
8	GND
9	DACHS
10	VCC (+5V)

J36：Front Panel Header

1-3	SATA LED
5-7	RESET Button
6-8	Power Button
2, 4, 9	N.C.

J37：I2C Header

1	I2C_CLK
2	N.C.
3	GND
4	I2C_DATA
5	VCC3 (+3.3V)

J38：SMBus Header

1	EC_SMCLK0_R
2	N.C.
3	GND
4	EC_SMDAT0_R
5	3V_DUAL (+3.3V)

CN1：LPC Debug Header

1	LPC_CLK4
2	LAD0
3	LFRAME#_N
4	LAD1
5	ICH_SERIRQ
6	LAD2
7	BUF_PLT_RST#
8	LAD3

CN2：Module GPIO Header

1	GPI0
2	GPO0
3	GPI1
4	GPO1
5	GPI2
6	GPO2
7	GPI3
8	GPO3