COM Express™ PCOM-B701GT User's Guide R0.2

Revision History

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1 Introduction

The Portwell PCOM-701GT Type 7, basic form factor (125mm x 95mm) COM Express module is designed with the Intel® Atom® processor C3000 product family (codenamed Denverton). Specifically, the COM Express 3.0 specification's new Type 7 pinout, when compared to the Type 6 pinout, trades all the graphics interfaces for up to four 10GbE ports and a total of 32 PCIe lanes, ideal for applications in micro server and alike, requiring low power consumption while supporting high computing performance and communication throughput.

Portwell's PCOM-B701GT features four 10GbE KR, one GbE, DDR4 ECC/non-ECC memory support, and Gen3 PCIe supporting high speed I/O card. It is compatible with Type 7 carrier board. In addition, Portwell's PCOM-B701GT Type 7 COM Express module also supports a wide -40°C~85°C industrial temperature range (selected SKUs).

2 Block Diagram

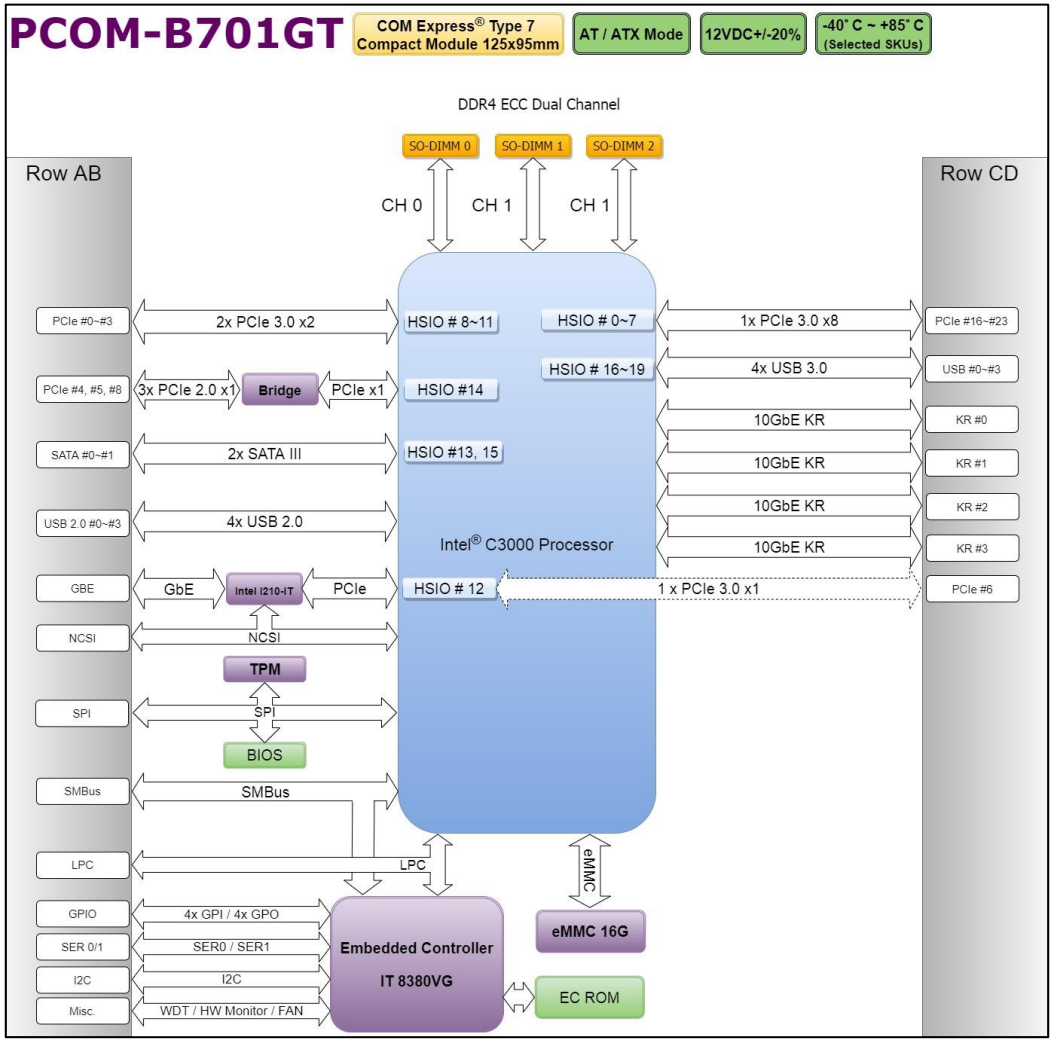


Figure 1 PCOM-B701GT Block Diagram

3 Specifications

Product	➢ PCOM-B701GT
Form Factor	➢ Type 7, Basic Size Form Factor COM Express® (125 X 95mm)
Processor	➢ Intel®Atom-Processor-C3808 ➢ Intel®Atom-Processor-C3758 ➢ Intel®Atom-Processor-C3708 ➢ Intel®Atom-Processor-C3538 ➢ Intel®Atom-Processor-C3508 ➢ Intel®Atom-Processor-C3308
BIOS	➢ AMI BIOS
Memory	➢ SODIMM DDR4 ➢ Support ECC ➢ Up to 96GB 2400MHz
Ethernet	➢ Intel® I210IT ➢ 4 x KR(10GbE)
Security	➢ TPM 2.0 (Option)
PCI Express	➢ Up to 1x PCIe Gen3 x8、2x PCIe Gen3 x2、1x PCIe Gen3 x1、3x PCIe Gen2 x1 (based on CPU/HSIO arrangement)
I/O	➢ 4 x USB2.0 ➢ 4 x USB 3.0(selected SKUs) ➢ 2 x SATA3.0 ➢ 8 bit GPIO (default 4 in/ 4out) ➢ I2C / SMBus ➢ 2x UART

Hardware Monitors	➢ ITE series Embedded Controller, Voltage, Fan and Temperature
Power Management	➢ ACPI 4.0
Environment	➢ Operating Temperature 0°C ~60°C Extended : -40°C ~+85°C (Processor dependent) ➢ Storage Temperature -40°C ~+85°C ➢ Relative Humidity 5%~95%

Table 1 PCOM-B701GT SPEC

3.1 PCOM-B701GT Processor list

PCOM-B701GT Series	PCOM-B701GT	PCOM-B701GT -	PCOM-B701GT -	PCOM-B701GT -	PCOM-B701GT	PCOM-B701GT -
Ordering P/N	AB1-3J01	AB1-3H86	AB1-3H96	AB1-3H89	AB1-3J94	AB1-3H90
CPU Feature						
Processor Number	C3308	C3508	C3538	C3708	C3758	C3808
Cache	4 MB	8 MB	8 MB	16 MB	16 MB	12 MB
Instruction Set	64-bit	64-bit	64-bit	64-bit	64-bit	64-bit
Performance						
# of Cores	2	4	4	8	8	12
# of Threads	2	4	4	8	8	12
Processor Base Frequency	1.6 GHz	1.6 GHz	2.1 GHz	1.7 GHz	2.20 GHz	2.0 GHz
Max Turbo Frequency	2.1 GHz	1.6 GHz	2.1 GHz	1.7 GHz	2.20 GHz	2.0 GHz
TDP	9.5 W	11.5 W	15W	17 W	25 W	25 W

Table 2 PCOM-B701GT Processor list

3.2 Supported Operating Systems

The following operating system support is based on the operating system support matrix information released by Intel for the Atom® Denverton platform. For operation system support, please follow the intel release.

Portwell does not endorse/validate/support any specific Linux distribution or entity mentioned on this list.

Portwell recommends customers to work with Linux vendors/open source communities to find feature list and support model.

Windows	Windows server 2012 r2,2016
Linux Yocto	Kernel version: 4.14 Yocto version: Yp 2.5 sumo
Red Hat	7.3, 7.4 version
Ubuntu(Canonical)	16.04, 18.04
CentOS	7.3
WR Linux	WRL8, WRL 9 , LTS 17,LTS 18, LTS 19
SUSE	12 SP3

3.3 Windows OS driver

Please download the drivers from Portwell download center website.

If you can't find the file you need, please contact your responsible sales window

Download Center	http://www.portwell.tw/support/download_center.php	Standard releases for launched products · Drivers

3.4 Electrical Characteristics

Input voltage	+12VDC (Nominal)
RTC Battery	From Carrier
Power on mode	AT Mode & ATX Mode

Table 3 Electrical characteristics

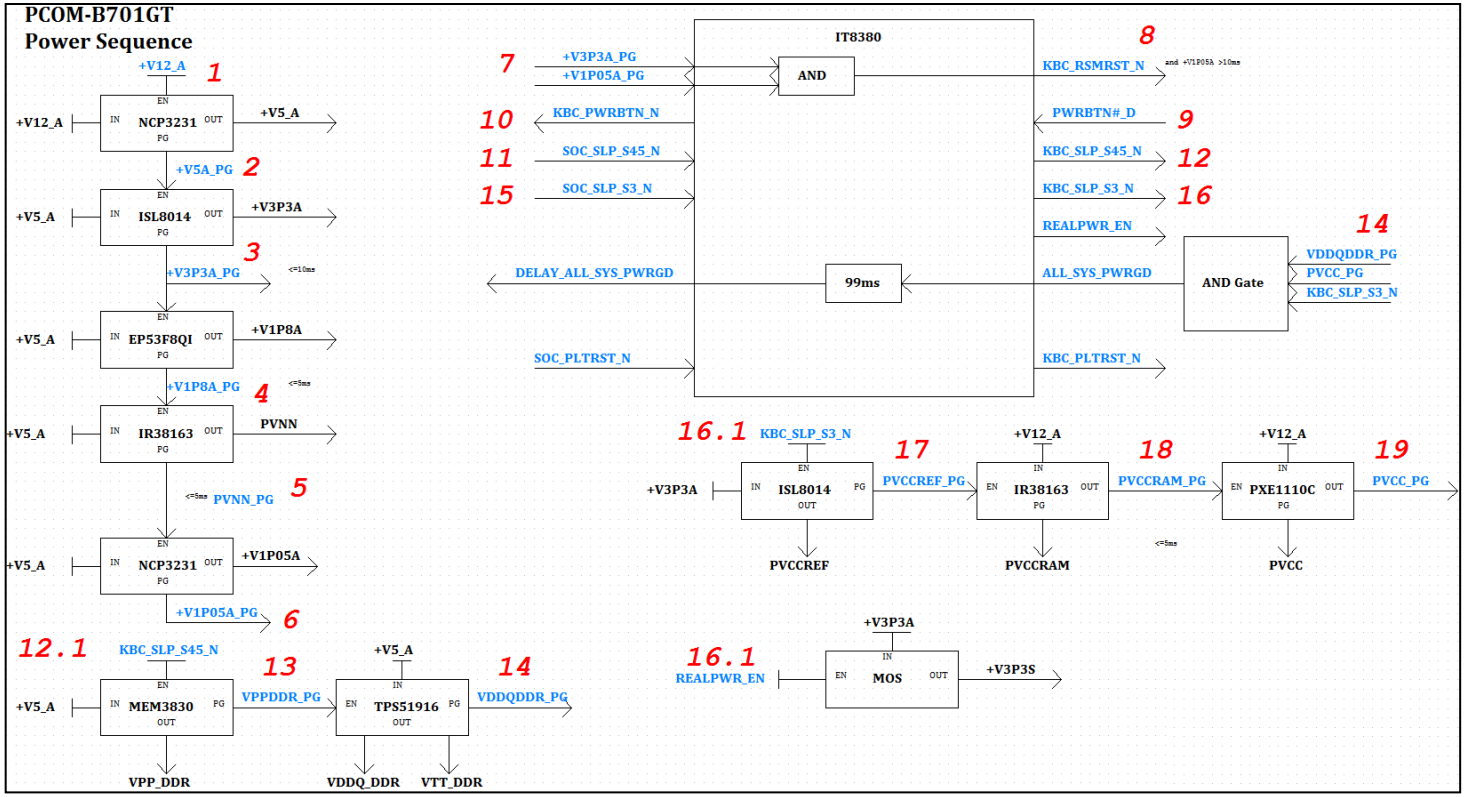


Figure 2 PCOM-B701GT Power sequence

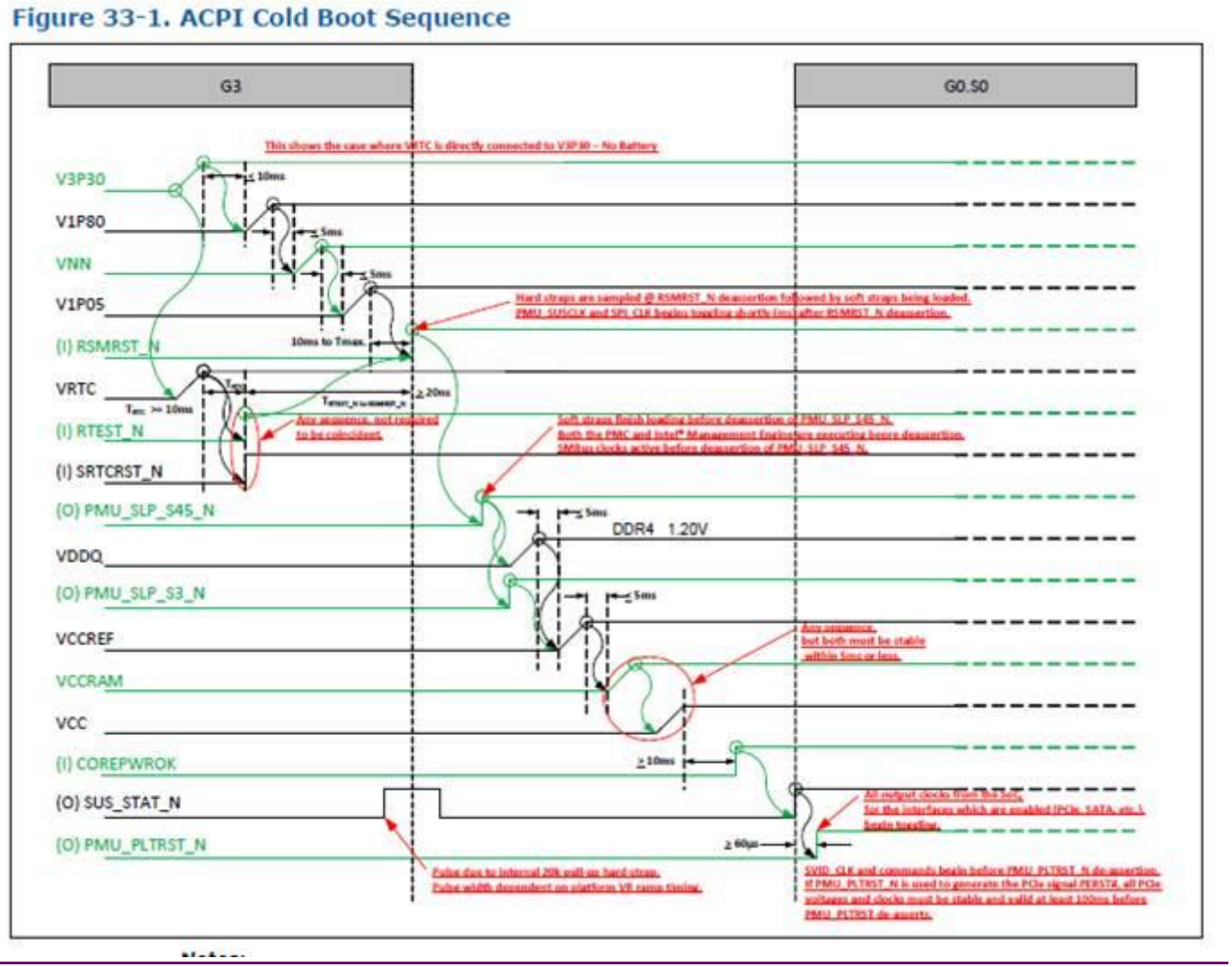


Figure 3 Power on sequence

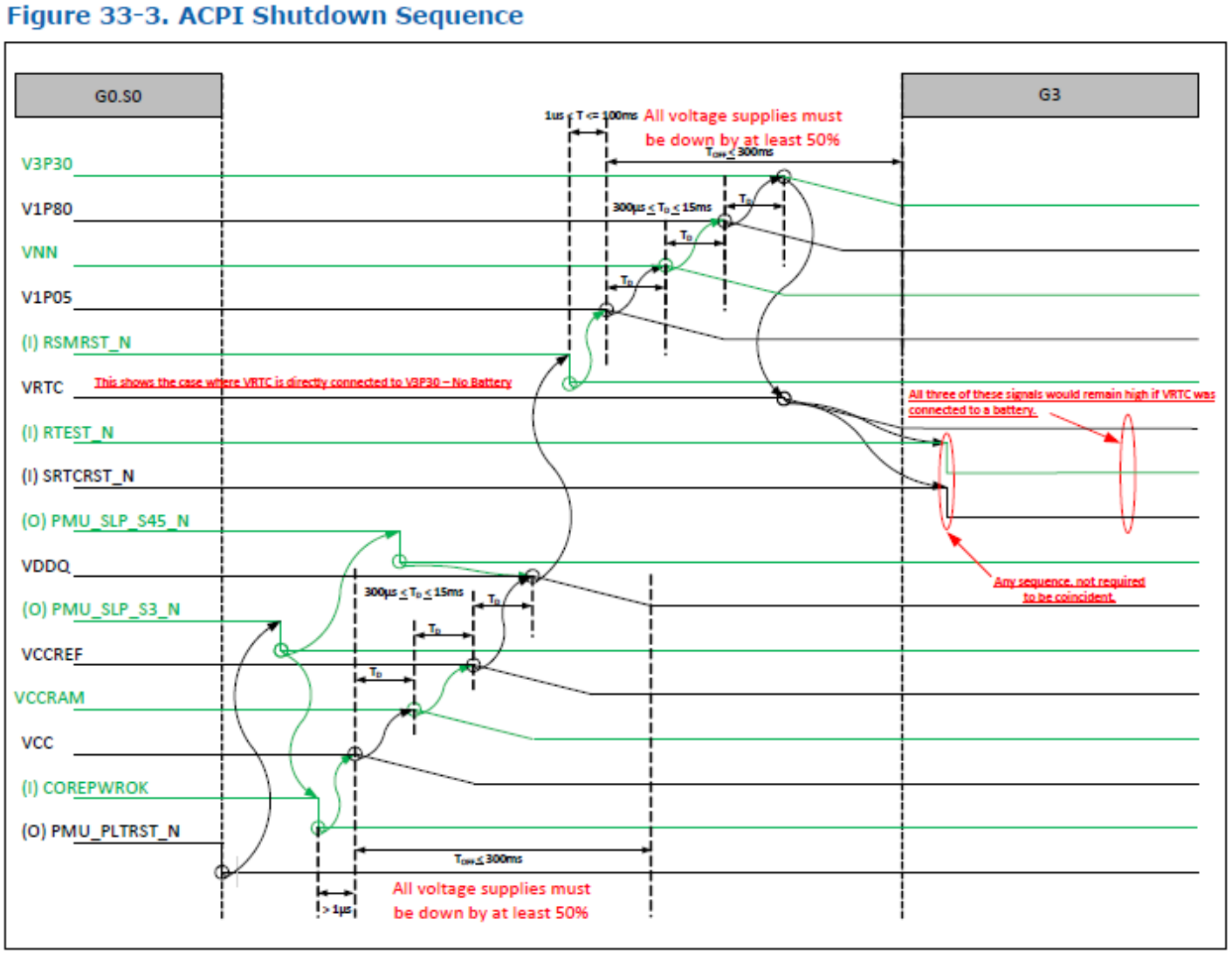


Figure 4 Shutdown sequence

3.5 Mechanical Dimensions

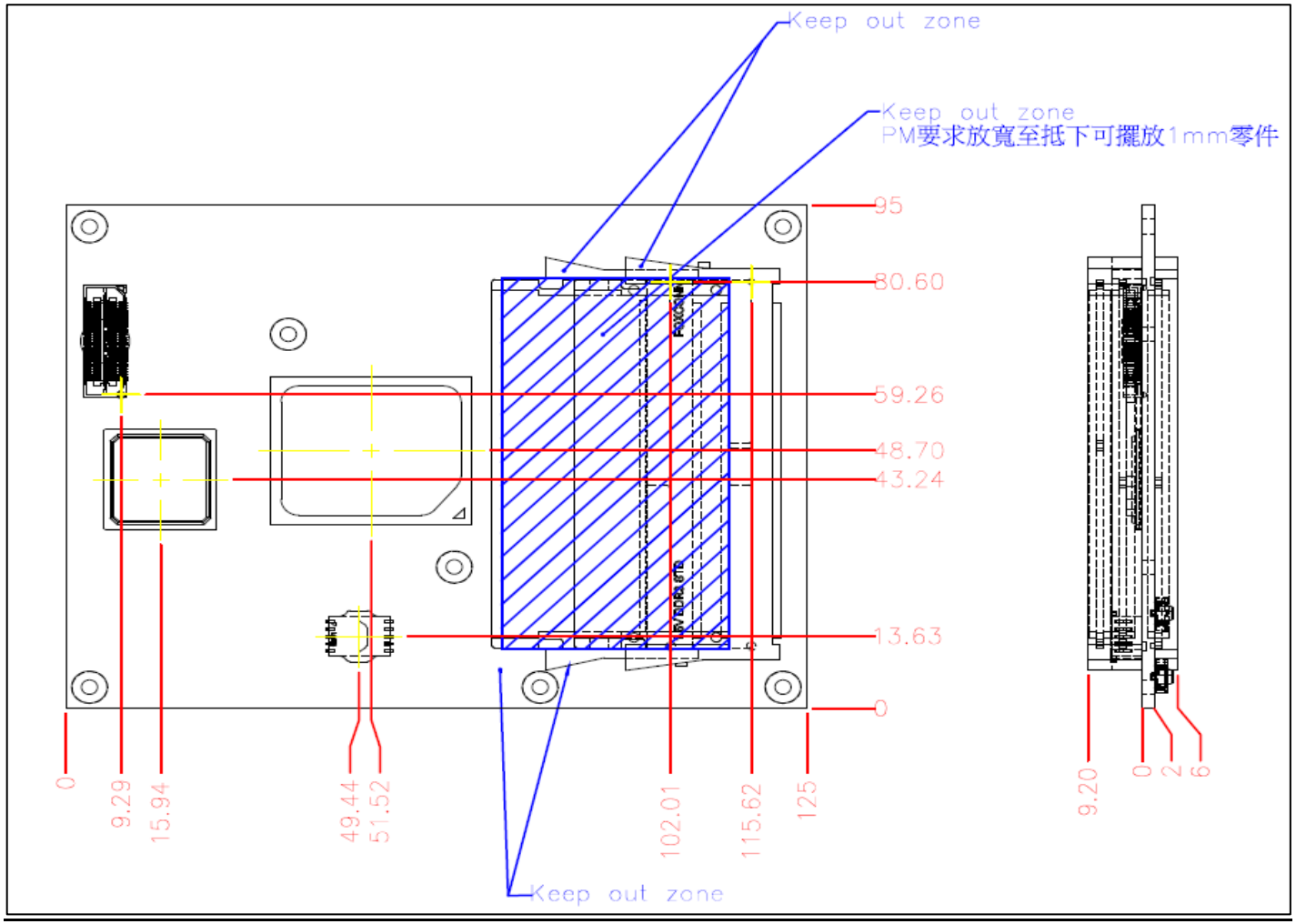


Figure 5 Mechanical Dimensions - Top

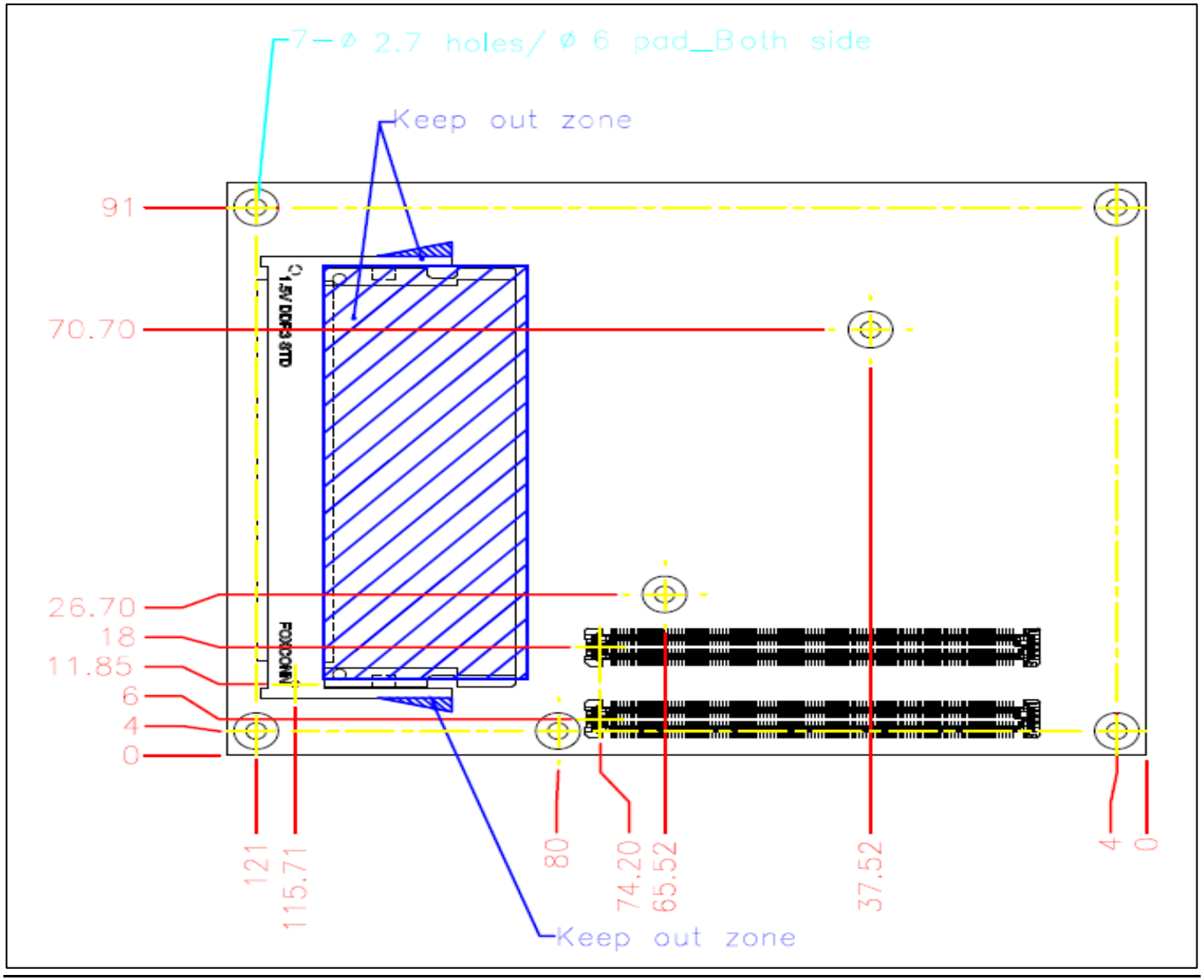


Figure 6 Mechanical Dimensions - Bottom

3.6 3 SODIMM socket design

PCOM-B701GT has designed additional Memory SODIMM socket at the bottom, which supports up to DDR4 up to 96GB capacities. Before inserting the DDR4 SODIMM memory, please refer to the below SODIMM arrangement and note that there are 2 SODIMM sockets of channel 1, the CH1 SODIMM2 (the button one) works only if CH1 SDDIMM1 (the top one) is inserted. If you only need one DDR4 SODIMM, please insert it in CH0.

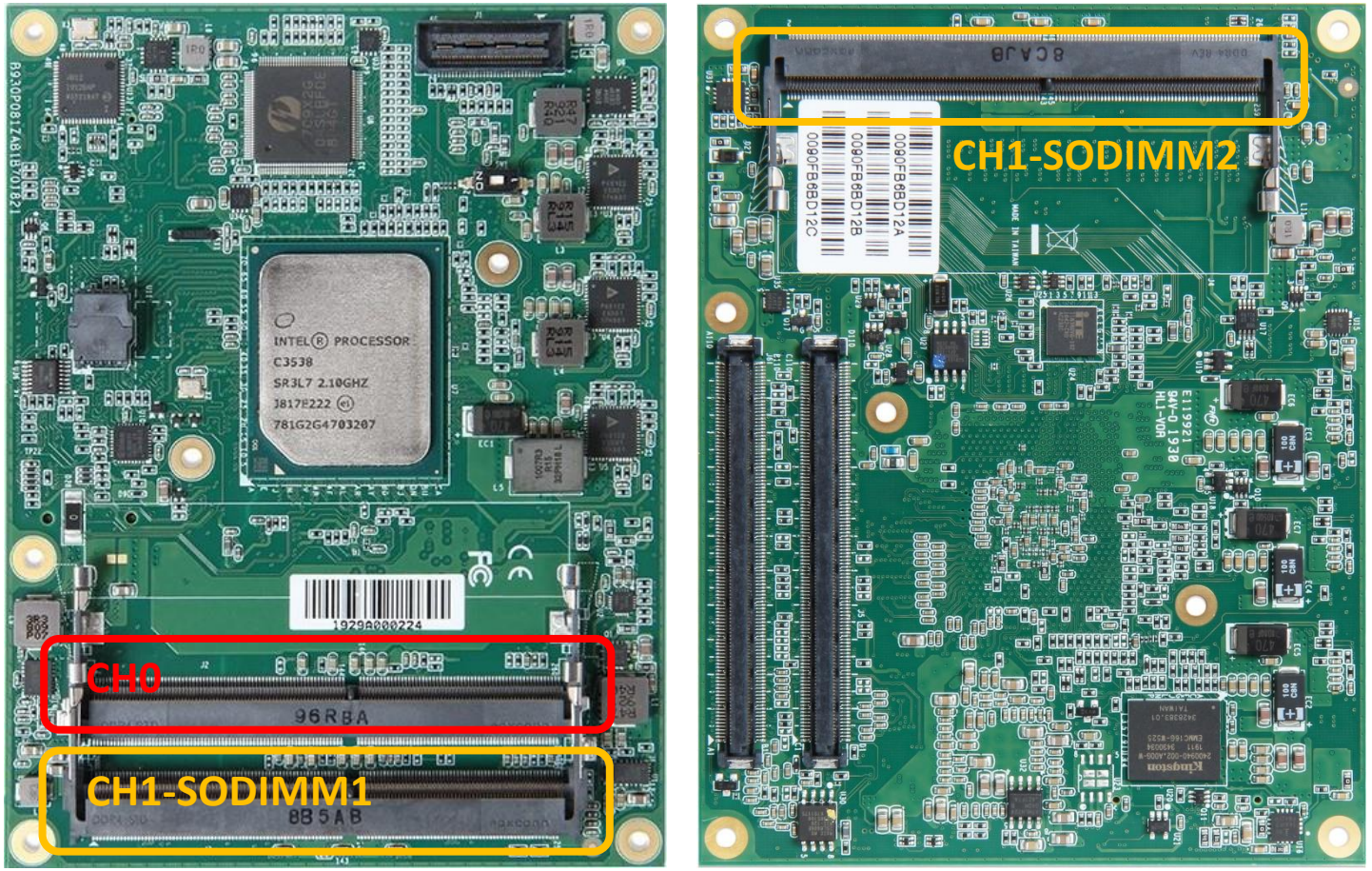


Figure 7 SODIMM socket design

3.7 Environmental Specifications

Storage Temperature	-40°C ~+85°C
Operation Temperature	0°C ~60°C Extended : -40°C ~+85°C (Processor dependent)
Storage Humidity	0%~95%
Operation Humidity	0%~95%

Table 4 Environmental Specifications

3.8 Ordering Guide

- Module

Product	Ordering P/N
PCOM-B701GT-C3808	AB1-3H90
PCOM-B701GT-C3758	AB1-3J94
PCOM-B701GT-C3708	AB1-3H89
PCOM-B701GT-C3538	AB1-3H96
PCOM-B701GT-C3508	AB1-3H86
PCOM-B701GT-C3308	AB1-3J01

Table 5 Ordering Guide - PCOM-B701GT

- Accessory

Accessory	Ordering P/N
PCOM-B701GT Cooler	B9971960
PCOM-B701GT Heat Sink	B830B300
PCOM-B701GT Heat spreader	B830B290
Evaluation Carrier PCOM-C701-BMC	AB1-3K14Z

Table 6 Ordering Guide - Accessory

4 Thermal Solution

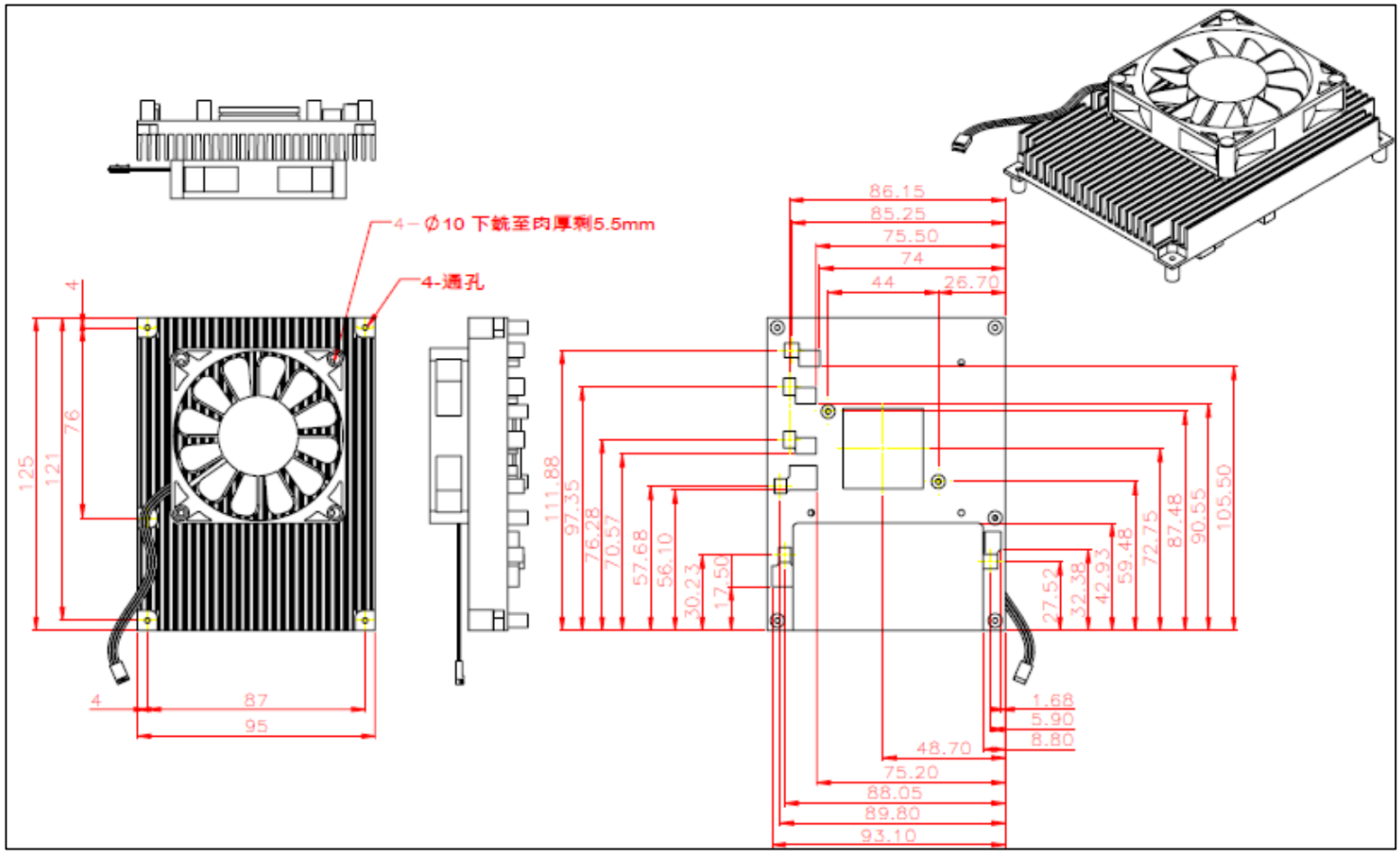


Figure 8 PCOM-B701GT Cooler Dimension

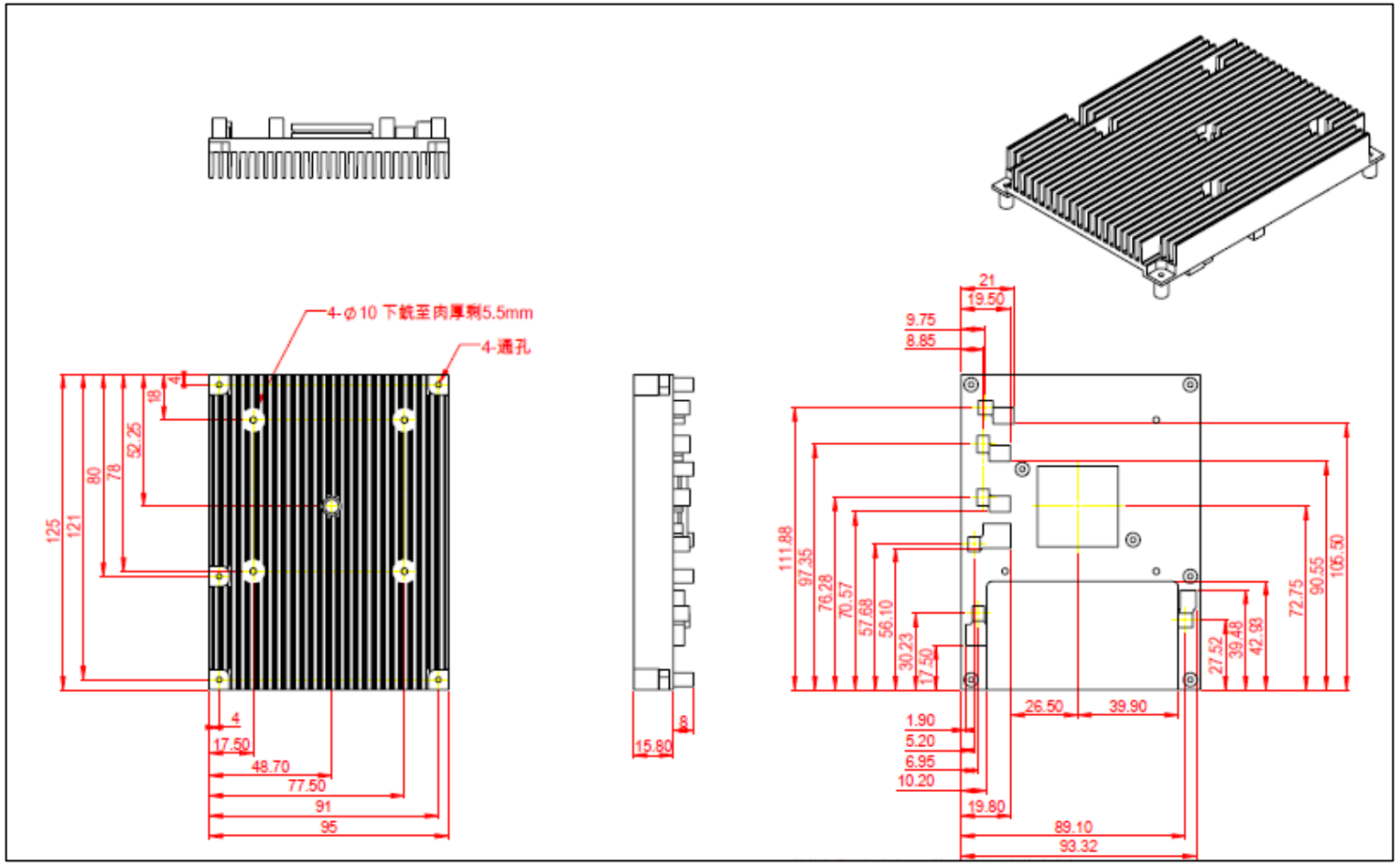


Figure 9 PCOM-B701GT Heat Sink Dimension

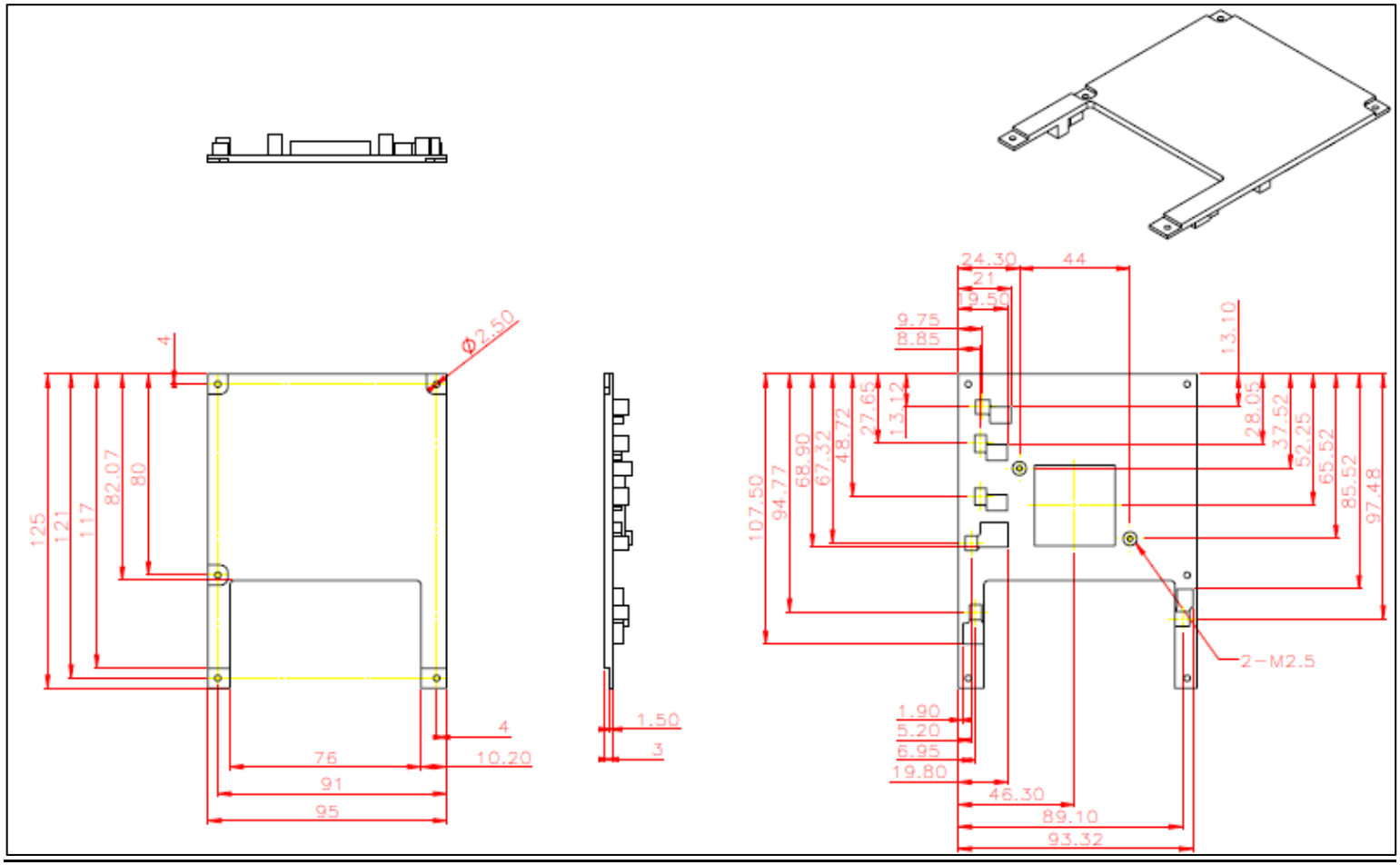


Figure 10 PCOM-B701GT Heat Spreader Dimension

4.1 Assembly Guide

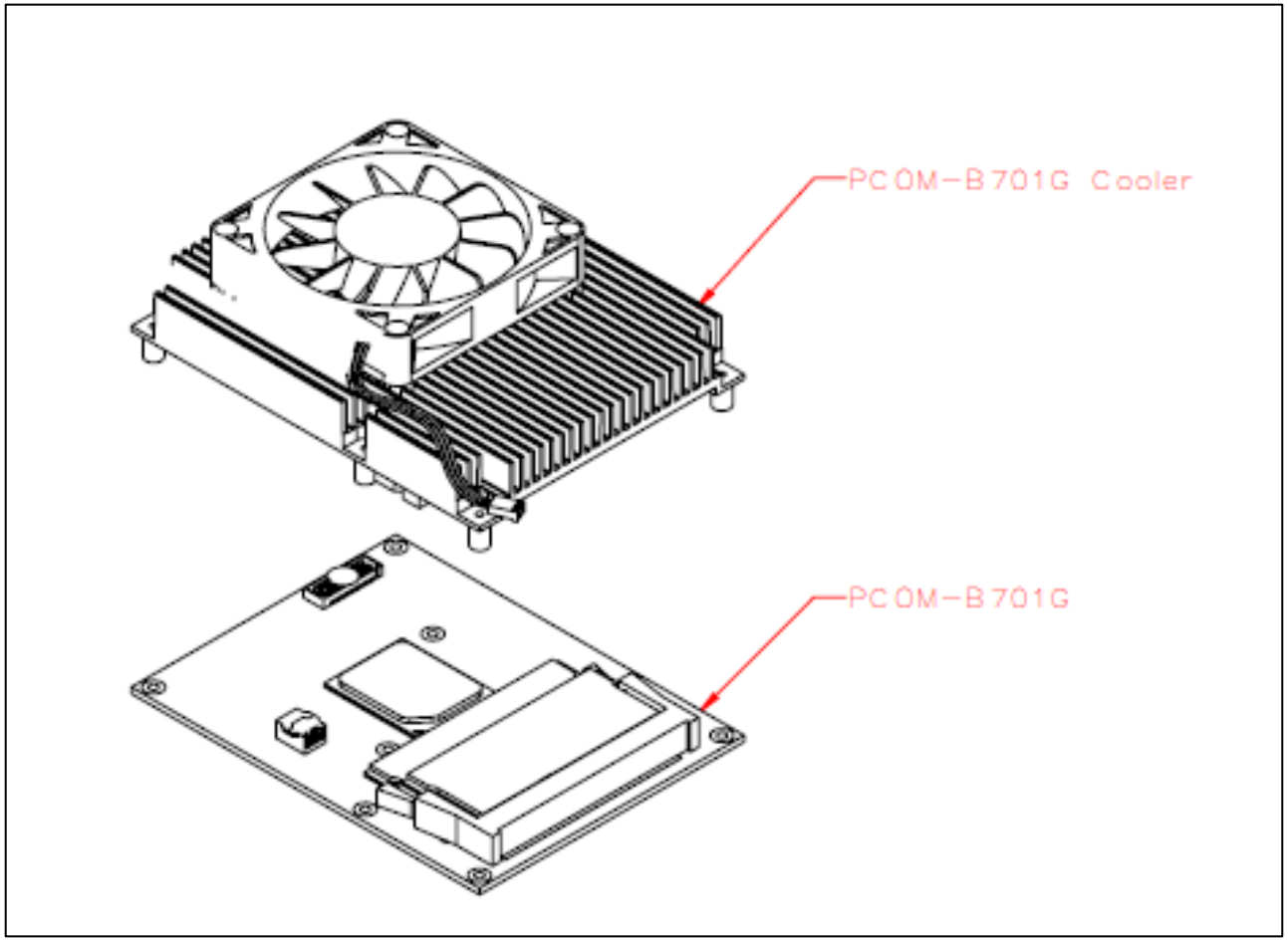


Figure 11 PCOM-B701GT Cooler Assembly Guide

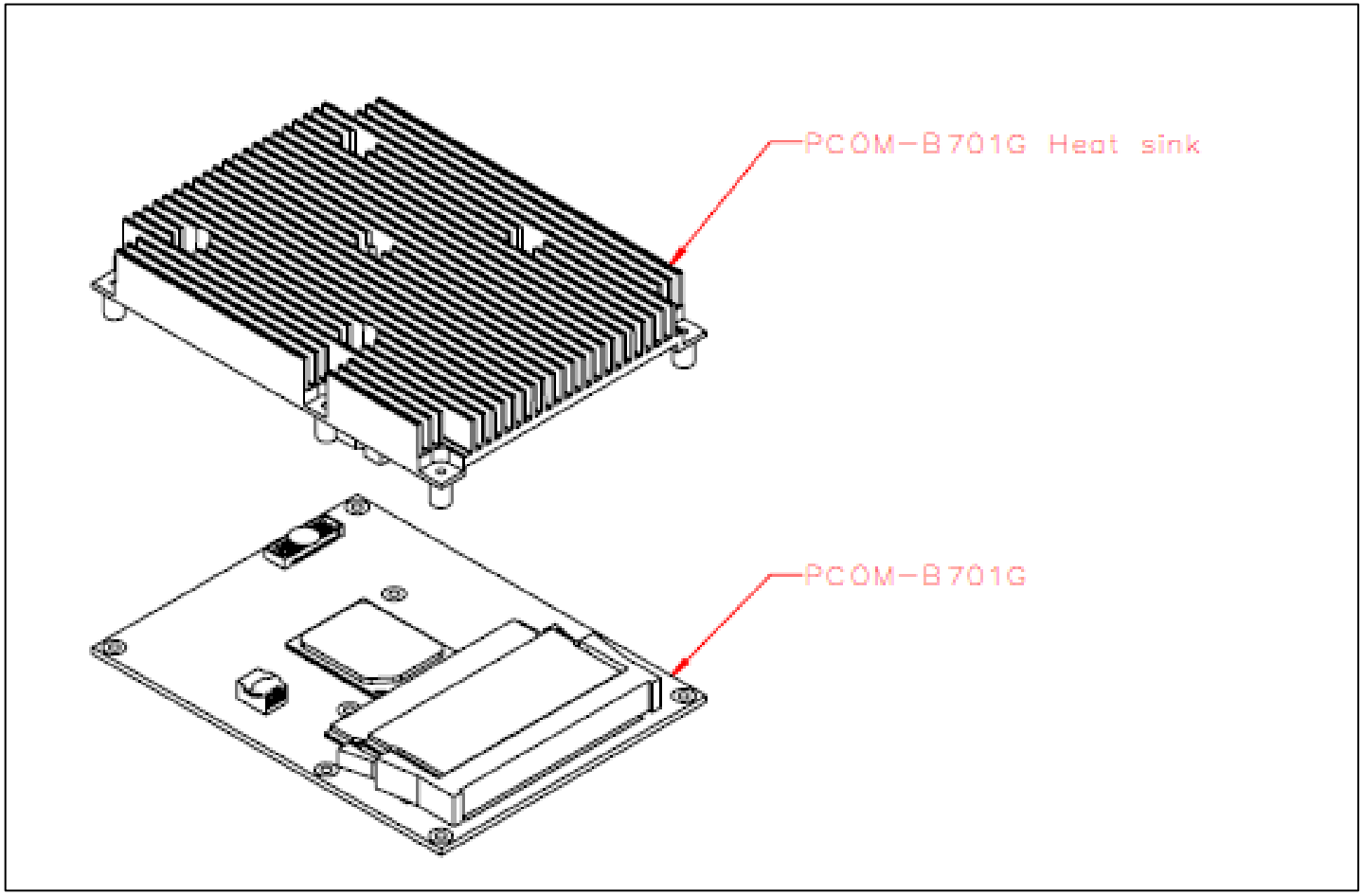


Figure 12 PCOM-B701GT Heat Sink Assembly Guide

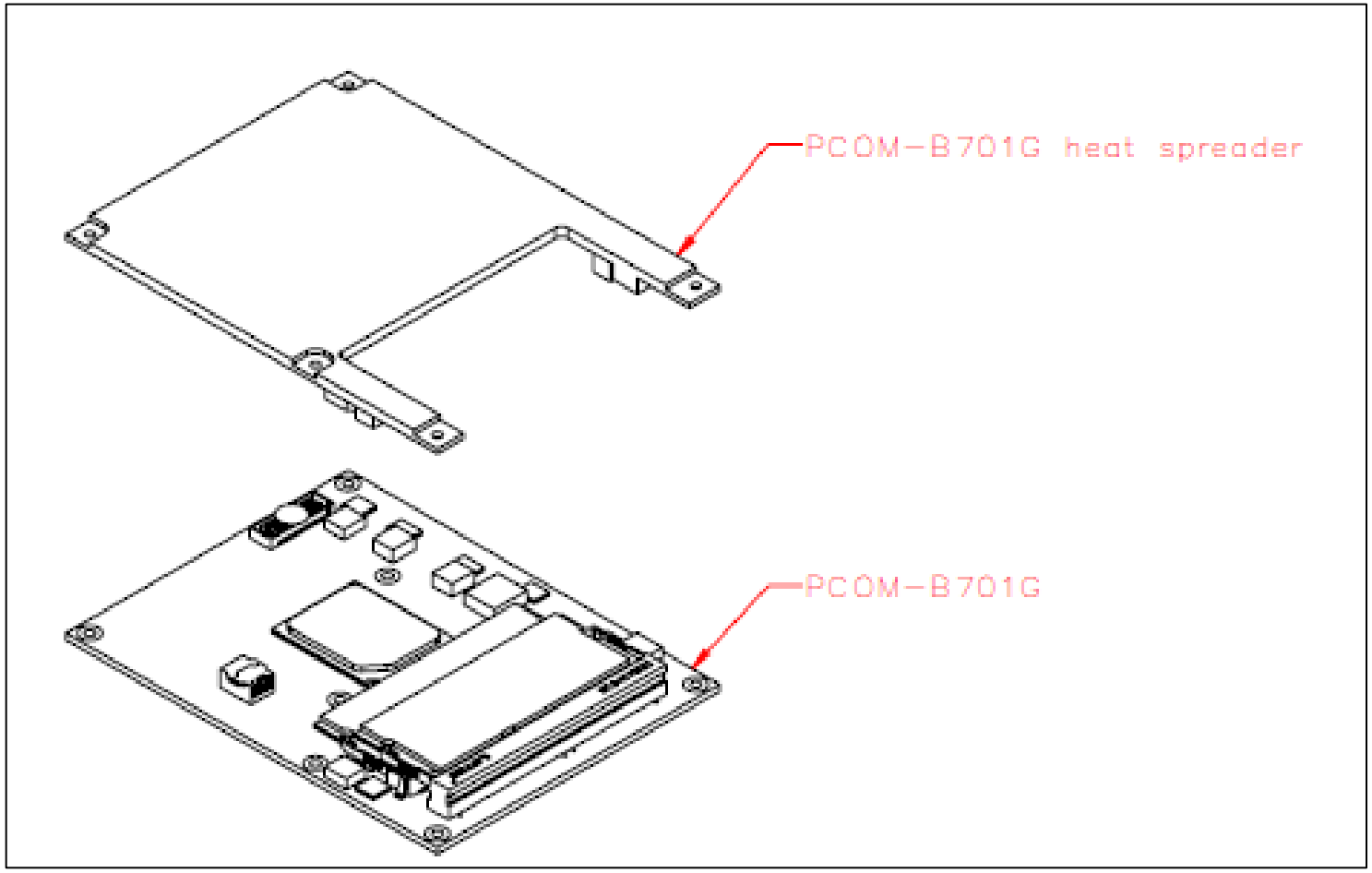


Figure 13 PCOM-B701GT Heat Spreader Assembly Guide

5 Signal Descriptions and Pin out Tables

Signal Tables Terminology Descriptions

I	Input to the Module
O	Output from the Module
I/O	Bi-direction input / output signal
OD	Open Drain output
CMOS	Logic input or output. Input thresholds and output levels shall be 80% of supply rail for high side and 20% of the relevant supply rail for low side.
PCIE	PCI Express compatible differential signal. Please refer to the PCI Express Specification for details. PCIE transmit pins (Module outputs) shall be AC coupled on the Module. PCIE receive pins (Module inputs) shall be DC coupled on the COM Express® Module and shall be assumed to be AC coupled off Module, close to the signal source. If the target PCI Express device resides on the Carrier Board, the Module PCIE receive lanes (target PCIE device transmit lanes) shall be AC coupled near the device on the Carrier Board. If the Carrier Board implements a PCIE slot, then these signals shall be AC coupled on the add-in card, not on the Carrier Board.
SATA	SATA compatible differential signal. Please refer to the SATA Specification for details. All COM Express® SATA signals shall be AC coupled on the Module.
LVDS	Low Voltage Differential Signal – 330mV nominal; 450mV maximum differential signal.
Analog	Inputs and Outputs used for LAN, and VGA are analog signals.
PU	Pull-up resistor on PCOM-B701GT
PD	Pull-down resistor on PCOM-B701GT

Table 7 Signal Tables Terminology Descriptions

#Note : Reserved / Not connected pins are highlighted as gray color.

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A1	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A2	GBE0_MDI3-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A3	GBE0_MDI3+	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A4	GBE0_LINK100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A5	GBE0_LINK1000#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A6	GBE0_MDI2-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A7	GBE0_MDI2+	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A8	GBE0_LINK#	Gigabit Ethernet Controller 0 link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
A9	GBE0_MDI1-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-

A10	GBE0_MDI1+	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A11	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A12	GBE0_MDI0-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A13	GBE0_MDI0+	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A14	GBE0_CTREF	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.	-	-	GND min 3.3V max	Placeholder 0 ohm to V_1P5_L1	-
A15	SUS_S3#	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.	O	CMOS	3.3V Suspend / 3.3V	PD 10kohm	-
A16	SATA0_TX+	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A17	SATA0_TX-	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A18	SUS_S4#	Indicates system is in Suspend to Disk state. Active low output.	O	CMOS	3.3V Suspend / 3.3V	-	-
A19	SATA0_RX+	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-

A20	SATA0_RX-	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A22	PCIE_TX15+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A23	PCIE_TX15-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A24	SUS_S5#	Indicates system is in Soft Off state.	O	CMOS	3.3V Suspend / 3.3V	-	There is no SUS_S5# in Broadwell-DE.
A25	PCIE_TX14+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A26	PCIE_TX14-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A27	BATLOW#	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	I	CMOS	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
A28	(S)ATA_ACT#	SATA activity indicator, active low.	I/O	CMOS	3.3V / 3.3V	PU 4.7K ohm to 3.3V	-
A29	RSVD	Reserved Pin	-	-	-	-	-
A30	RSVD	Reserved Pin	-	-	-	-	-
A31	GND(FIXED)	GND(FIXED)	-	-	-	-	-

A32	RSVD	Reserved Pin	-	-	-	-	-
A33	RSVD	Reserved Pin	-	-	-	-	-
A34	BIOS_DIS0#	Selection straps to determine the BIOS boot device.The Carrier should only float these or pull them low. Shared pin with ESPI_SAFS	I	CMOS	NA	PU 10K ohm to 3.3V	-
A35	THRMTRIP#	Active low output indicating that the CPU has entered thermal shutdown	O	CMOS	3.3V / 3.3V	PU 1K ohm to 3VSB	-
A36	PCIE_TX13+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A37	PCIE_TX13-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A38	GND	GND	-	-	-	-	-
A39	PCIE_TX12+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A40	PCIE_TX12-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A41	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A42	USB2-	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A43	USB2+	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-

A44	USB_2_3_OC#	USB over-current sense, USB channels 2 and 3. A pull-up for this line shallbe present on the Module. Do not pull this line high on the Carrier Board	I	CMOS	3.3V Suspend / 3.3V	PU 10K ohm to 3VSB	-
A45	USB0-	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A46	USB0+	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A47	VCC_RTC	Real-time clock circuit-power input. Nominally +3.0V.	-	PWR	-	-	-
A48	RSVD	Reserved Pin	-	-	-	-	-
A49	GBE0_SDP	Gigabit Ethernet Controller 0 Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 4.3.4 for details.	I/O	CMOS	3.3V Suspend / 3.3V	PU 10K ohm to 3VSB	-
A50	LPC_SERIRQ	LPC serial interrupt / Shared pin with ESPI_CS1#	I/O	CMOS	3.3V / 3.3V	PU 10K ohm to 3.3V	-
A51	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A52	PCIE_TX5+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

A53	PCIE_TX5-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A54	GPI0	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A55	PCIE_TX4+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A56	PCIE_TX4-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A57	GND	GND	-	-	-	-	-
A58	PCIE_TX3+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A59	PCIE_TX3-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A60	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A61	PCIE_TX2+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A62	PCIE_TX2-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A63	GPI1	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A64	PCIE_TX1+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A65	PCIE_TX1-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A66	GND	GND	-	-	-	-	-

A67	GPI2	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A68	PCIE_TX0+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A69	PCIE_TX0-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A70	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A71	PCIE_TX8+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A72	PCIE_TX8-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A73	GND	GND	-	-	-	-	-
A74	PCIE_TX9+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A75	PCIE_TX9-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A76	GND	GND	-	-	-	-	-
A77	PCIE_TX10+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A78	PCIE_TX10-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A79	GND	GND	-	-	-	-	-
A80	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A81	PCIE_TX11+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

A82	PCIE_TX11-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A83	GND	GND	-	-	-	-	-
A84	NCSI_TX_EN	NCSI Transmit Enable (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PD 270 ohm	-
A85	GPI3	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A86	RSVD	Reserved Pin	-	-	-	-	-
A87	RSVD	Reserved Pin	-	-	-	-	-
A88	PCIE_CLK_REF+	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A89	PCIE_CLK_REF-	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A90	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A91	SPI_POWER	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O	-	3.3V Suspend / 3.3V	-	-
A92	SPI_MISO	Data in to Module from Carrier SPI	I	CMOS	3.3V Suspend / 3.3V	-	-

A93	GPO0	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
A94	SPI_CLK	Clock from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A95	SPI_MOSI	Data out from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A96	TPM_PP	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I	CMOS	3.3V / 3.3V	-	-
A97	TYPE10#	Dual use pin. Indicates to the Carrier Board that a Type 10 module is installed. Indicates to the Carrier that a Rev 1.0/2.0 module is installed	-	-	-	-	-
A98	SER0_TX	General purpose serial port transmitter	O	CMOS	5V / 12V	Placeholder PD 4.7K	-
A99	SER0_RX	General purpose serial port receiver	I	CMOS	5V / 12V	PU 47K to 3.3V	-
A100	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O	CMOS	5V / 12V	Placeholder PD 4.7K	-
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I	CMOS	5V / 12V	PU 47K to 3.3V	-

A103	LID#	LID button. Low active signal used by the ACPI operating system for a LID switch.	I	CMOS	3.3V Suspend / 12V	PU 47K to 3VSB	-
A104	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A105	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A106	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A107	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A108	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A109	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A110	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B1	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B2	GBE0_ACT#	Gigabit Ethernet Controller 1 activity indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
B3	LPC_FRAME#	LPC frame indicates the start of an LPC cycle / Shared pin with ESPI_CS0#	O	CMOS	3.3V / 3.3V	PU 8.2k ohm to 3.3V	-
B4	LPC_AD0	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-

B5	LPC_AD1	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B6	LPC_AD2	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B7	LPC_AD3	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B8	LPC_DRQ0# / ESPI_ALERT0#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B9	LPC_DRQ1# / ESPI_ALERT1#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B10	LPC_CLK	LPC clock output - 33MHz nominal / Shared pin with ESPI_Clock	O	CMOS	3.3V / 3.3V	-	-
B11	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B12	PWRBTN#	Power button to bring system out of S5 (soft off), active on falling edge.	I	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
B13	SMB_CK	System Management Bus bidirectional clock line.	I/O	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-
B14	SMB_DAT	System Management Bus bidirectional data line.	I/O	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-

B15	SMB_ALERT#	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-
B16	SATA1_TX+	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B17	SATA1_TX-	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B18	SUS_STAT#	Indicates imminent suspend operation; used to notify LPC devices / Shared pin with ESPI_RESET	O	CMOS	3.3V Suspend / 3.3V	-	-
B19	SATA1_RX+	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B20	SATA1_RX-	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B22	PCIE_RX15+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B23	PCIE_RX15-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B24	PWR_OK	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or	I	CMOS	3.3V / 3.3V	-	-

		other configurable devices time to be programmed.					
B25	PCIE_RX14+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B26	PCIE_RX14-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B27	WDT	Output indicating that a watchdog time-out event has occurred.	O	CMOS	3.3V / 3.3V	-	-
B28	RSVD	Reserved Pin	-	-	-	-	-
B29	RSVD	Reserved Pin	-	-	-	-	-
B30	RSVD	Reserved Pin	-	-	-	-	-
B31	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B32	SPKR	Output for audio enunciator	O	CMOS	3.3V / 3.3V	-	-
B33	I2C_CK	General purpose I2C port clock output	I/O	CMOS	3.3V Suspend / 3.3V	PU 2.2k ohm to 3.3V	-
B34	I2C_DAT	General purpose I2C port data I/O line	I/O	CMOS	3.3V Suspend / 3.3V	PU 2.2k ohm to 3.3V	-
B35	THRM#	Input from off-Module temp sensor indicating an over-temp situation	I	CMOS	3.3V / 3.3V	PU 1k ohm to 3VSB	-
B36	PCIE_RX13+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B37	PCIE_RX13-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

B38	GND	GND	-	-	-	-	-
B39	PCIE_RX12+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B40	PCIE_RX12-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B41	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B42	USB3-	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B43	USB3+	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B44	USB_0_1_OC#	USB over-current sense, USB channels 0 and 1. A pull-up for this line shallbe present on the Module. Do not pull this line high on the Carrier Board	I	CMOS	3.3V Suspend / 3.3V	PU 10 kohm to 3VSB	-
B45	USB1-	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B46	USB1+	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-

B47	ESPI_EN	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If pulled down by the Carrier LPC mode is selected. If pulled up or left floating, eSPI is selected if available. This signal is pulled up on the Module. This signal is a “don’t care” for Modules that do not support eSPI	I	CMOS	NA	-	-
B48	USB0_HOST_PRSNT	Module USB client may may detect the presence of a USB host on USB0. A high value indicates that a host is present.	I	CMOS	3.3V Suspend/ 3.3V	-	-
B49	SYS_RESET#	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used	I	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-

B50	CB_RESET#	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and mayresult from a low SYS_RESET#input, a low PWR_OKinput, a VCC_12Vpower input that falls below the minimum specification, a watchdog timeout, or maybe initiated by the Module software.	O	CMOS	3.3V Suspend / 3.3V	PU 1k ohm to 3VSB (OD)	-
B51	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B52	PCIE_RX5+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B53	PCIE_RX5-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B54	GPO1	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B55	PCIE_RX4+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B56	PCIE_RX4-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B57	GPO2	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B58	PCIE_RX3+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

B59	PCIE_RX3-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B60	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B61	PCIE_RX2+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B62	PCIE_RX2-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B63	GPO3	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B64	PCIE_RX1+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B65	PCIE_RX1-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B66	WAKE0#	PCI Express wake up signal.	I	CMOS	3.3V Suspend / 3.3V	PU 1k ohm to 3VSB	-
B67	WAKE1#	General purpose wake up signal. Maybe used to implement wake-up on PS2 keyboard or mouse activity	I	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
B68	PCIE_RX0+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B69	PCIE_RX0-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B70	GND(FIXED)	GND(FIXED)	-	-	-	-	-

B71	PCIE_RX8+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B72	PCIE_RX8-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B73	GND	GND	-	-	-	-	-
B74	PCIE_RX9+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B75	PCIE_RX9-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B76	GND	GND	-	-	-	-	-
B77	PCIE_RX10+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B78	PCIE_RX10-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B79	GND	GND	-	-	-	-	-
B80	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B81	PCIE_RX11+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B82	PCIE_RX11-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B83	GND	GND	-	-	-	-	-
B84	VCC_5V_SBY	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B85	VCC_5V_SBY	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B86	VCC_5V_SBY	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-

B87	VCC_5V_SBY	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B88	BIOS_DIS1#	Selection straps to determine the BIOS boot device.The Carrier should only float these or pull them low / Shared pin with ESPI_BBS	I	CMOS	NA	PU 10k ohm to 3.3V	-
B89	NCSI_RX_ER	NC-SI Receive error	O	-	3.3V Suspend / 3.3V	-	-
B90	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B91	NCSI_CLK_IN	NC-SI Clock reference for receive, transmit, and control lnterface. (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	-	-
B92	NCSI_RXD1	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	PU 5.1K to 1.05V	-
B93	NCSI_RXD0	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	PU 5.1K to 1.05V	-
B94	NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O	-	3.3V Suspend / 3.3V	PD 270 ohm	-
B95	NCSI_TXD1	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PU 10K to 1.05V	-

B96	NCSI_TXD0	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PU 10K to 1.05V	-
B97	SPI_CS#	Chip select for Carrier Board SPI - maybe sourced from chipset SPI0 or SPI1	O	CMOS	3.3V Suspend / 3.3V	-	-
B98	NCSI_ARB_IN	NC-SI hardware arbitration input.	I	-	3.3V Suspend / 3.3V	PD 10k ohm	-
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output.	O	-	3.3V Suspend / 3.3V	PU 10K to 1.05V	-
B100	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B101	FAN_PWNOUT	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM	O	CMOS	3.3V / 12V	PU 10K to 3.3V	-
B102	FAN_TACHIN	Fan tachometer input for a fan with a two pulse output.	I	CMOS	3.3V / 12V	PU 10K to 3.3V	-
B103	SLEEP#	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I	CMOS	3.3V Suspend / 12V	PU 10K to 3VSB	-
B104	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B105	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B106	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-

B107	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B108	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B109	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B110	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C1	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C2	GND	GND	-	-	-	-	-
C3	USB_SSRX0-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C4	USB_SSRX0+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C5	GND	GND	-	-	-	-	-
C6	USB_SSRX1-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C7	USB_SSRX1+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C8	GND	GND	-	-	-	-	-
C9	USB_SSRX2-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-

C10	USB_SSRX2+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C11	GND(FIXED)					-	-
C12	USB_SSRX3-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C13	USB_SSRX3+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C14	GND	GND	-	-	-	-	-
C15	10G_PHY_MDC_SCL3	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C16	10G_PHY_MDC_SCL2	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-

C17	10G_SDP2	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	-	-
C18	GND	GND	-	-	-	-	-
C19	PCIE_RX6+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C20	PCIE_RX6-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C22	PCIE_RX7+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C23	PCIE_RX7-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C24	10G_INT2	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	-	-
C25	GND	GND	-	-	-	-	-
C26	10G_KR_RX3+	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C27	10G_KR_RX3-	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C28	GND	GND	-	-	-	-	-
C29	10G_KR_RX2+	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C30	10G_KR_RX2-	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C31	GND(FIXED)	GND(FIXED)	-	-	-	-	-

C32	10G_SFP_SDA3	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	-	-
C33	10G_SFP_SDA2	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	-	-
C34	10G_PHY_RST_23	Output signal that resets an optical PHY on port 2 and port3 (Not used with copper PHY)	O	-	3.3V Suspend / 3.3V	-	-
C35	10G_PHY_RST_01	Output signal that resets an optical PHY on port 0 and port1 (Not used with copper PHY)	O	-	3.3V Suspend / 3.3V	-	-
C36	10G_LED_SDA	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.	I/O	OD	3.3V Suspend / 3.3V	-	-
C37	10G_LED_SCL	I2C Clock,of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs	I/O	OD	3.3V Suspend / 3.3V	-	-

C38	10G_SFP_SDA1	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 4.7K to 3VSB	-
C39	10G_SFP_SDA0	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 4.7K to 3VSB	-
C40	10G_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	PU 1K to 3VSB	-
C41	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C42	10G_KR_RX1+	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C43	10G_KR_RX1-	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C44	GND	GND	-	-	-	-	-
C45	10G_PHY_MDC_SCL1	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-

C46	10G_PHY_MDC_SCL0	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C47	10G_INT0	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	-	-
C48	GND	GND	-	-	-	-	-
C49	10G_KR_RX0+	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C50	10G_KR_RX0-	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C51	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C52	PCIE_RX16+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C53	PCIE_RX16-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C54	TYPE0#	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	-	-
C55	PCIE_RX17+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C56	PCIE_RX17-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C57	TYPE1#	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	-	-
C58	PCIE_RX18+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C59	PCIE_RX18-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C60	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C61	PCIE_RX19+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C62	PCIE_RX19-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C63	RSVD	Reserved Pin	-	-	-	-	-
C64	RSVD	Reserved Pin	-	-	-	-	-
C65	PCIE_RX20+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C66	PCIE_RX20-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C67	RAPID_SHUTDOWN	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for a	I	CMOS	5.0V Suspend/ 5.0V	-	-
C68	PCIE_RX21+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C69	PCIE_RX21-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C70	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C71	PCIE_RX22+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C72	PCIE_RX22-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C73	GND	GND	-	-	-	-	-
C74	PCIE_RX23+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C75	PCIE_RX23-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C76	GND	GND	-	-	-	-	-
C77	RSVD	Reserved Pin	-	-	-	-	-
C78	PCIE_RX24+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C79	PCIE_RX24-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C80	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C81	PCIE_RX25+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C82	PCIE_RX25-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C83	RSVD	Reserved Pin	-	-	-	-	-
C84	GND	GND	-	-	-	-	-
C85	PCIE_RX26+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C86	PCIE_RX26-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C87	GND	GND	-	-	-	-	-
C88	PCIE_RX27+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C89	PCIE_RX27-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C90	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C91	PCIE_RX28+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C92	PCIE_RX28-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C93	GND	GND	-	-	-	-	-
C94	PCIE_RX29+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C95	PCIE_RX29-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C96	GND	GND	-	-	-	-	-
C97	RSVD	Reserved Pin	-	-	-	-	-
C98	PCIE_RX30+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C99	PCIE_RX30-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C100	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C101	PCIE_RX31+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C102	PCIE_RX31-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C103	GND	GND	-	-	-	-	-
C104	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C105	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C106	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C107	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C108	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C109	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C110	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D1	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D2	GND	GND	-	-	-	-	-
D3	USB_SSTX0-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D4	USB_SSTX0+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D5	GND	GND	-	-	-	-	-

D6	USB_SSTX1-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D7	USB_SSTX1+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D8	GND	GND	-	-	-	-	-
D9	USB_SSTX2-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D10	USB_SSTX2+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D11	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D12	USB_SSTX3-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D13	USB_SSTX3+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D14	GND	GND	-	-	-	-	-
D15	10G_PHY_MDIO_SDA3	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-

		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
D16	10G_PHY_MDIO_SDA2	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
D17	10G_SDP3	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	-	-
D18	GND	GND	-	-	-	-	-
D19	PCIE_TX6+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D20	PCIE_TX6-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D22	PCIE_TX7+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D23	PCIE_TX7-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

D24	10G_INT3	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	-	-
D25	GND	GND	-	-	-	-	-
D26	10G_KR_TX3+	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D27	10G_KR_TX3-	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D28	GND	GND	-	-	-	-	-
D29	10G_KR_TX2+	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D30	10G_KR_TX2-	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D31	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D32	10G_SFP_SCL3	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	-	-
D33	10G_SFP_SCL2	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	-	-

D34	10G_PHY_SEL_23	Phy mode select pin: If high Phy2 and Phy3 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode, this pin should be left not connected on the Carrier. For I2C mode pull down with 1K on Carrier	I	-	3.3V Suspend / 3.3V	-	-
D35	10G_PHY_SEL_01	Phy mode select pin: If high Phy0 and Phy1 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode, this pin should be left not connected on the Carrier. For I2C mode pull down with 1K on Carrier	I	-	3.3V Suspend / 3.3V	-	-
D36	RSVD	RSVD	-	-	-	-	-
D37	RSVD	RSVD	-	-	-	-	-
D38	10G_SFP_SCL1	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 4.7K to 3VSB	-
D39	10G_SFP_SCL0	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 4.7K to 3VSB	-

D40	10G_SDP1	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	PU 1K to 3VSB	-
D41	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D42	10G_KR_TX1+	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D43	10G_KR_TX1-	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D44	GND	GND	-	-	-	-	-
D45	10G_PHY_MDIO_SDA1	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
D46	10G_PHY_MDIO_SDA0	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-

D47	10G_INT1	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	-	-
D48	GND	GND	-	-	-	-	-
D49	10G_KR_TX0+	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D50	10G_KR_TX0-	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D51	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D52	PCIE_TX16+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D53	PCIE_TX16-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D54	RSVD	Reserved Pin	-	-	-	-	-
D55	PCIE_TX17+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D56	PCIE_TX17-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D57	TYPE2#	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	Connect to GND	-
D58	PCIE_TX18+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D59	PCIE_TX18-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D60	GND(FIXED)	GND(FIXED)	-	-	-	-	-

D61	PCIE_TX19+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D62	PCIE_TX19-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D63	RSVD	Reserved Pin	-	-	-	-	-
D64	RSVD	Reserved Pin	-	-	-	-	-
D65	PCIE_TX20+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D66	PCIE_TX20-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D67	GND	GND	-	-	-	-	-
D68	PCIE_TX21+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D69	PCIE_TX21-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D70	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D71	PCIE_TX22+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D72	PCIE_TX22-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D73	GND	GND	-	-	-	-	-
D74	PCIE_TX23+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D75	PCIE_TX23-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D76	GND	GND	-	-	-	-	-
D77	RSVD	Reserved Pin	-	-	-	-	-

D78	PCIE_TX24+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D79	PCIE_TX24-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D80	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D81	PCIE_TX25+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D82	PCIE_TX25-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D83	RSVD	Reserved Pin	-	-	-	-	-
D84	GND	GND	-	-	-	-	-
D85	PCIE_TX26+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D86	PCIE_TX26-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D87	GND	GND	-	-	-	-	-
D88	PCIE_TX27+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D89	PCIE_TX27-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D90	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D91	PCIE_TX28+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D92	PCIE_TX28-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D93	GND	GND	-	-	-	-	-

D94	PCIE_TX29+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D95	PCIE_TX29-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D96	GND	GND	-	-	-	-	-
D97	RSVD	Reserved Pin	-	-	-	-	-
D98	PCIE_TX30+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D99	PCIE_TX30-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D100	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D101	PCIE_TX31+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D102	PCIE_TX31-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D103	GND	GND	-	-	-	-	-
D104	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D105	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D106	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D107	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D108	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-

D109	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D110	GND(FIXED)	GND(FIXED)	-	-	-	-	-

Table 8 Pin out description

6 BIOS Setup Items

PCOM-B701GT is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, PCOM-B701GT communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

6.1 Entering Setup -- Launch System Setup

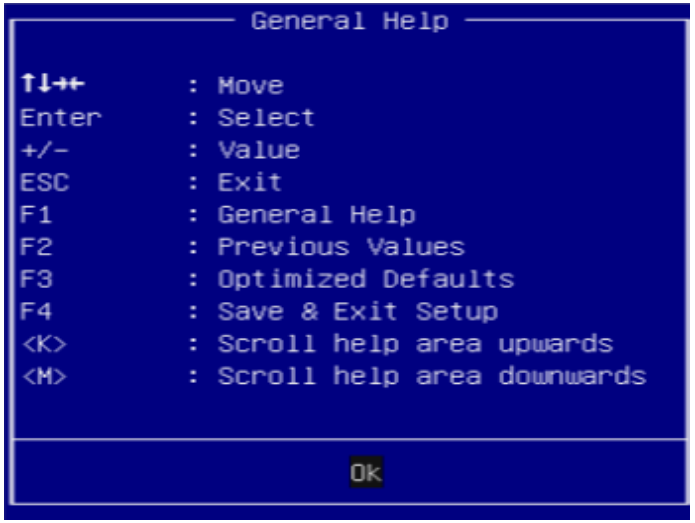
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



6.2 Main

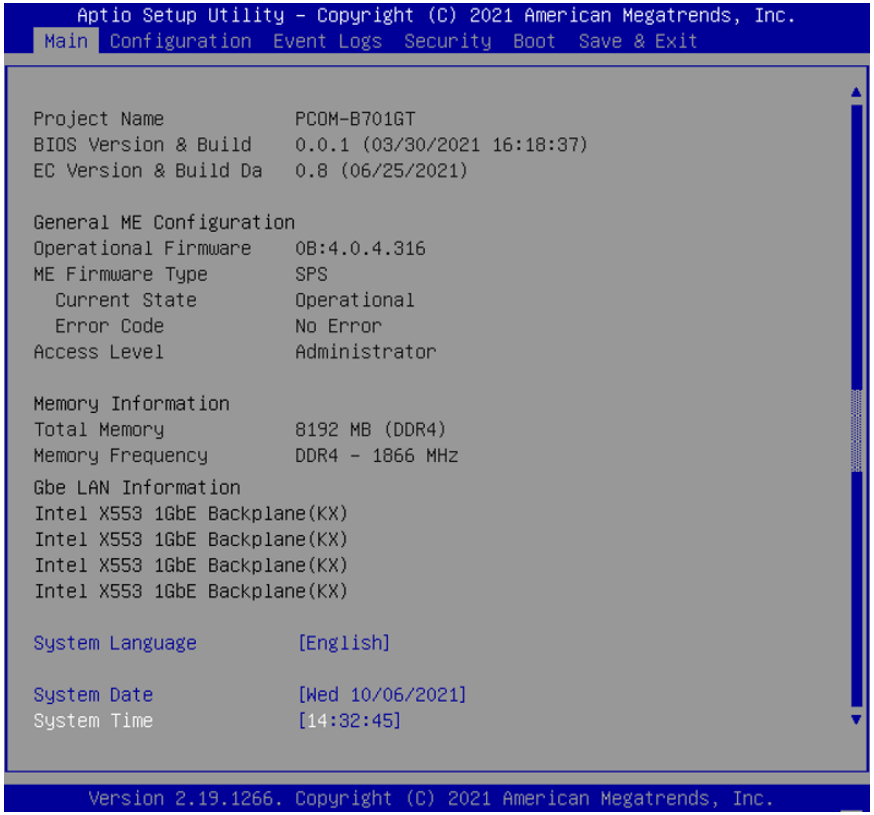


Figure 14 BIOS MAIN

Feature	Description	Options
System Date	The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.	
System Time	The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.	

6.3 Configuration

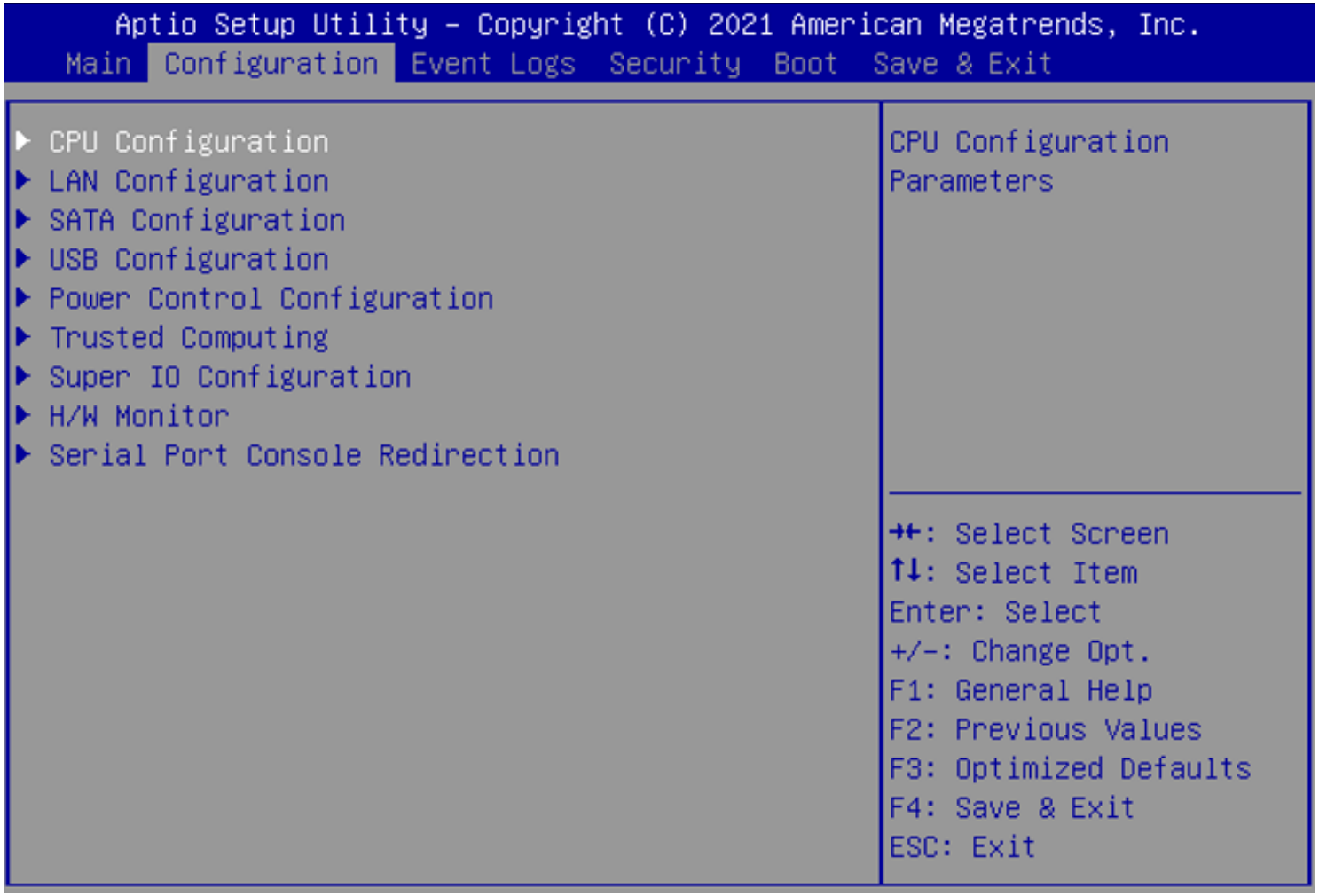


Figure 15 BIOS CONFIGURATION

CPU

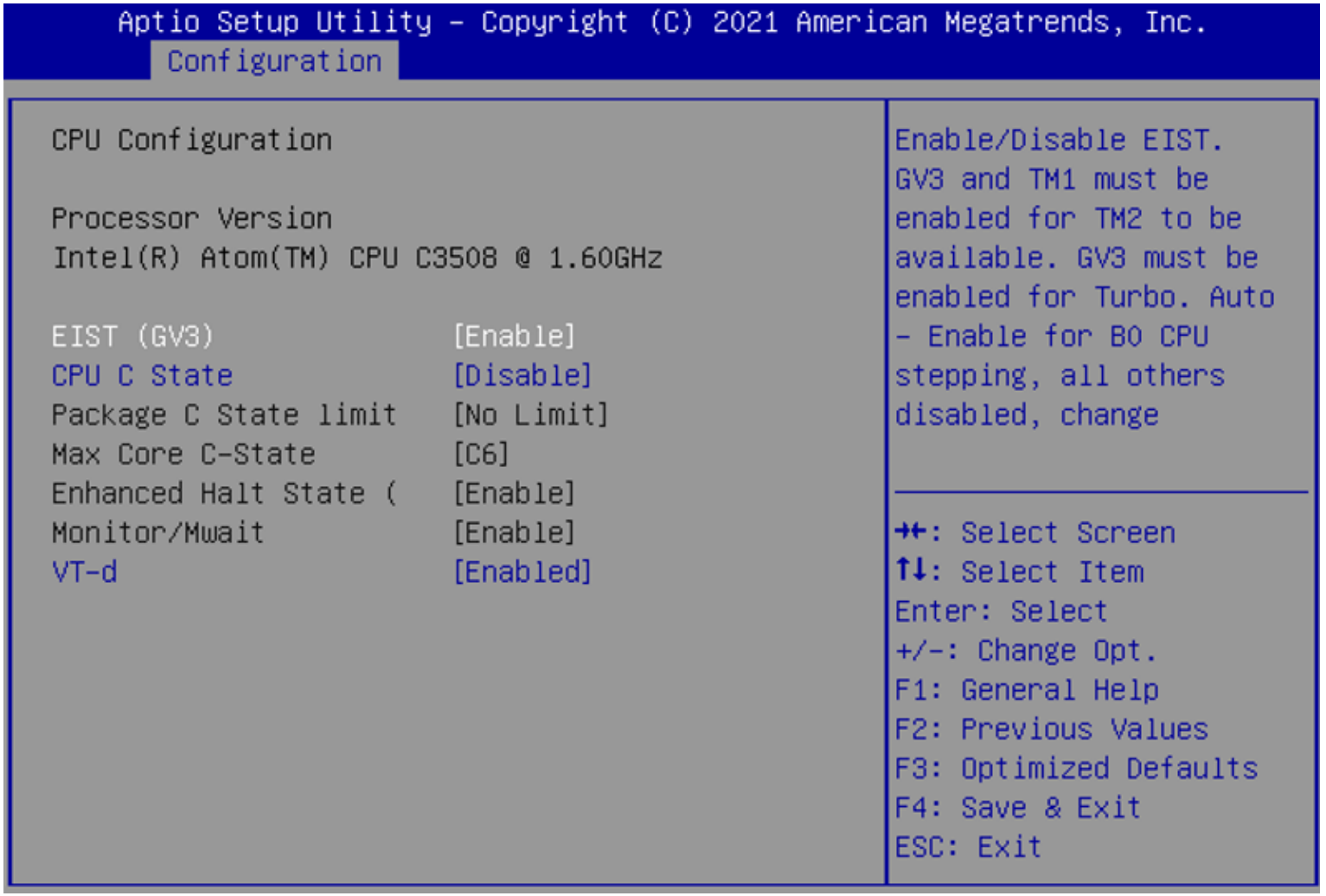


Figure 16 CPU

Feature	Description	Options
EIST (GV3)	Enable / Disable EIST. GV3 and TM1 must be enabled for TM2 to be available. GV3 must be enabled for Turbo. Auto – Enable for B0 CPU stepping, all others disabled, change	★Enabled, Disabled
CPU C State	Enables the Enhanced Cx state of the CPU, takes effect after reboot. Auto – Enable for B0 CPU stepping, all others disabled, change setting to override.	Enabled, ★Disabled
Package C State limit	Package C State limit	★No Limit, No Pkg C-State No S0Ix
Max Core C-State	Options are: C1 and C6.	★C6, C1
Enhanced Halt State	Enables the Enhanced C1E state of the CPU, takes effect after reboot.	★Enabled, Disabled
Monitor / Mwait	Enable or Disable the Monitor / Mwait instruction	★Enabled, Disabled
VT-d	COption to Enable / Disable VT-d	★Enabled, Disabled

LAN

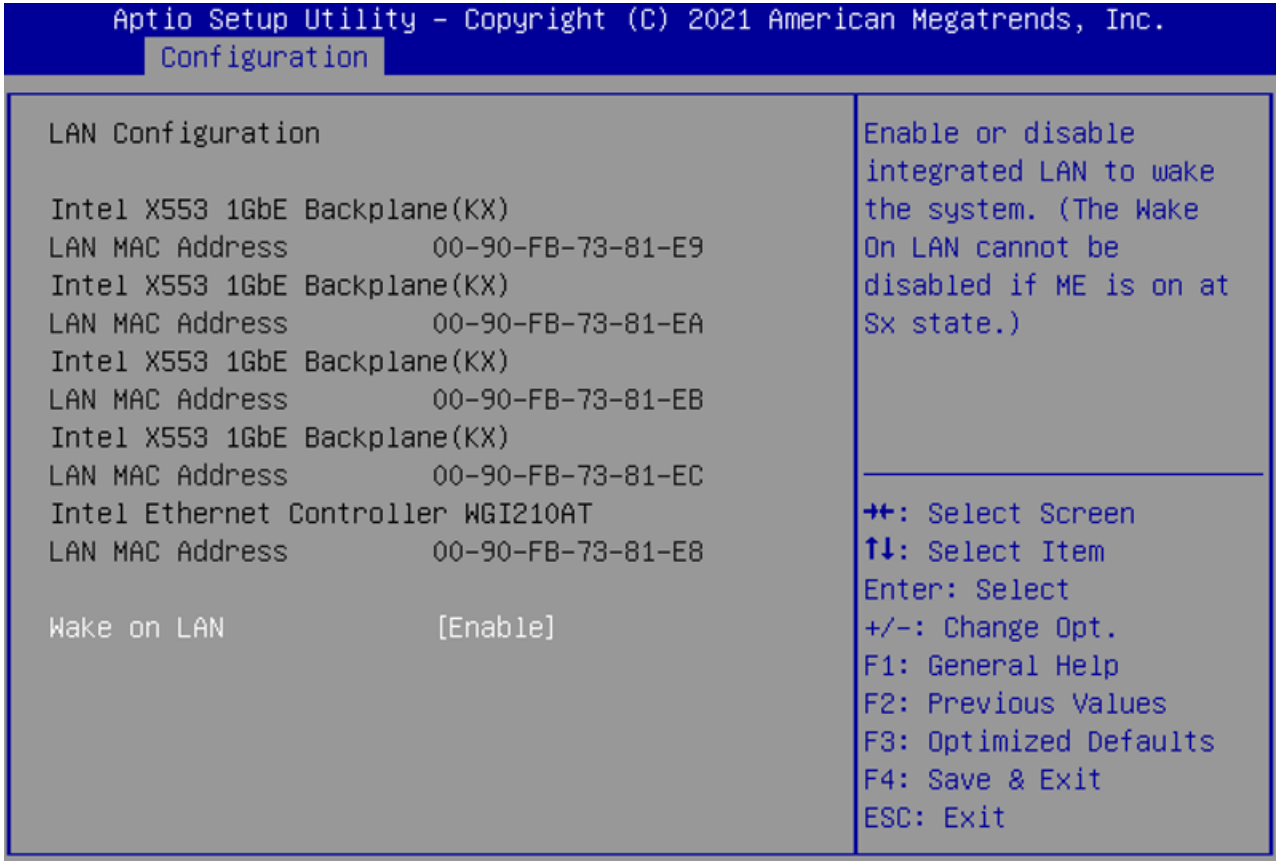


Figure 17 LAN

Feature	Description	Options
Wake On LAN	Enable or Disable integrated LAN to wake the system. (The wake on LAN cannot be disabled if ME is on at Sx state.)	★Enabled , Disabled

SATA

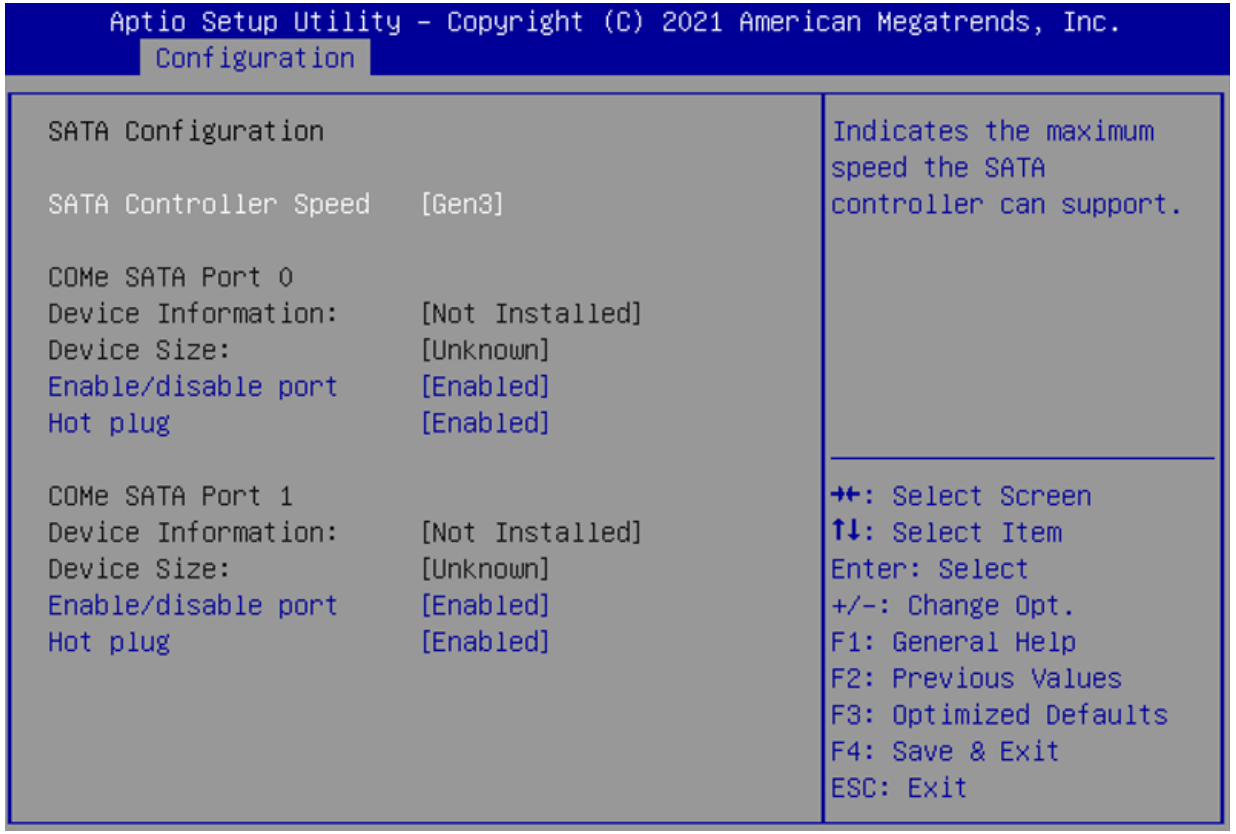


Figure 18 BIOS SATA

Feature	Description	Options
SATA Controller speed	Indicates the maximum speed the SATA controller can support.	★Gen3, Default, Gen1, Gen2
Enable / disable port	Enables / Disables SATA Controller port if supported by current cpu SKU.	★Enabled , Disabled
Hot plug	Hot plug	★Enabled , Disabled

USB

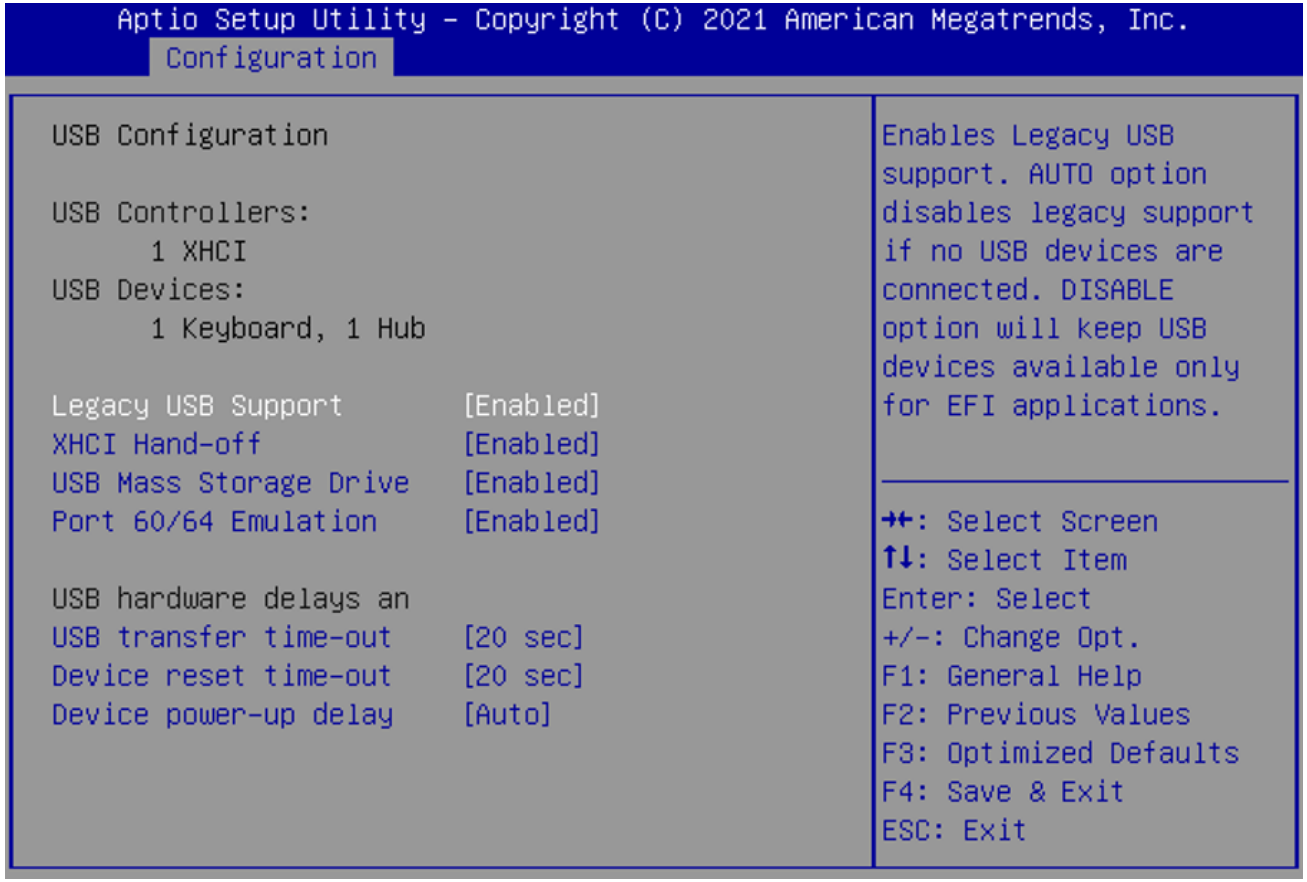


Figure 19 BIOS USB

Feature	Description	Options
Legacy USB Support	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI application	★Enabled , Disabled, Auto
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver	★Enabled , Disabled
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support	★Enabled , Disabled
Port 60/64 Emulation	Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.	★Enabled , Disabled
USB transfer time-out	The time-out value for Control, Bulk, and Interrupt transfers.	1, 5, 10, ★20 sec
Device reset time-out	USB mass storage device Start Unit command time-out.	10, ★20, 30, 40 sec
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. 'AUTO' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken	★AUTO, Manual
Device power-up delay	Delay range is 1~40 seconds, in one second increments.	★5

Power control

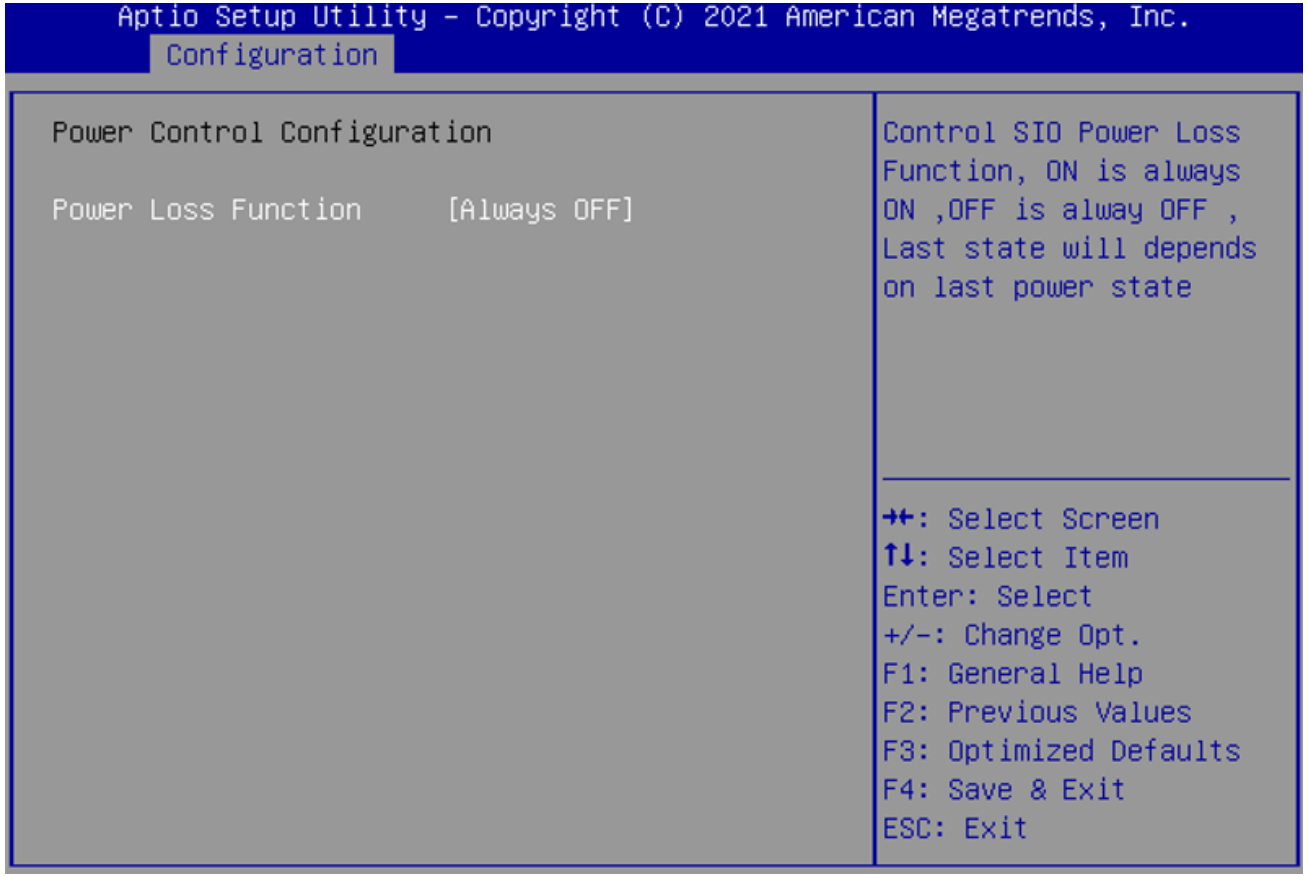


Figure 20 BIOS Power Control

Feature	Description	Options
Power Loss Function	Control SIO Power Loss Function, ON is always ON, OFF is always OFF, Last state will depends on last power state.	★Always OFF, Always ON, Last State

TPM

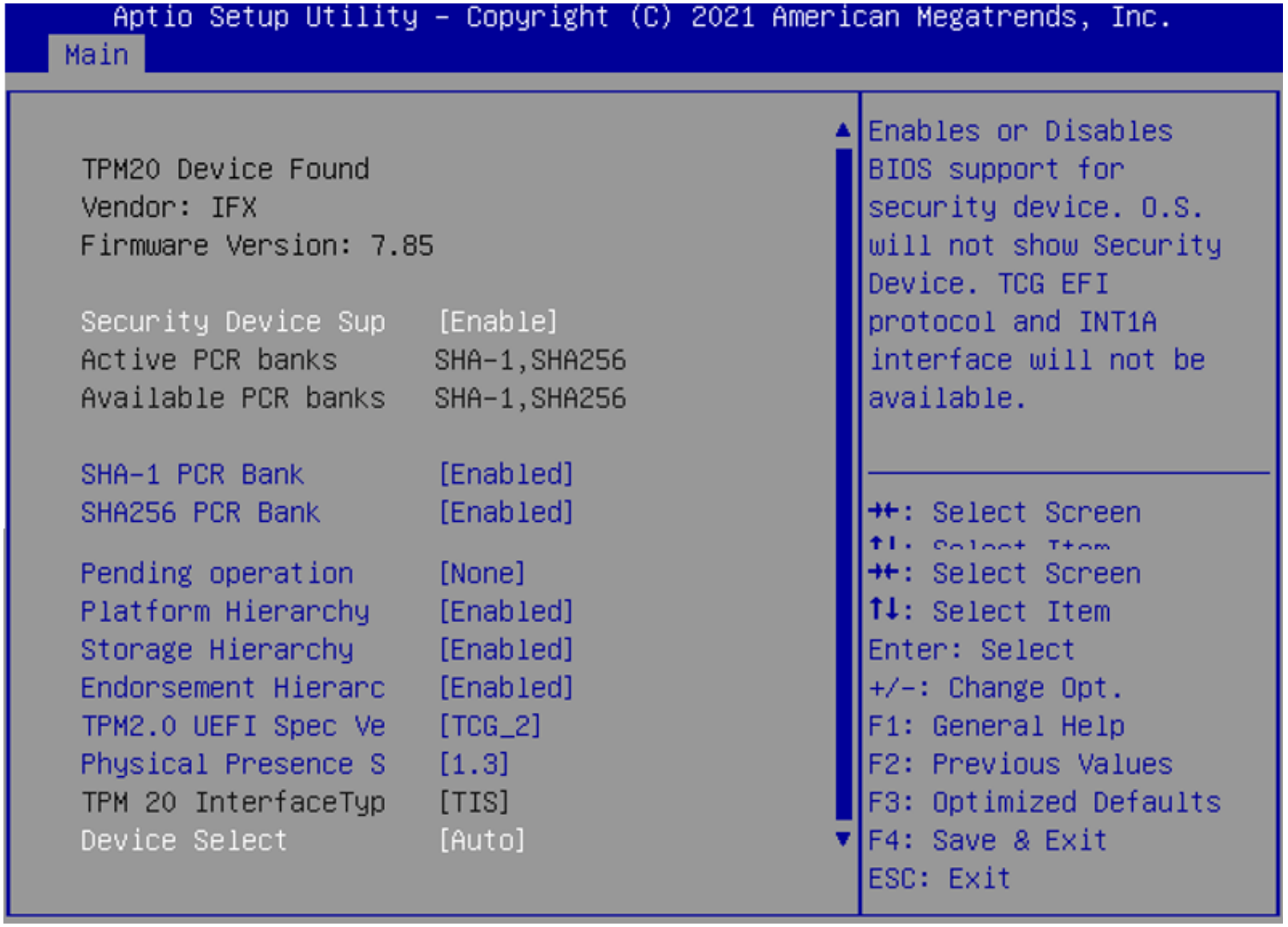


Figure 21 BIOS TPM

Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A Interface will not be available.	★Enabled, Disabled
SHA-1 PCR Bank	Enable or Disable SHA-1 PCR Bank	★Enabled, Disabled
SHA256 PCR Bank	Enable or Disable SHA256 PCR Bank	★Enabled, Disabled
Pending operation	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.	★None, TPM Clear
Platform Hierarchy	Enable or Disable Platform Hierarchy	★Enabled, Disabled
Storage Hierarchy	Enable or Disable Storage Hierarchy	★Enabled, Disabled
Endorsement Hierarchy	Enable or Disable Endorsement Hierarchy	★Enabled, Disabled
TPM2.0 UEFI Spec Version	Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8 / Win10, TCG_2: Support new TCG2 protocol and event	★TCG_2, TCG_1_2
Physical Presence Spec Version	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.	★1.3 1.2
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found.	★Auto, TPM 2.0, TPM 1.2

Super IO

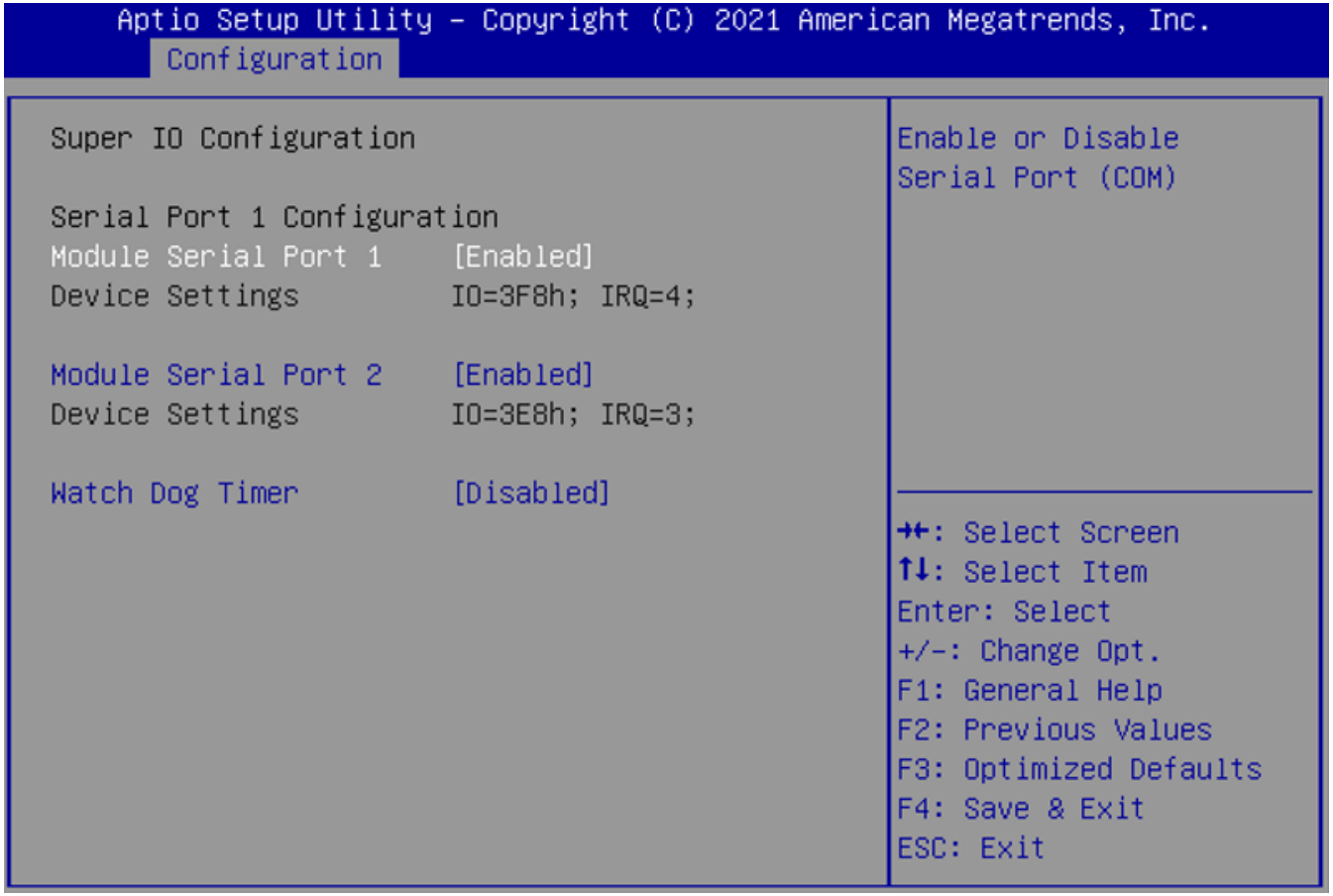


Figure 22 BIOS Super IO

Feature	Description	Options
Module Serial Port	Enable or Disable Serial Port (COM)	★Enabled, Disabled
Watch Dog Timer	Enable/Disable Watch Dog Timer	★Disabled, Enabled
Timer Unit	Select Timer count unit of WDT	★Second, Minute
Timer value	Set WDT Timer value seconds / minutes	★20

HW Monitor

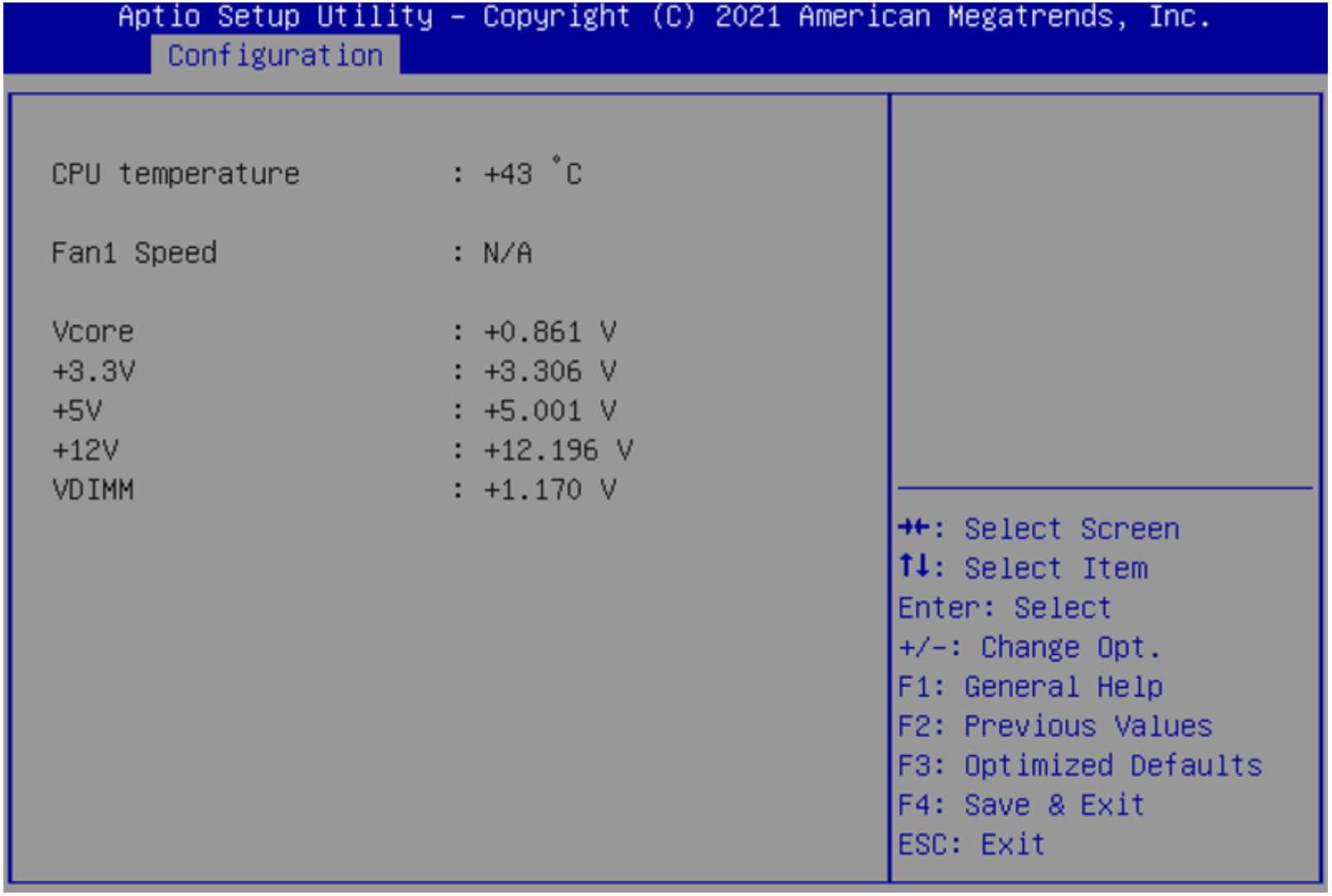


Figure 23 BIOS HW Monitor

Serial Port Console Redirection

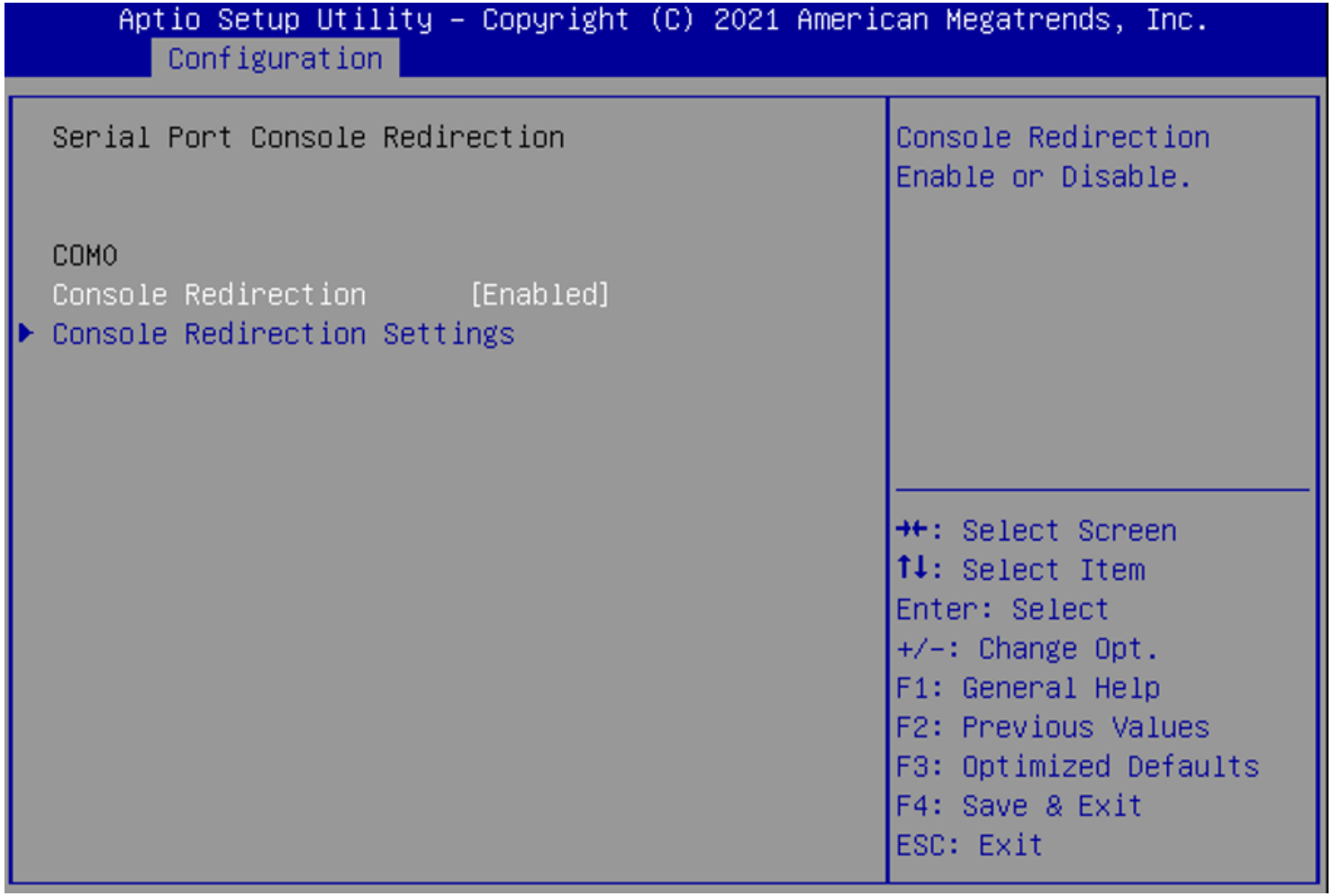
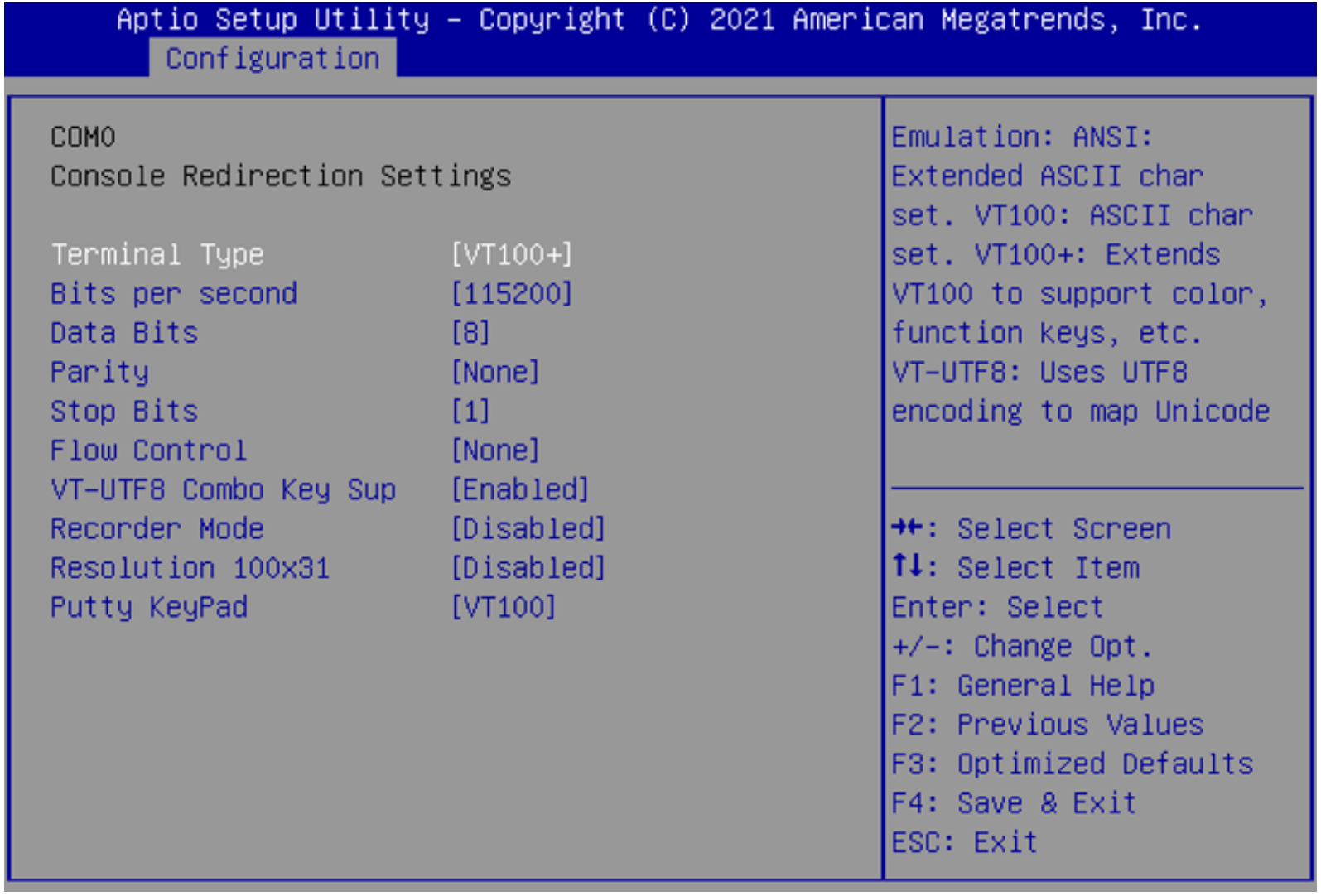


Figure 24 BIOS Serial Port

Feature	Description	Options
Console Redirection	Console Redirection Enable or Disable	★Enabled, Disabled


Aptio Setup Utility – Copyright (C) 2021 American Megatrends, Inc.
Configuration
COM0
Console Redirection Settings
Terminal Type [VT100+]
Bits per second [115200]
Data Bits [8]
Parity [None]
Stop Bits [1]
Flow Control [None]
VT-UTF8 Combo Key Sup [Enabled]
Recorder Mode [Disabled]
Resolution 100x31 [Disabled]
Putty KeyPad [VT100]
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color , function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★VT100+, VT100, ANSI, VT-UTF8
Bits per second	Select Serial port transmission speed. The speed must be matched on other side. Long or noisy lines may require lower speeds.	★115200, 9600, 19200, 38400, 57600
Data bits	Data bits	★8, 7
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★None, Even, Odd, Mark, Space
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1,2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signal.	★None, Hardware RTS/CTS
VT-UTF8 Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI / VT100 terminals	★Enabled, Disabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★Disabled, Enabled
Putty KeyPad	Select FunctionKey and KeyPad on Putty.	★VT100, LINUX, XTERMR6, SCO, ESCN, VT400

6.4 Event Logs

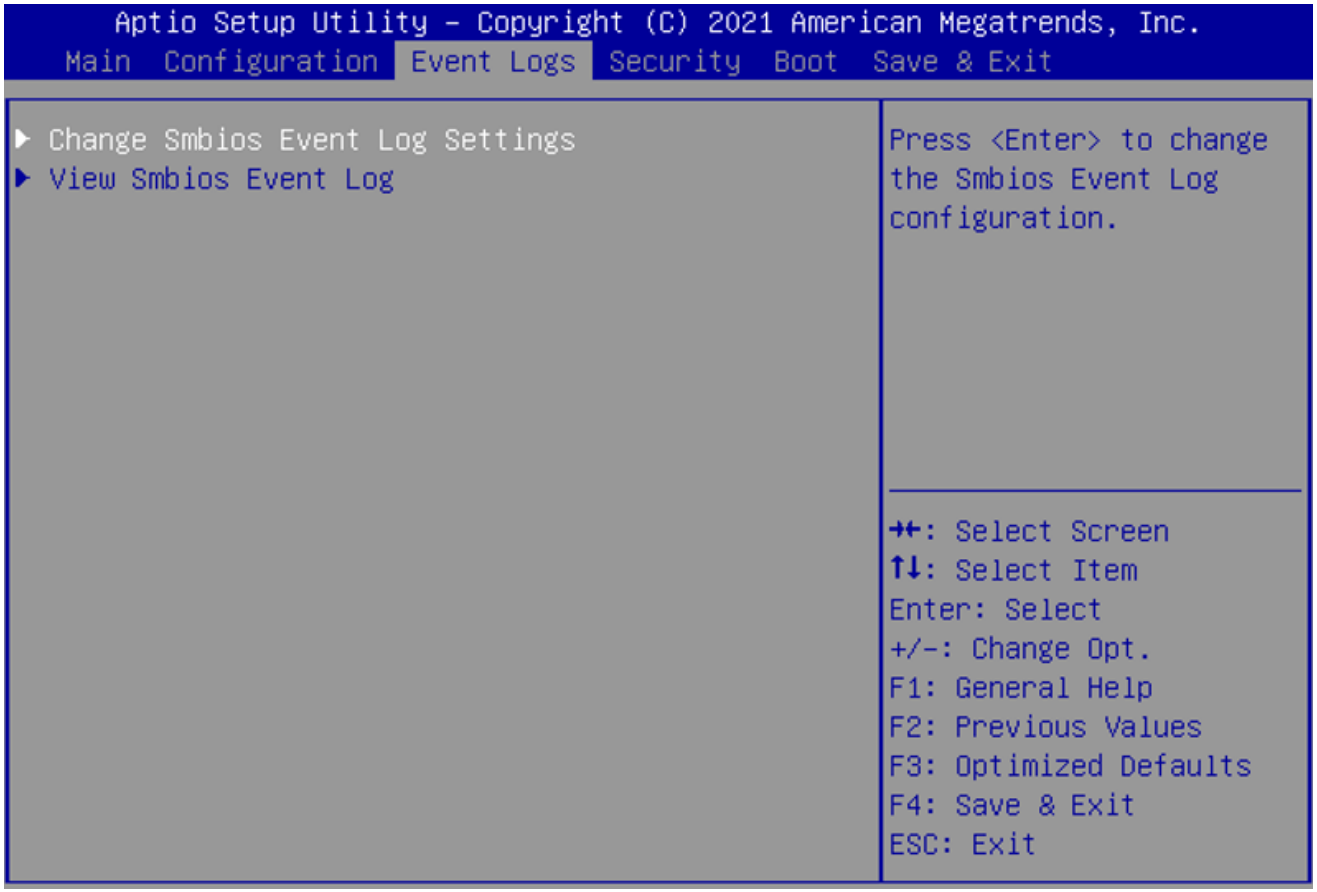


Figure 25 BIOS Event Log

Feature	Description	Options
Change Smbios Event Log Settings	Press <Enter> to change the Smbios Event Log configuration	
View Smbios Event Log	Press <Enter> to view the Smbios Event Log records	

Change Smbios Event Log Settings

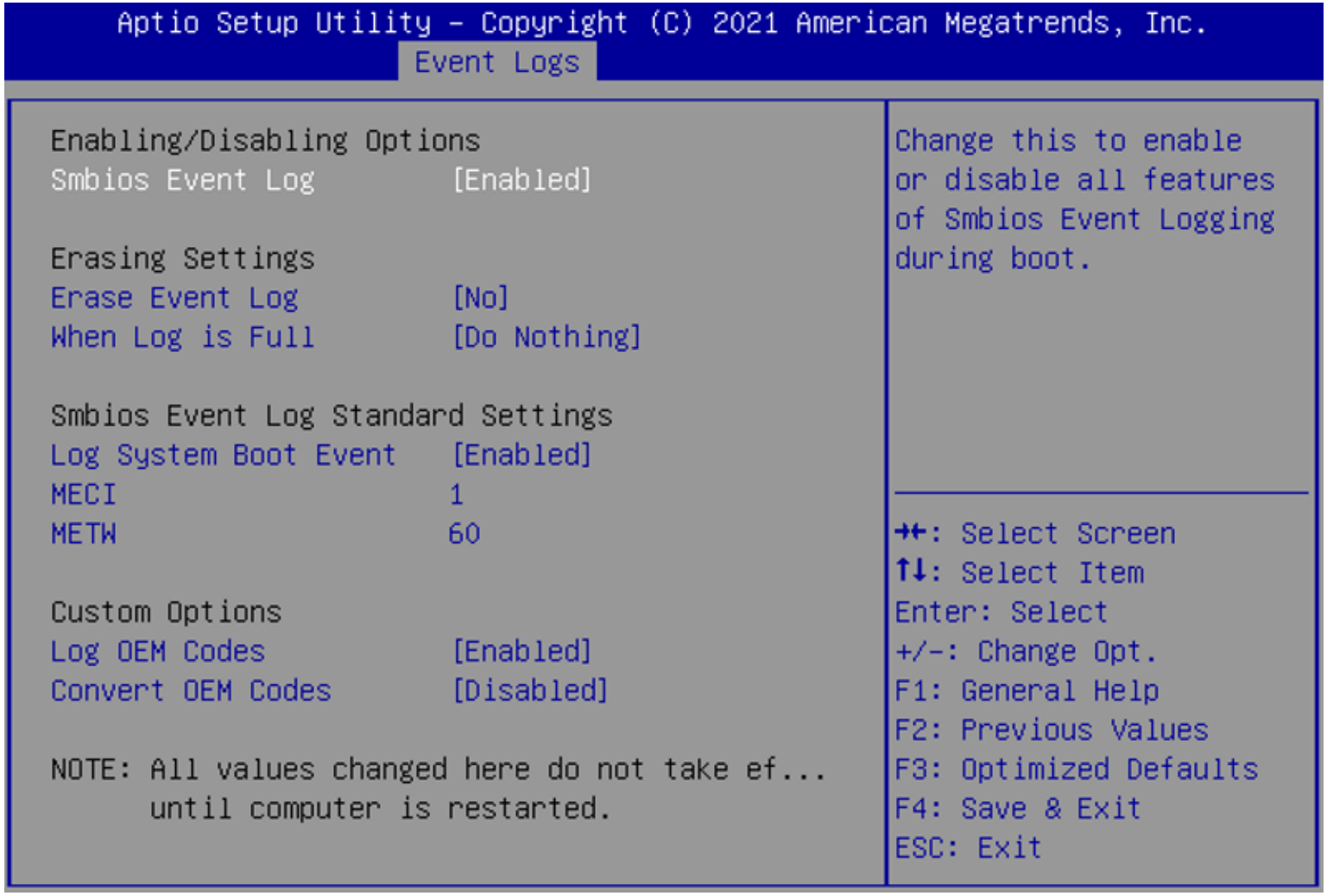


Figure 26 BIOS Event Log Settings

Feature	Description	Options
Smbios Event Log	Change this to enable or disable all features of Smbios Event Logging during boot.	★Enabled, Disabled
Erase Event Log	Choose options for erasing Smbios Event Log. Erasing is done prior to any logging activation during reset.	★No, Yes Next reset, Yes Every reset
When Log is Full	Choose options for reactions to a full Smbios Event Log.	★Do Nothing, Erase Immediately
Log System Boot Event	Choose option to enable / disable logging of System boot event.	★Enabled, Disabled
MECI	Multiple Event Count Increment: The number of occurrences of a duplicate event that must pass before the multiple-event counter of log entry is updated.	★1
METW	Multiple Event Time Window: The number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes.	★60
Log OEM Codes	Enable or disable the logging of EFI Status Codes as OEM Codes (if not already converted to legacy)	★Enabled, Disabled
Convert OEM Codes	Enable or disable the converting of EFI Status Codes to Standard Smbios Types (Not all may be translated).	Enabled, ★Disabled

View Smbios Event Log

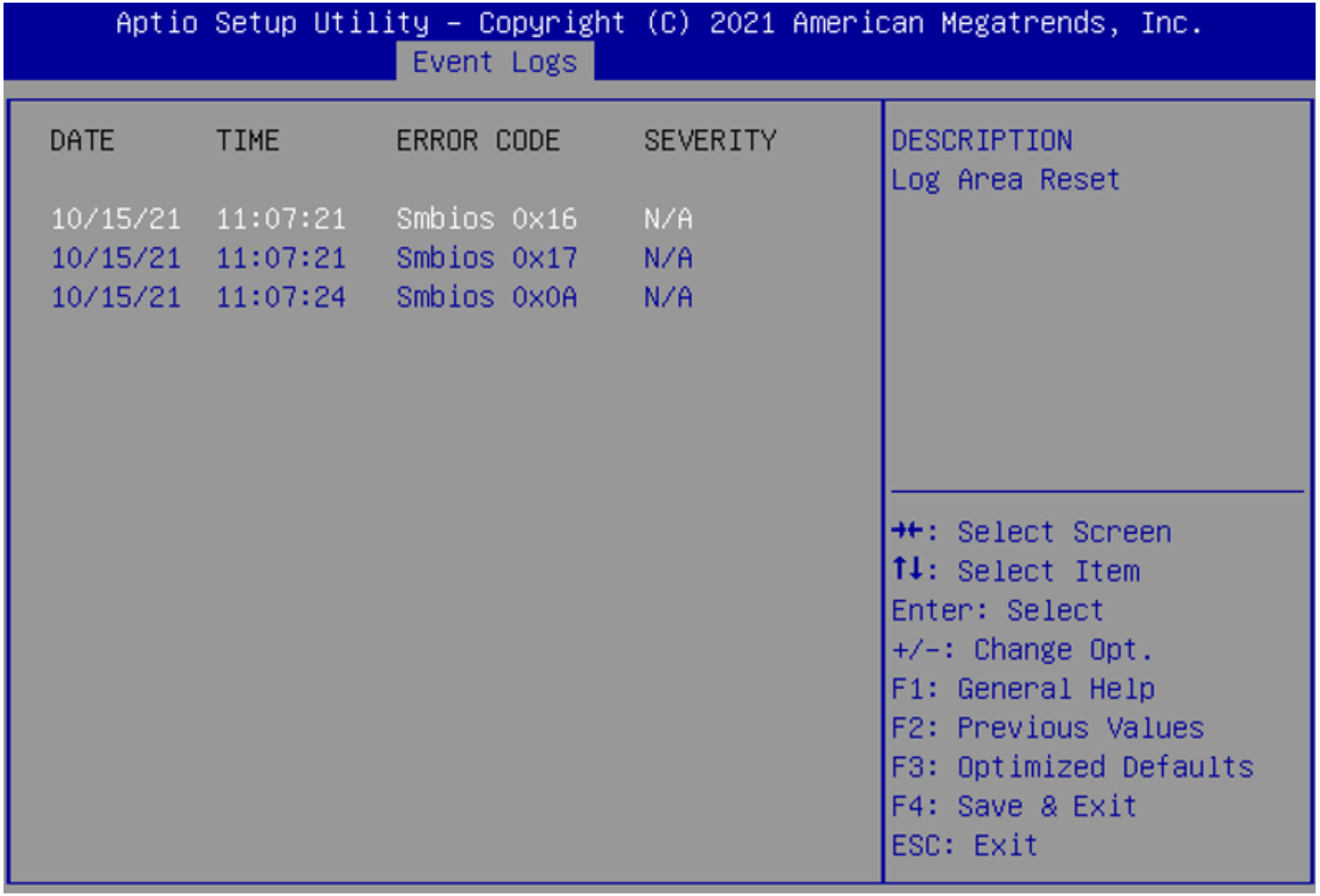


Figure 27 BIOS Smbios Event Log

6.5 Security

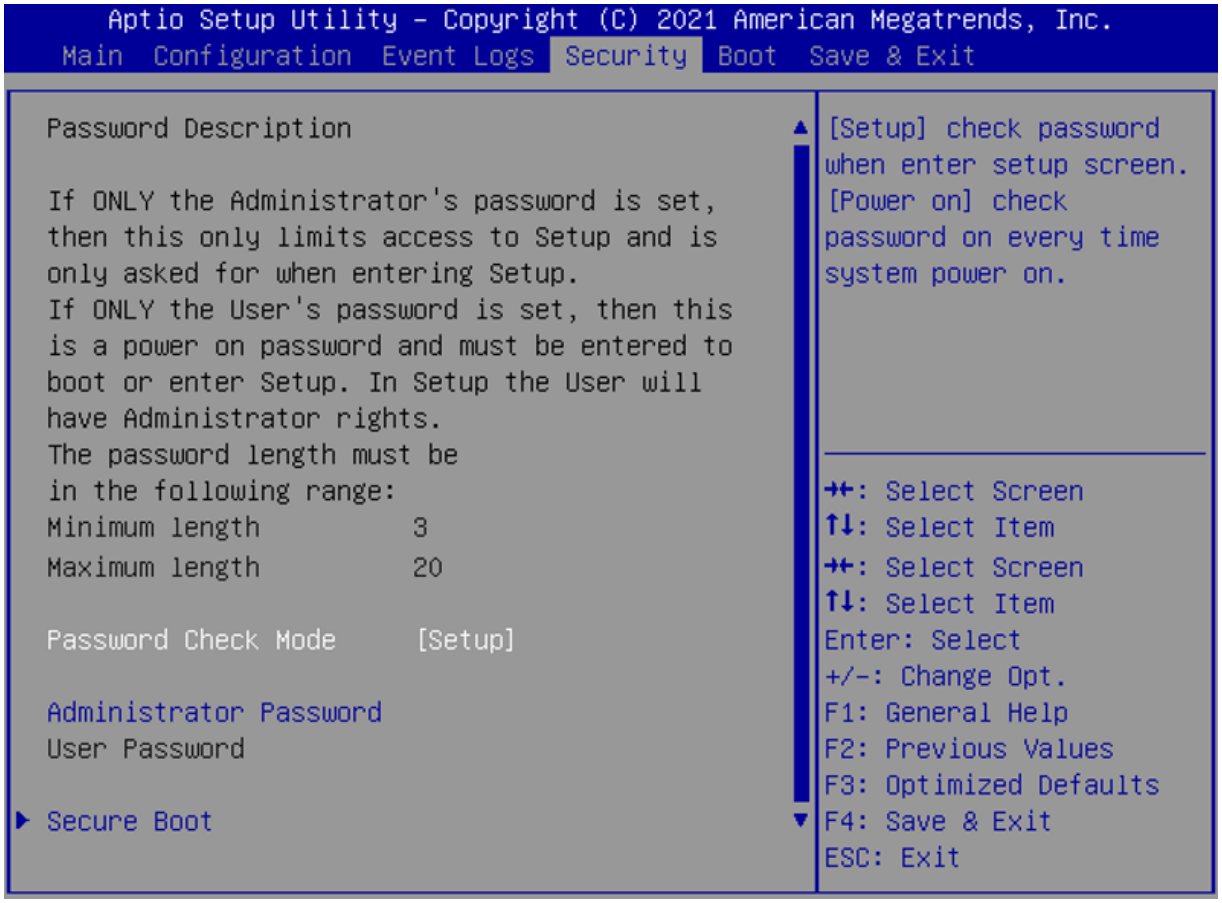


Figure 28 BIOS Security

Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★Setup, Power On
Administrator Password	Set Administrator Password	
Secure Boot	Customizable Secure Boot settings	

Secure Boot

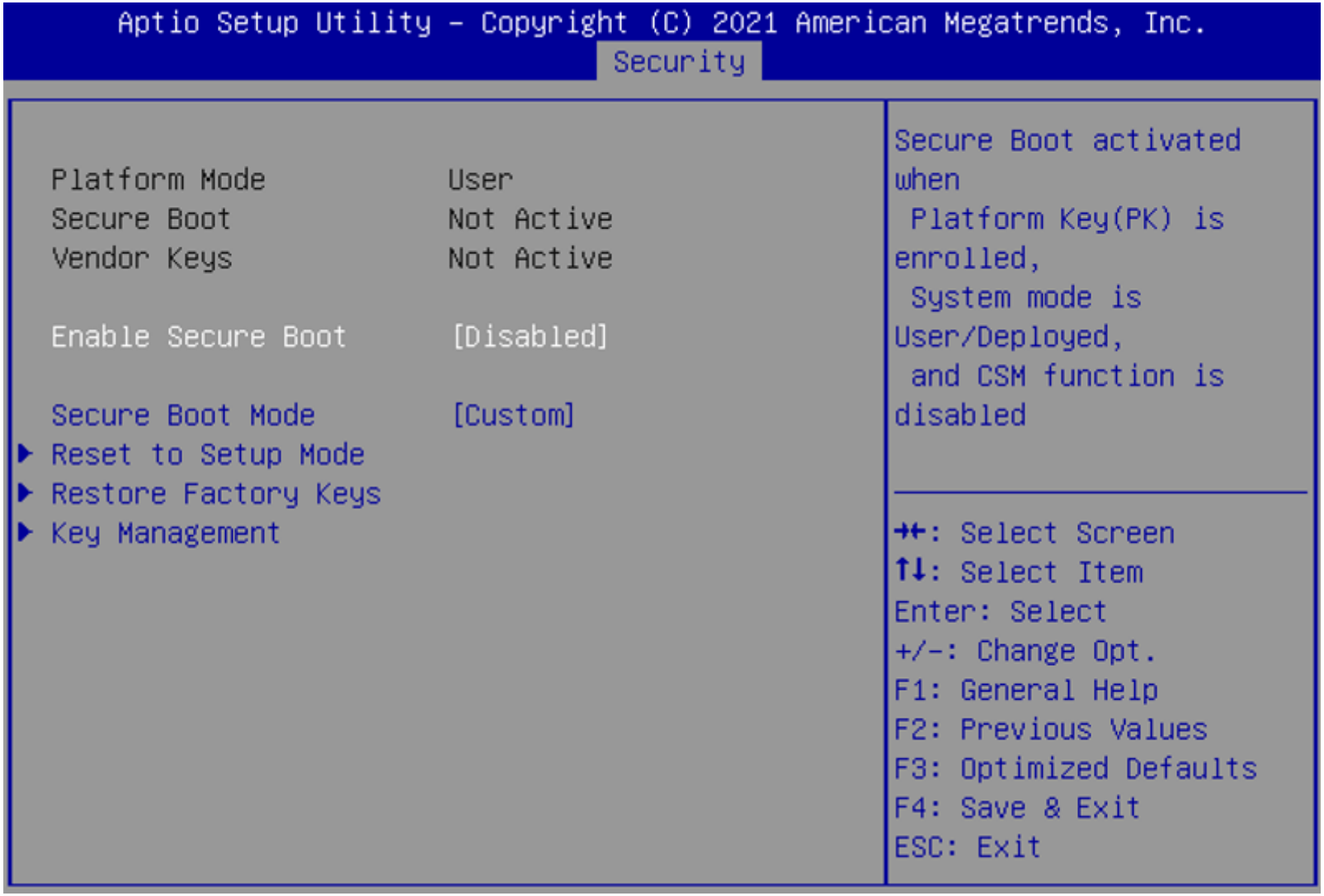


Figure 29 BIOS Secure Boot

Feature	Description	Options
Enable Secure Boot	Secure Boot activated when Platform Key(PK) is enrolled, System mode is User / Deployed, and CSM function is disabled	Enabled, ★Disabled
Secure Boot Mode	Secure Boot mode selector: Standard / Custom. In Custom mode Secure Boot variables can be configured without authentication	★Custom, Standard
Reset to Setup Mode	Force system to setup mode – delete all Secure Boot Key databases	
Install factory defaults	Force system to user mode – restore factory default Secure Boot Key databases.	
Key Management	Enables expert users to modify Scure Boot Policy variables without full authentication	

Key Management

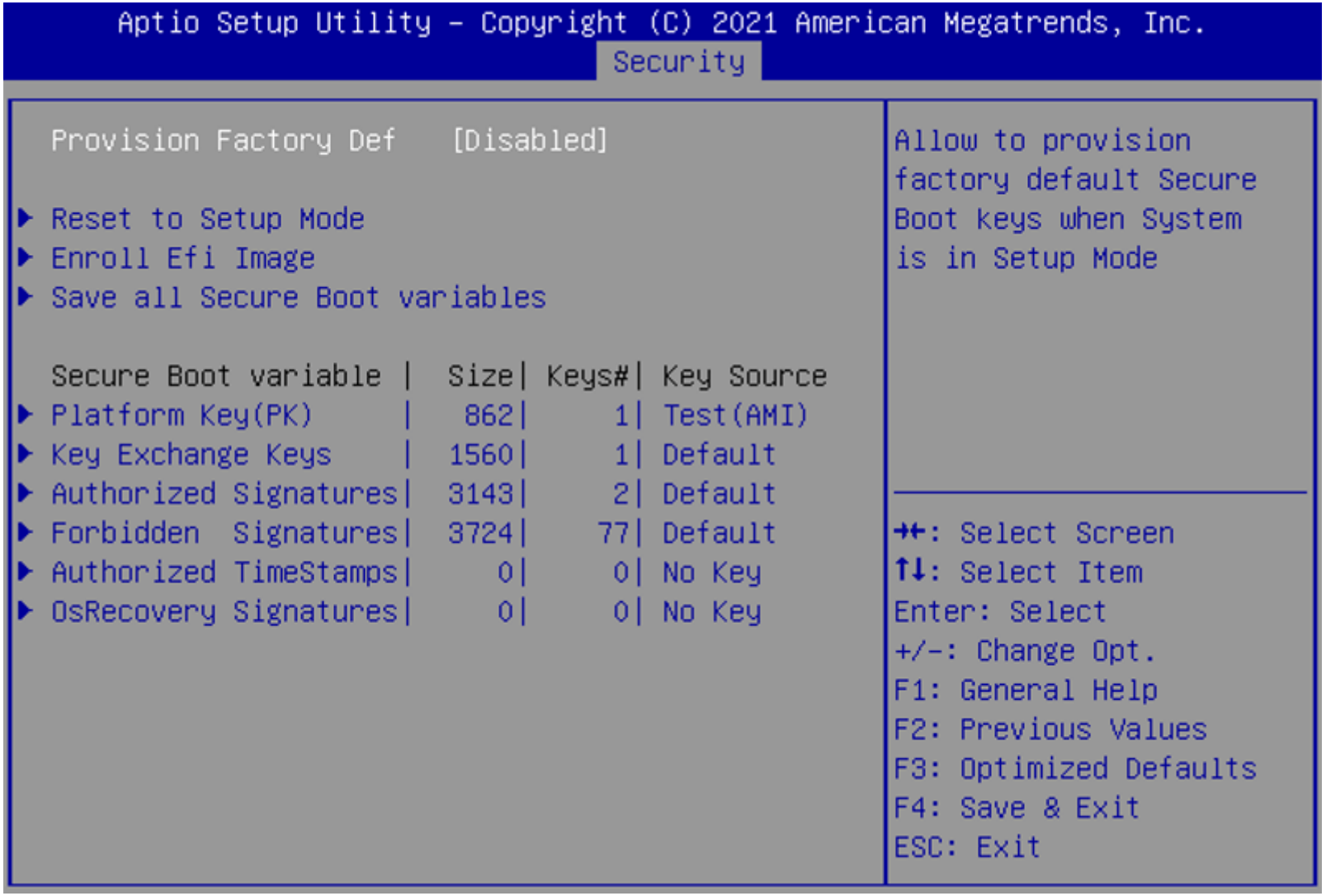


Figure 30 Security Key Management

Feature	Description	Options
Provision Factory Def	Allow to provision factory default Secure Boot Keys when System is in Setup Mode.	Enabled, ★Disabled
Reset to Setup Mode	Force system to setup mode – delete all Secure Boot Key databases	
Enroll Efi Image	Allow the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Authorized Signature Database (db)	
Save all Secure Boot variables	Save NVRAM content of Secure Boot policy variables to the files (EFI_SIGNATURE_LIST data format) in root folder on a target file system device.	
Platform Key(PK)	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Save to file, Set New, Erase
Key Exchange Keys	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Save to File, Set New, Append, Erase
Authorized Signatures	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Save to File, Set New, Append, Erase
Forbidden Signatures	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Save to File, Set New, Append, Erase
Authorized TimeStamps	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Set New, Append

OsRecovery Signatures	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded)	Set New, Append

6.6 Boot

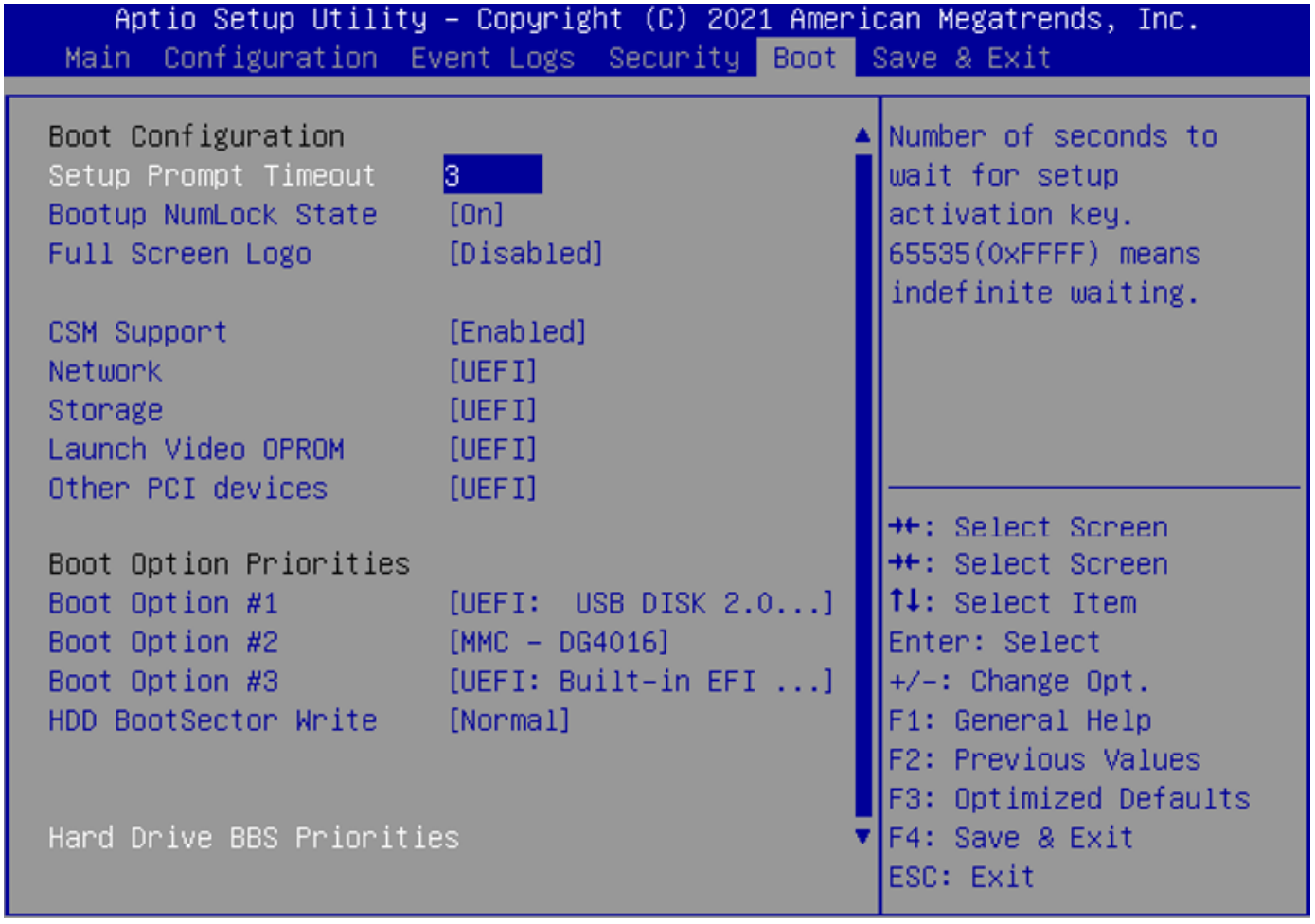


Figure 31 BIOS BOOT

Feature	Description	Options
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★3
Bootup NumLock State	Select the keyboard NumLock state	★On, Off
Full Screen LOGO	Enables or disables Quiet Boot option and Full screen Logo.	★Disabled, Enabled
CSM Support	Enable/Disable CSM support	★Enabled, Disabled
Network	Controls the execution of UEFI and Legacy PXE OpROM	★UEFI, Do not launch, Legacy
Storage	Controls the execution of UEFI and Legacy Storage OpROM	★UEFI, Do not launch, Legacy
Launch Video OPROM	Controls the execution of UEFI and Legacy Video OpROM	★UEFI, Do not launch, Legacy
Other PCI devices	Determines OpROM execution policy for devices other than Network, Storage, or Video.	★UEFI, Do not launch, Legacy
Boot Option #	Sets the system boot order	MMC-DG4016 UEFI: Built-in EFI Shell Disabled
HDD BootSector Write	Enables or disables writes to Hard Disk Sector 0	★Normal, Write Protect
Hard Drive BBS Priorities	Set the order of the legacy devices in this group	

Hard Drive BBS Priorities

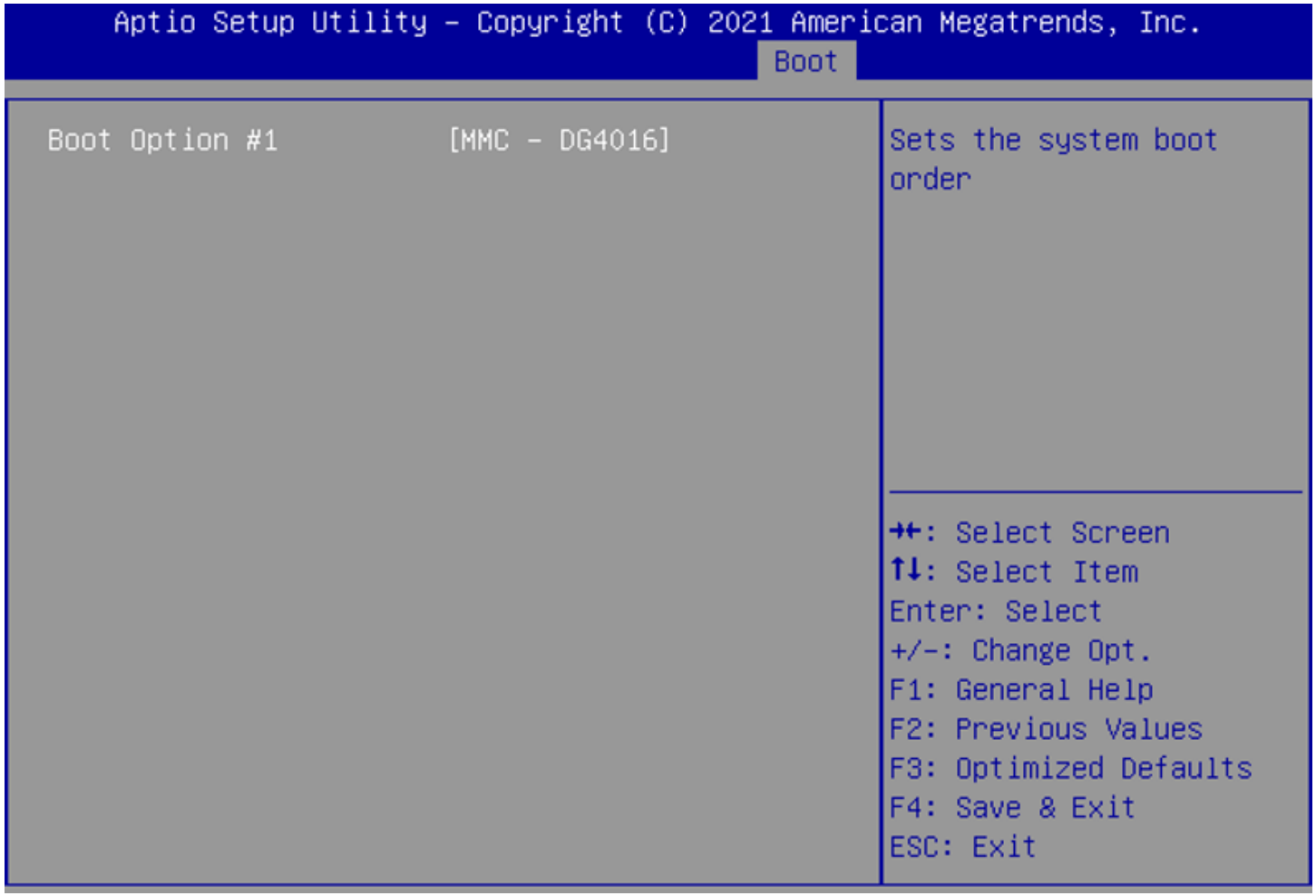


Figure 32 BIOS Boot Option

Feature	Description	Options
Boot Option #	Sets the system boot order	★MMC – DG4016, Disable

6.6 Save & Exit

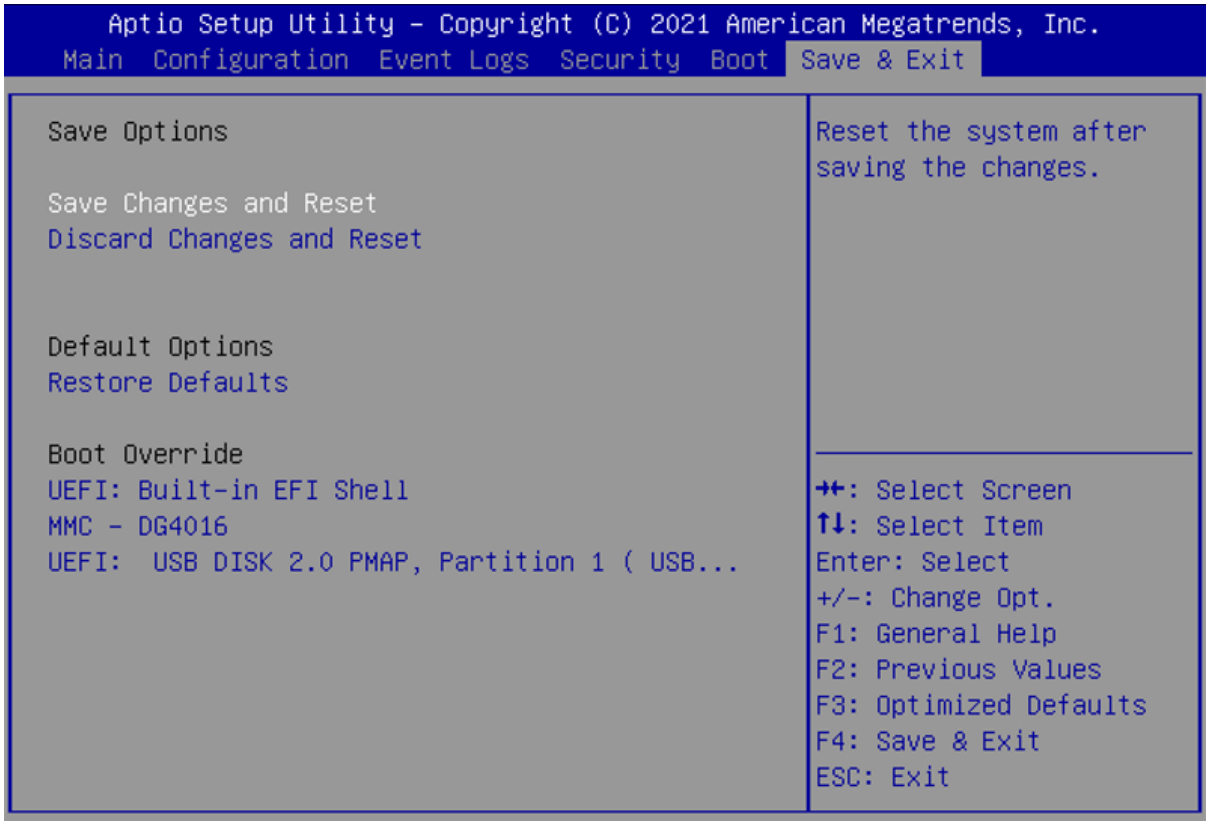


Figure 33 BIOS SAVE & EXIT

Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Reset system setup without saving any changes.	
Restore Defaults	Restore/Load Default values for all the setup options.	
UEFI: Built-in EFI Shell	Reset the system after saving the changes. (Boot option filter: UEFI only)	

7 System Resources

Device	I/O Address	Note
ITE series Embedded Controller	0x6E / 0x6F	EC Address
	0x62 / 0x66	EC ACPI CMD Port
	0x200 / 0x201	EC BRAM Port for I2C function
	0xE300~0xE3FF	EC LPC IO Space
	0x3F8~0x3FF	EC UART1
	0x3E8~0x3EF	EC UART2

Interface	8bit	7bit	Note
SMBus	0x30	0x18	DDR Temperature: Channel A DIMM0, J2 Slot
	0x34	0x1A	DDR Temperature: Channel B DIMM1, J4 Slot
	0x36	0x1B	DDR Temperature: Channel B DIMM2, J3 Slot
	0x6C	0x36	DDR4 Set SPD Page 0
	0x88	0x44	SMBus ARP
	0x98	0x4C	PECI
	0xA0	0x50	Memory SPD: Channel A DIMM0, J2 Slot
	0xA4	0x52	Memory SPD: Channel B DIMM1, J4 Slot
	0xA6	0x53	Memory SPD: Channel B DIMM2, J3 Slot

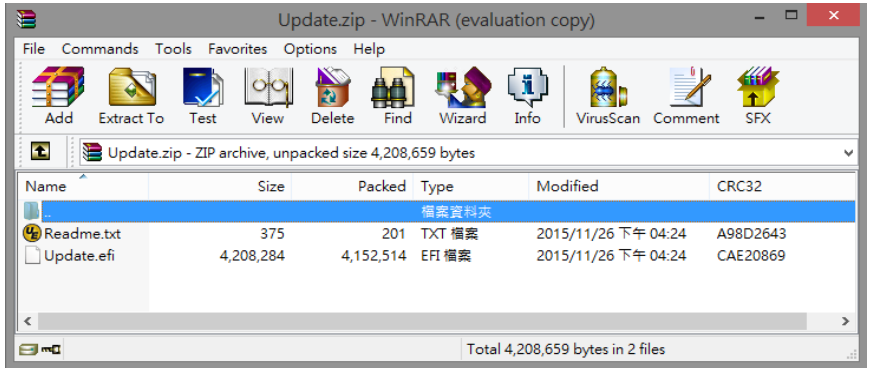
Table 9 System Resources

8 BIOS/EC Update

BIOS/EC UEFI Update SOP process

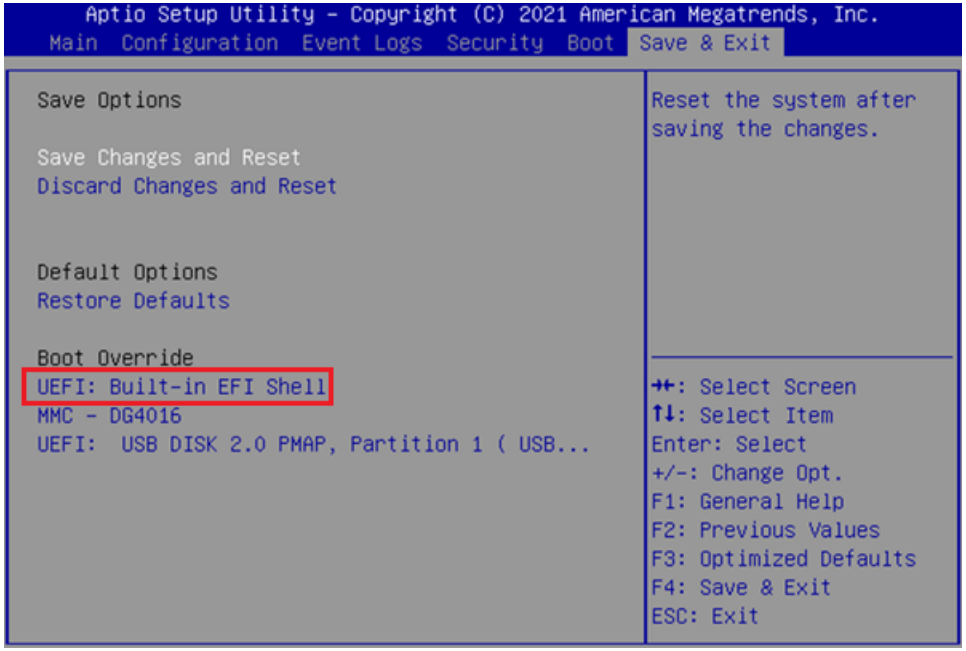
Step 1. Prepare a USB DOK. (Must be FAT or FAT32 format).

Step 2. Unzip update file to the USB DOK.

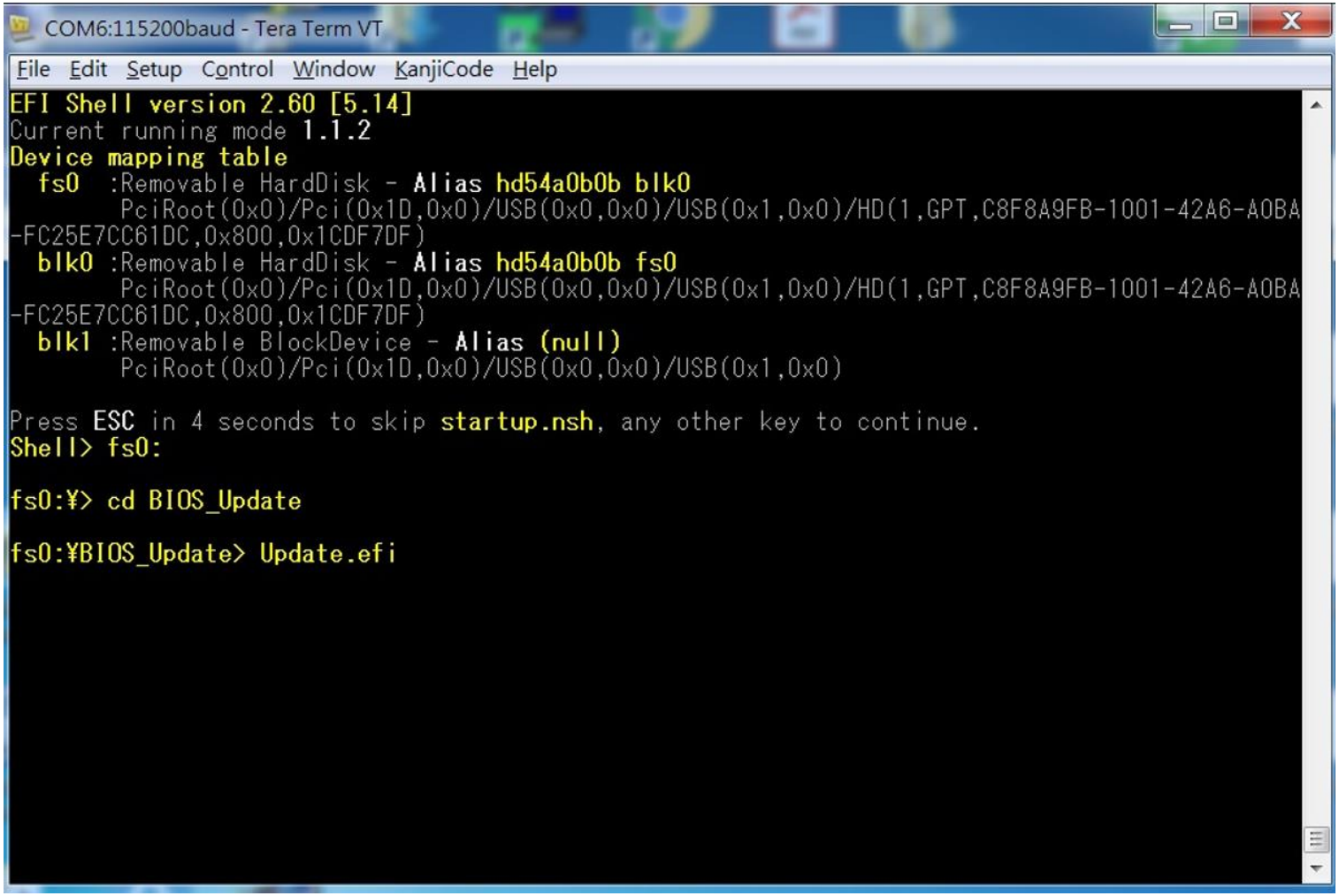


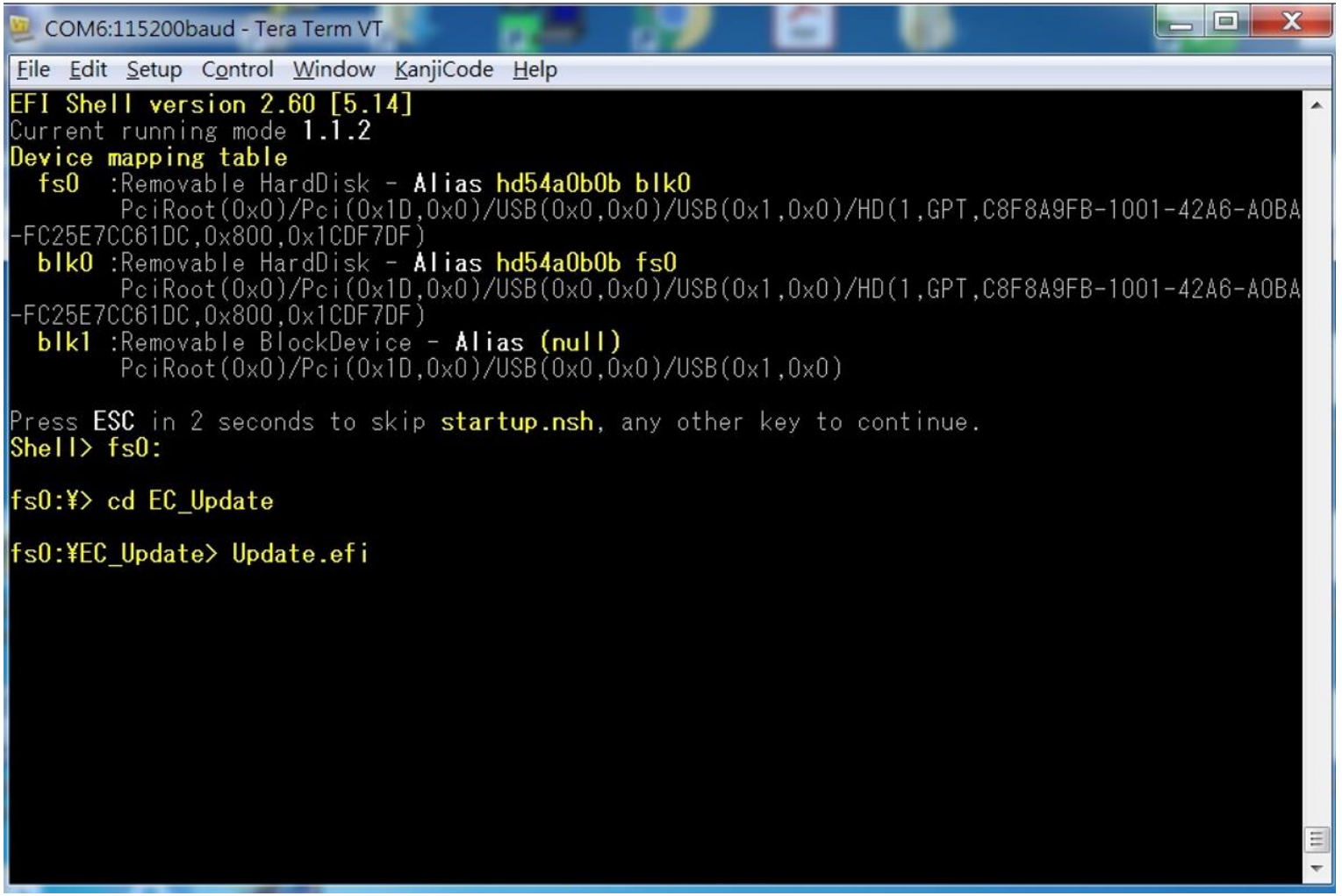
Step 3. Plug the USB DOK into the target system and then boot system.

Step 4. Press Del to access BIOS Save & Exit page to select BIOS UEFI: Built-in EFI Shell



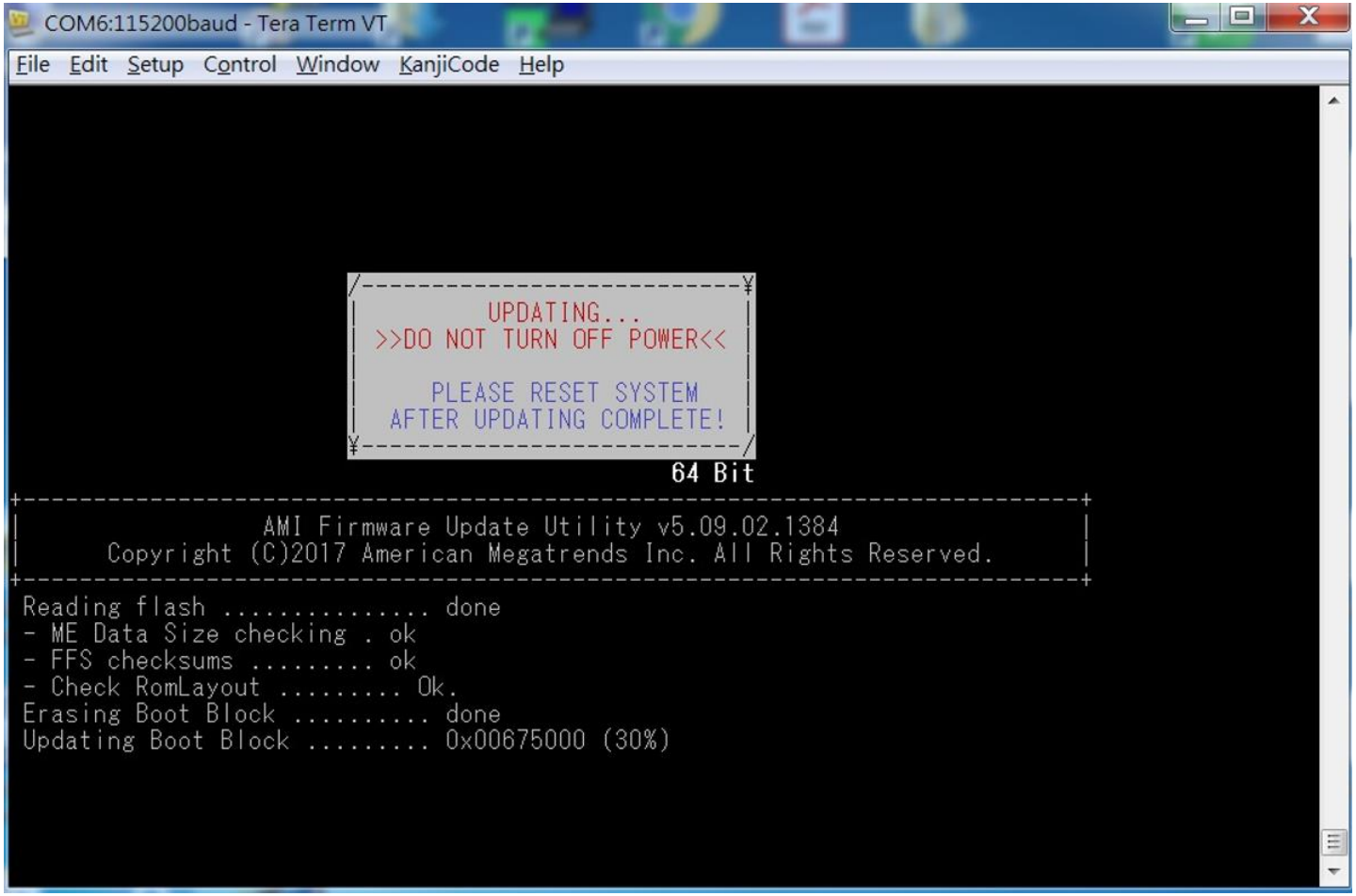
Step 5. Under the UEFI shell, direct to your USB DOK, below is an example uses fs0. Then direct to the folder with updated file and type command : "Update.efi" and press enter.

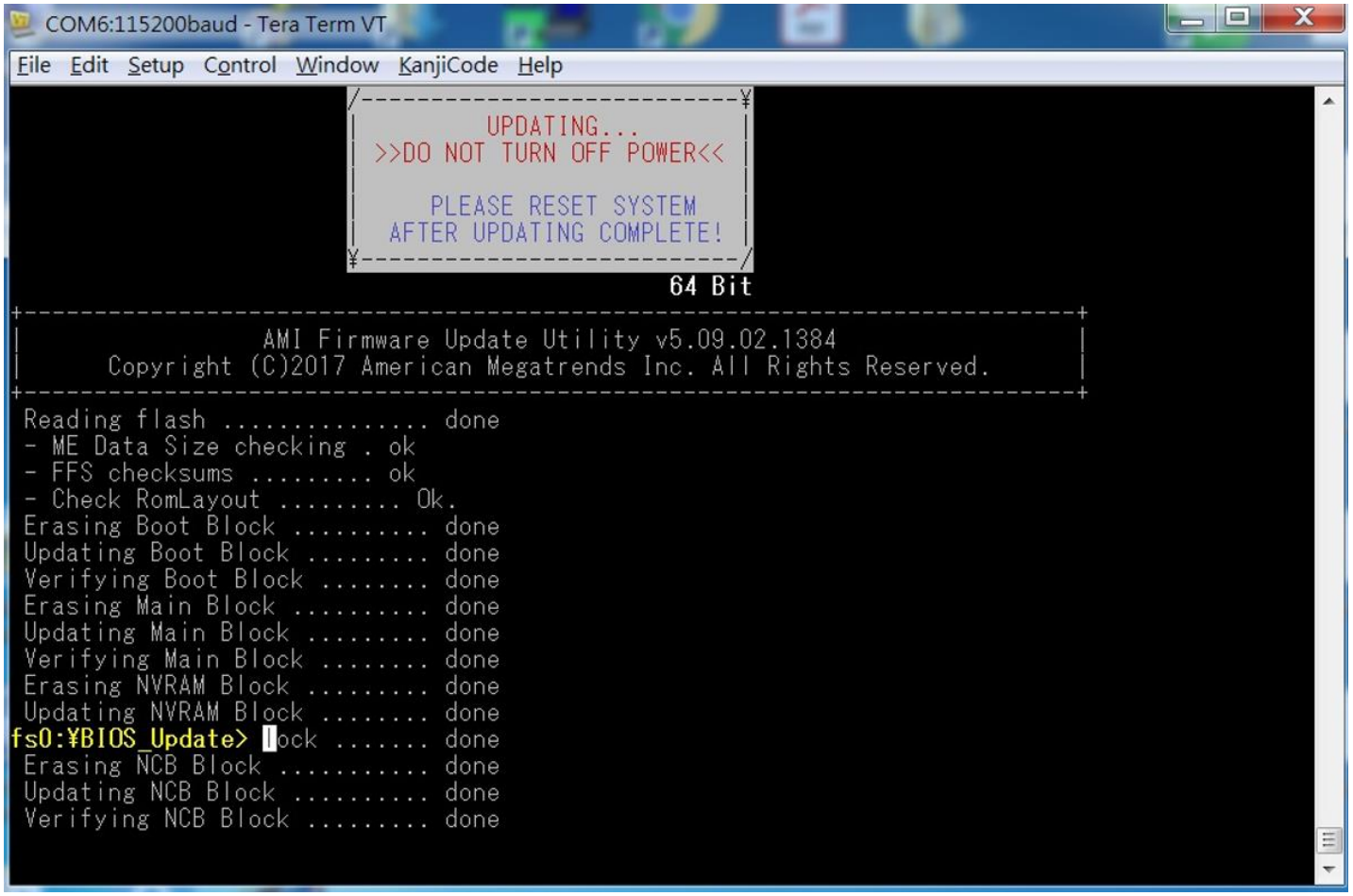



COM6:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help
EFI Shell version 2.60 [5.14]
Current running mode 1.1.2
Device mapping table
fs0 :Removable HardDisk - Alias hd54a0b0b blk0
PciRoot(0x0)/Pci(0x1D,0x0)/USB(0x0,0x0)/USB(0x1,0x0)/HD(1,GPT,C8F8A9FB-1001-42A6-A0BA
-FC25E7CC61DC,0x800,0x1CDF7DF)
blk0 :Removable HardDisk - Alias hd54a0b0b fs0
PciRoot(0x0)/Pci(0x1D,0x0)/USB(0x0,0x0)/USB(0x1,0x0)/HD(1,GPT,C8F8A9FB-1001-42A6-A0BA
-FC25E7CC61DC,0x800,0x1CDF7DF)
blk1 :Removable BlockDevice - Alias (null)
PciRoot(0x0)/Pci(0x1D,0x0)/USB(0x0,0x0)/USB(0x1,0x0)
Press ESC in 2 seconds to skip startup.nsh, any other key to continue.
Shell> fs0:
fs0:¥> cd EC_Update
fs0:¥EC_Update> Update.efi

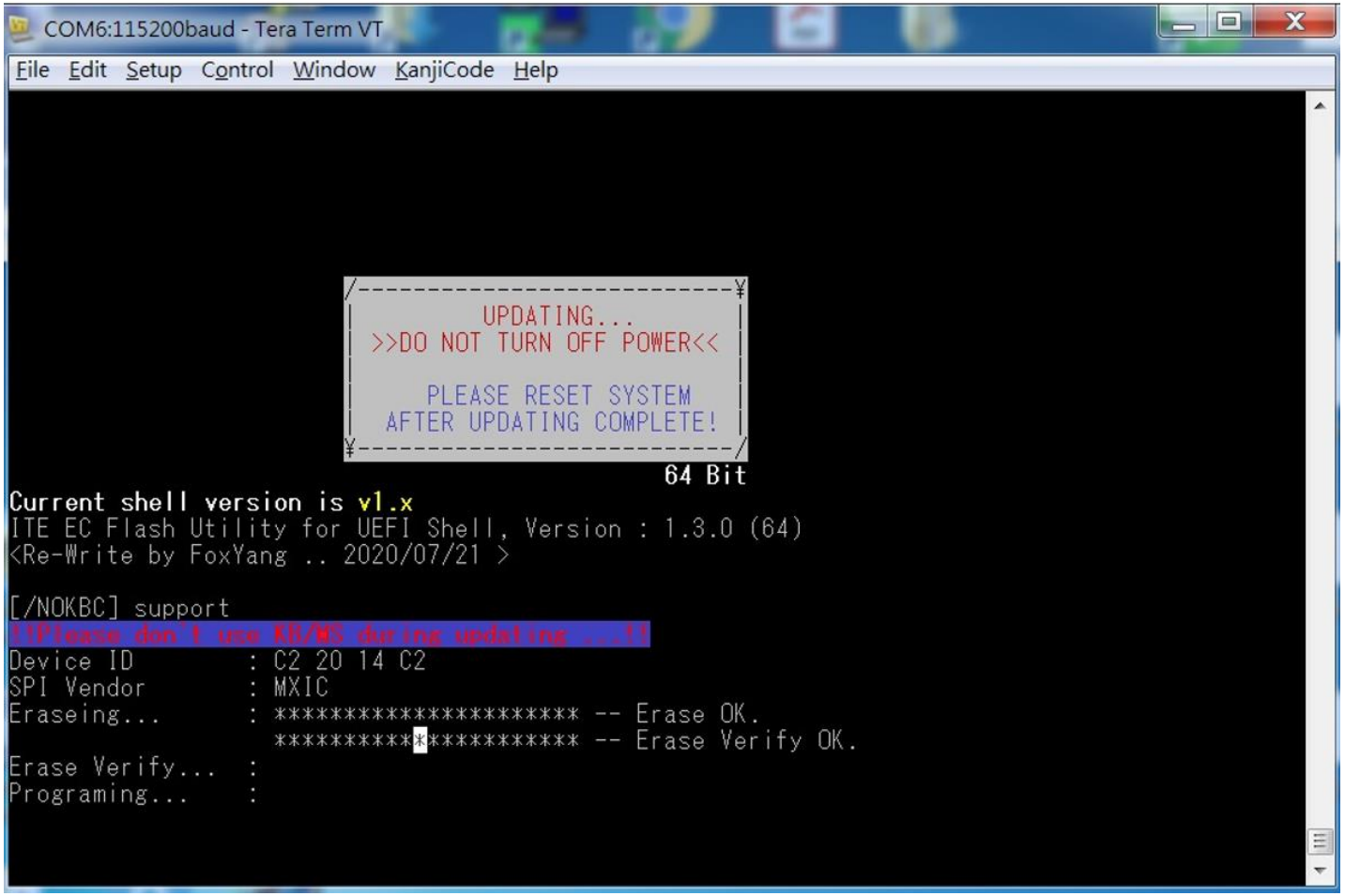
Step 6. The updating process will start and you can see the updating progress. Once finished, please power off and restart the system.

BIOS update




COM6:115200baud - Tera Term VT
File Edit Setup Control Window KanjiCode Help
UPDATING...
>>DO NOT TURN OFF POWER<<
PLEASE RESET SYSTEM
AFTER UPDATING COMPLETE!
64 Bit
AMI Firmware Update Utility v5.09.02.1384
Copyright (C)2017 American Megatrends Inc. All Rights Reserved.
Reading flash ..... done
- ME Data Size checking . ok
- FFS checksums ..... ok
- Check RomLayout ..... Ok.
Erasing Boot Block ..... done
Updating Boot Block ..... done
Verifying Boot Block ..... done
Erasing Main Block ..... done
Updating Main Block ..... done
Verifying Main Block ..... done
Erasing NVRAM Block ..... done
Updating NVRAM Block ..... done
fs0:¥BIOS_Update> lock ..... done
Erasing NCB Block ..... done
Updating NCB Block ..... done
Verifying NCB Block ..... done

EC update



<End of BIOS/EC UEFI update process>

9 PORTWELL Software Tool

PORTWELL Evaluation Tool (PET)

The PORTWELL Evaluation Tool (PET) is an API which PORTWELL's customers can access the GPIO, I2C, SMBus, etc under Windows and Linux OS. For more information please contact PORTWELL.

PORTWELL BIOS web Tool (PBT)

The PORTWELL BIOS web Tool (PBT) is a brand new on-line utility innovated by PORTWELL. PBT now is available for PORTWELL's premiere customers who are able to add customized BIOS logo and change BIOS default settings on American Megatrends (AMI) BIOS. Please contact PORTWELL for more information.

PORTWELL EC Auto Test Tool (PECAT)

The PORTWELL EC Auto Test Tool (PECAT) is a brand new utility innovated by PORTWELL. PECAT now is available for PORTWELL's premiere customers, who are able to Test Embedded Controller Function in UEFI Mode. Please contact PORTWELL for more information.

10 Packaging Information

Package	Appearance	Size
Anti-Static bubble bag		180x130mm
White Paper Box		210x150x40mm
Shipping Box (10 pcs White paper box)		595x300x185mm

Table 10 PCOM-B701GT Packaging

11 Industry Specifications

The list below provides links to industry specifications that apply to PORTWELL modules.

Low Pin Count Interface Specification, Revision 1.0 (LPC) http://www.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0 http://www.usb.org/home
PCI Specification, Revision 2.3 https://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0 http://www.serialata.org/
PICMG® COM Express Module™ Base Specification http://www.picmg.org/
PCI Express Base Specification, Revision 2.0 https://www.pcisig.com/specifications