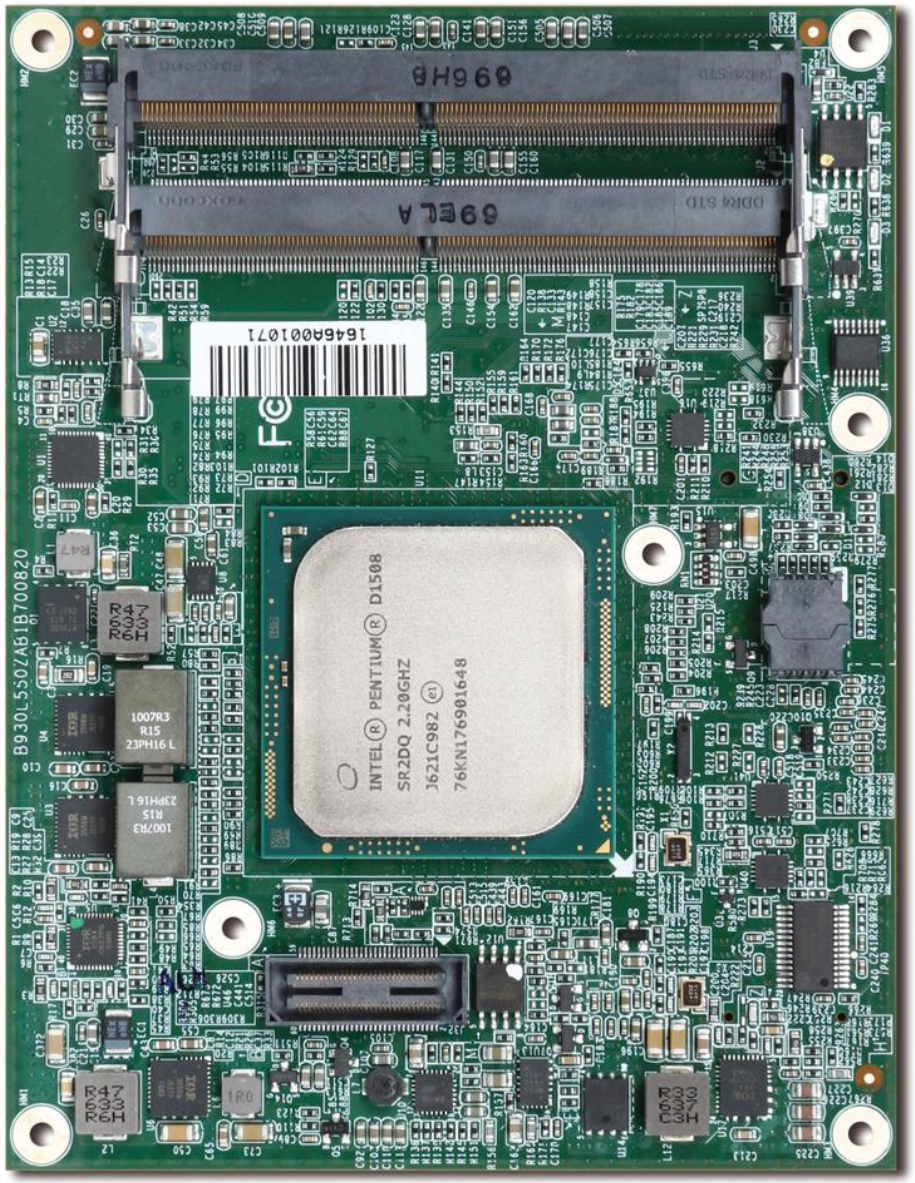

COM Express™ PCOM-B700G User's Guide R1.2

Revision History

Rev.	Note	Date
R1.0	Preliminary	March.2018
R1.1	Update mechanical drawing	June 2018
R1.2	Update BIOS Screen	June 2018

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1 Introduction

The Portwell PCOM-B700G, a Type 7 COM Express basic (125mm x 95mm) module is designed with Intel® Xeon® processor D-1500 product family. Specifically, the COM Express 3.0 specification's Type 7 pinout, when compared to the Type 6 pinout, trades all the graphics interfaces for up to four 10GbE ports and a total of 32 PCIe lanes, ideal for applications in micro server and the like, requiring low power consumption while supporting high computing performance and communication throughput. Portwell's PCOM-B700G features two 10GbE KR, one GbE, DDR4 ECC/non-ECC memory support, and Gen3 PCIe supporting high speed I/O card. In addition, Portwell's PCOM-B700G Type 7 COM Express module also supports a wide -40°C~85°C industrial temperature range (selected SKUs).

The new COM Express® Type 7 standard is a new specification with backward compatibility to the existing Type 6 pinout. While the focus of Type 6 is on display-oriented applications with support for audio and video interfaces, the Type 7 pinout definition is designed for applications that do not require graphics support. Specifically, the COM Express® 3.0 specification's Type 7 pinout, when compared to the Type 6 pinout, trades all the graphics interfaces for up to four 10GbE ports, and a total of 32 PCIe lanes. This makes it ideal for applications in micro server and the like that require low power consumption while supporting high computing performance and communication throughput.

This latest PCOM-B700G COM Express® module extends Portwell’s product family of server-grade COM Express® based platforms. Back in 2015, Portwell launched PCOM-B634VG, a Type 6 COM Express® module, which was the first COM Express® module featuring Intel® Xeon® processor D-1500 series, 10GbE support, and integrated VGA. Based on PCOM-B634VG’s success, Portwell’s new PCOM-B700G Type 7 COM Express® module extends the design from PCOM-B634VG, removes the VGA interface and adds NC-SI (Network Controller Sideband Interface) as well as more PCIe lanes to meet the COM Express® Type 7 standard. The two 10GbE-KR ports on PCOM-B700G allow customers to flexibly design their physical interface on a carrier board in several modes, KR for backplane connectivity, copper (RJ45), or fiber (SFP+). And the NC-SI signals provide a way of connecting BMC (baseboard management controller) on the carrier board to achieve remote control and management.

2 Block Diagram

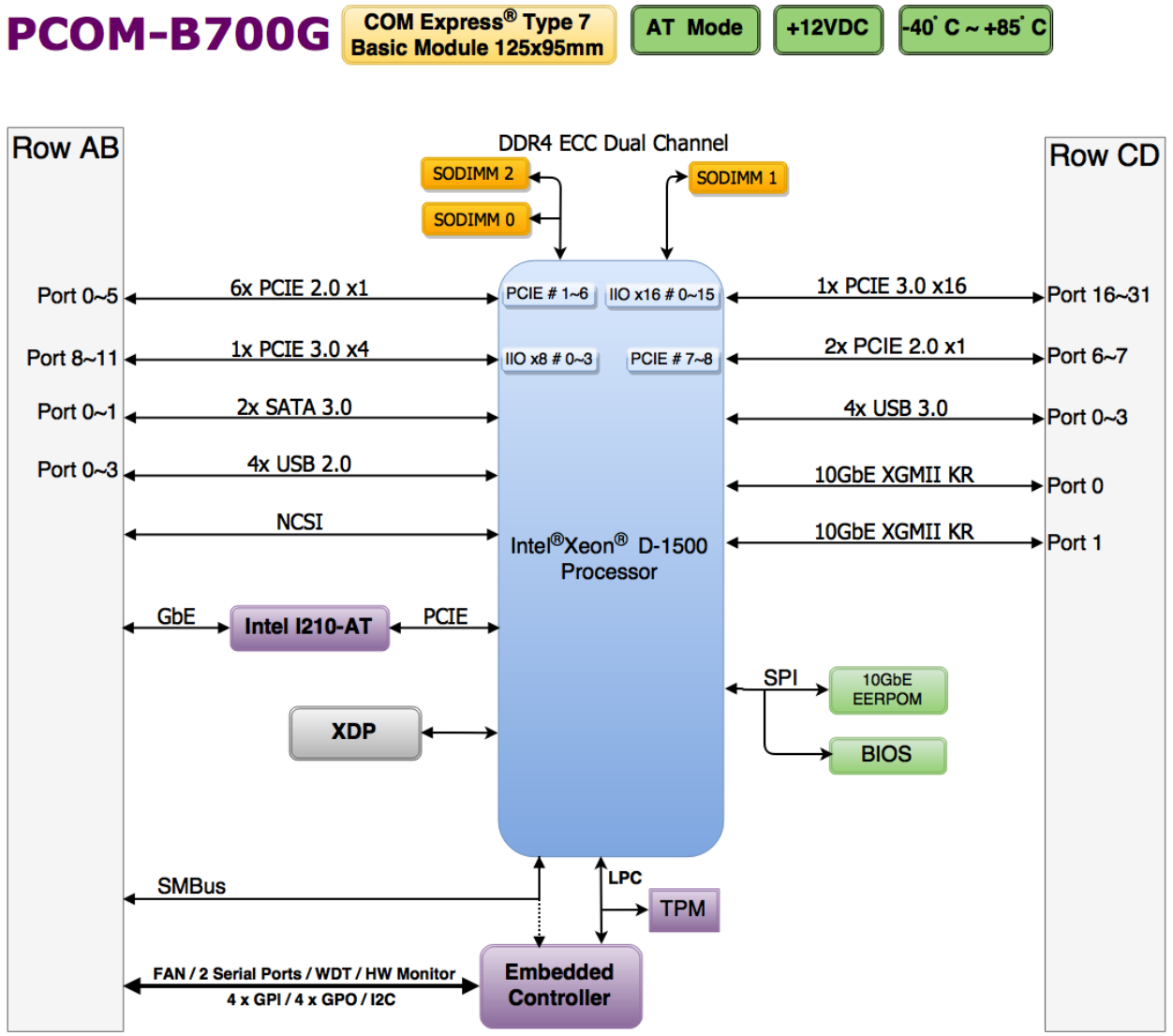


Figure 1 Block Diagram

3 Specifications

Table 1 PCOM-B700GVG SPEC

*Note1

The PEG available lanes configurations are shown below:

1x16 (Default)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
2x8	0	1	2	3	4	5	6	7								
									0	1	2	3	4	5	6	7
4x4	0	1	2	3					0	1	2	3				
					0	1	2	3					0	1	2	3
1x8 + 2x4	0	1	2	3	4	5	6	7	0	1	2	3				
													0	1	2	3
2x4 + 1x8	0	1	2	3					0	1	2	3	4	5	6	7
					0	1	2	3								

3.1 PCOM-B700G Processor list

PCOM-B700G series	PCOM-B700G D-1507	PCOM-B700G D1508	PCOM-B700G D1517	PCOM-B700G D1519	PCOM-B700G D1527	PCOM-B700G D1537	PCOM-B700G D1539	PCOM-B700G D1548	PCOM-B700G D1557	PCOM-B700G D1577
Ordering P/N	TBD	TBD	TBD	TBD	AB1-3F51Z	TBD	AB1-3F52Z	AB1-3F53Z	TBD	TBD
Processor	Intel® Pentium® D1507	Intel® Pentium® D1508	Intel® Pentium® D1517	Intel® Pentium® D1519	Intel® Xeon® D-1527	Intel® Xeon® D-1537	Intel® Xeon® D-1539	Intel® Xeon® D-1548	Intel® Xeon® D-1557	Intel® Xeon® D-1577
# of Cores	2	2	4	4	4	8	8	8	12	16
# of Threads	2	4	8	8	8	16	16	16	24	32
Processor Base Frequency	1.20 GHz	2.20 GHz	1.60 GHz	1.50 GHz	2.20 GHz	1.70 GHz	1.60 GHz	2.00 GHz	1.50 GHz	1.30 GHz
Max Turbo Frequency	1.20 GHz	2.60 GHz	2.20 GHz	2.10 GHz	2.70 GHz	2.30 GHz	2.20 GHz	2.60 GHz	2.10 GHz	2.10 GHz
Cache	3 MB	3 MB	6 MB	6 MB	6 MB	12 MB	12 MB	12 MB	18 MB	24 MB
TDP	20 W	25 W	25 W	25 W	35 W	35 W	35 W	45 W	45 W	45 W
ECC Memory Supported	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
USB Revision	2.0/3.0	2.0/3.0	2.0/3.0	2.0/3.0	2.0/3.0	2.0/3.0	2.0/3.0	2.0/3.0	2.0/3.0	2.0/3.0
Networking Specifications										
SFI Interface	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
KR Interface	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
KR4 Interface	No	No	No	No	No	No	No	No	No	No
KX Interface	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
KX4 Interface	Yes	Yes	Yes	Yes	No	No	No	No	No	No
100Base-T	No	No	No	No	No	No	No	No	No	No

1000Base-T	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
10GBase-T	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Operating Temperature Range	-	-	-	-40°C to 85°C	-	-	-40°C to 85°C	-	-	-
Advanced Technologies										
Intel® Turbo Boost Technology	No	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Intel® Hyper-Threading Technology	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Virtualization Technology (VT-x)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Intel® Virtualization Technology for Directed I/O (VT-d)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Intel® VT-x with Extended Page Tables (EPT)	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Intel® TSX-NI	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Intel® 64	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Instruction Set	64-bit	64-bit	64-bit	64-bit	64-bit	64-bit	64-bit	64-bit	64-bit	64-bit
Instruction Set Extensions	AVX 2.0	AVX 2.0	AVX 2.0	AVX 2.0	AVX 2.0	AVX 2.0	AVX 2.0	AVX 2.0	AVX 2.0	AVX 2.0

Idle States	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Enhanced Intel SpeedStep® Technology	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Thermal Monitoring Technologies	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Intel® AES New Instructions	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Secure Key	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Trusted Execution Technology	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Execute Disable Bit	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
OS Guard	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 2 PCOM-B700G Processor list

3.2 Supported Operating Systems

The PCOM-B700GVG supports the following operating systems.

Vendor	Operating System	Supported
Microsoft	Windows 7 (32/64bit)	YES
	Windows 8 (32/64bit)	YES
	Windows 8.1 (32/64bit)	YES
	Windows 10 (32/64bit)	YES
	Microsoft Windows 2008 R2 SP1	YES
	Microsoft Windows 2012	YES
	Microsoft Windows 2012 R2	YES
Linux	Fedora 22 (kernel 4.0.4-301)	YES
	Ubuntu 15.04 (kernel 3.11.6.4)	YES

Table 3 Supported OS list

3.3 Windows OS driver

Please download the drivers from Portwell download center website http://www.portwell.tw/support/download_center.php

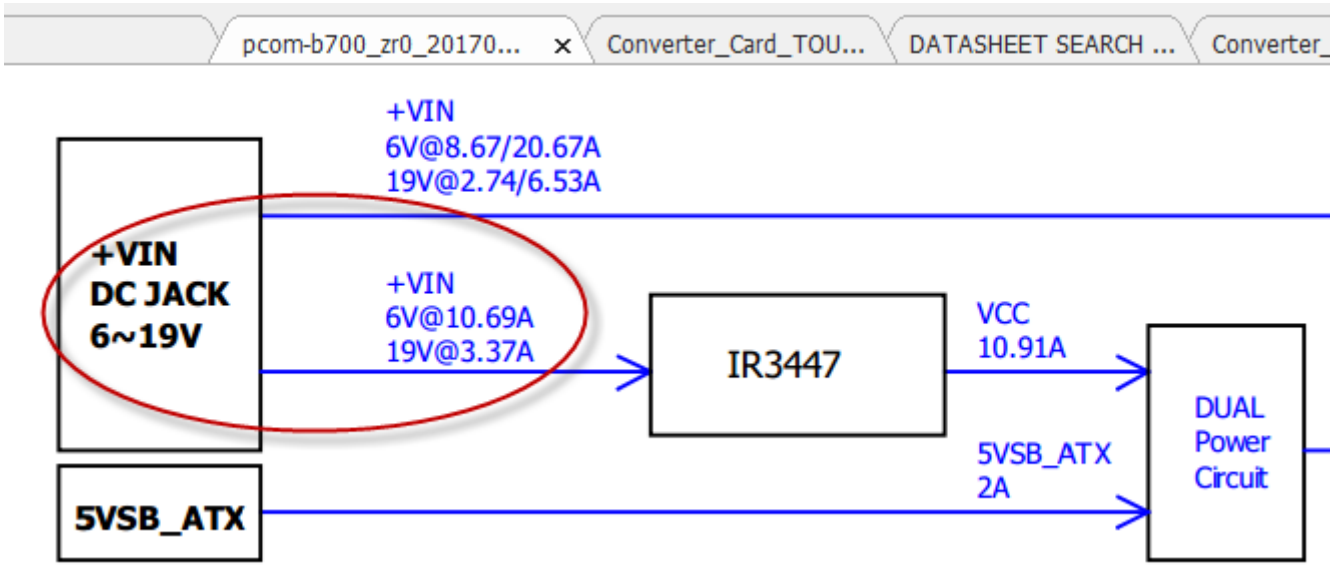
Drivers file name	Supported Operating Systems
10GLAN_Win7_64	Windows Server 2008 R2 (64bit) Microsoft Windows 7 (64bit)
Chipset_Win7_8_81_32_64	Microsoft Windows 7 (32/64bit) Microsoft Windows 8 (32/64bit) Microsoft Windows 8.1 (32/64bit)
Graphics_Win7_32_64	Microsoft Windows 7 (32/64bit)
Graphics_Win8_81_32_64	Microsoft Windows 8 / 8.1 (32/64bit)
Graphic_Windows10_Driver	Microsoft Windows 10 (32/64bit)
I210LAN_Win7_8_81_32_64	Microsoft Windows 7 (32/64bit) Microsoft Windows 8 / 8.1 (32/64bit) Windows Server 2008 R2 Microsoft Windows 2012 Microsoft Windows 2012 R2
XHCI_Win7_32_64	Microsoft Windows 7 (32/64bit) Windows Server 2008 (32/64bit)
10GLAN_Win8_81_64	Microsoft Windows 8 / 8.1 (64bit) Microsoft Windows 2012 (64bit) Microsoft Windows 2012 R2 (64bit)

Table 4 Windows OS driver list

3.4 Electrical Characteristics

Input voltage	+12VDC (Nominal) +6VDC ~ +19VDC (Wide range)
RTC Battery	?
Power on mode	AT Mode

Table 5 Electrical characteristics



PCOM-B700GVG Power sequence

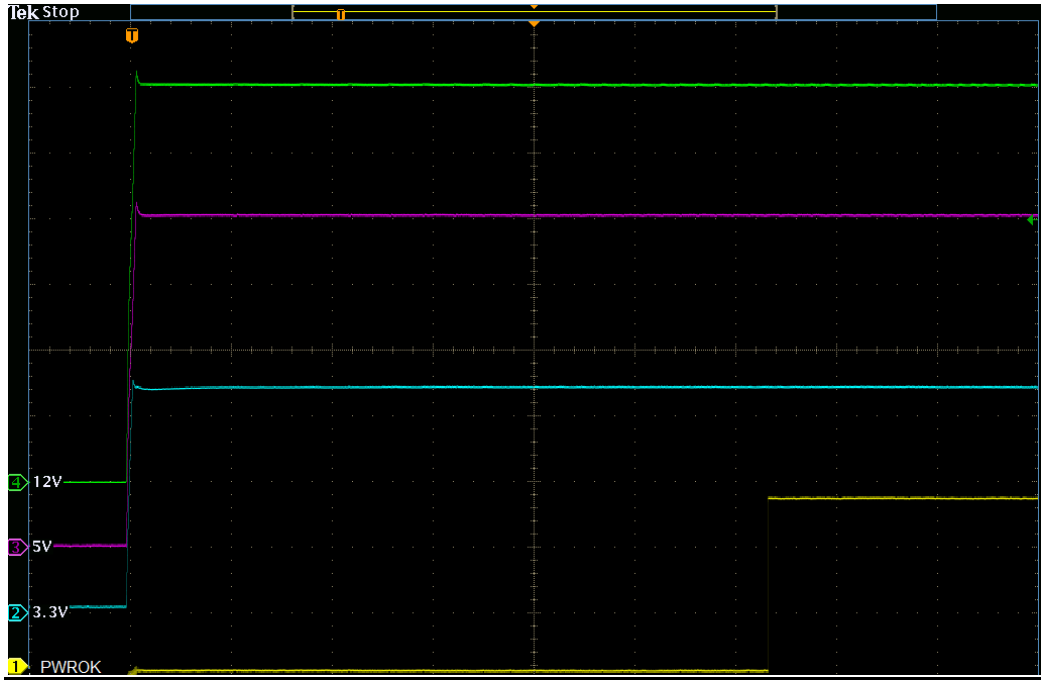


Figure 2 Power on sequence

3.5 Mechanical Dimensions

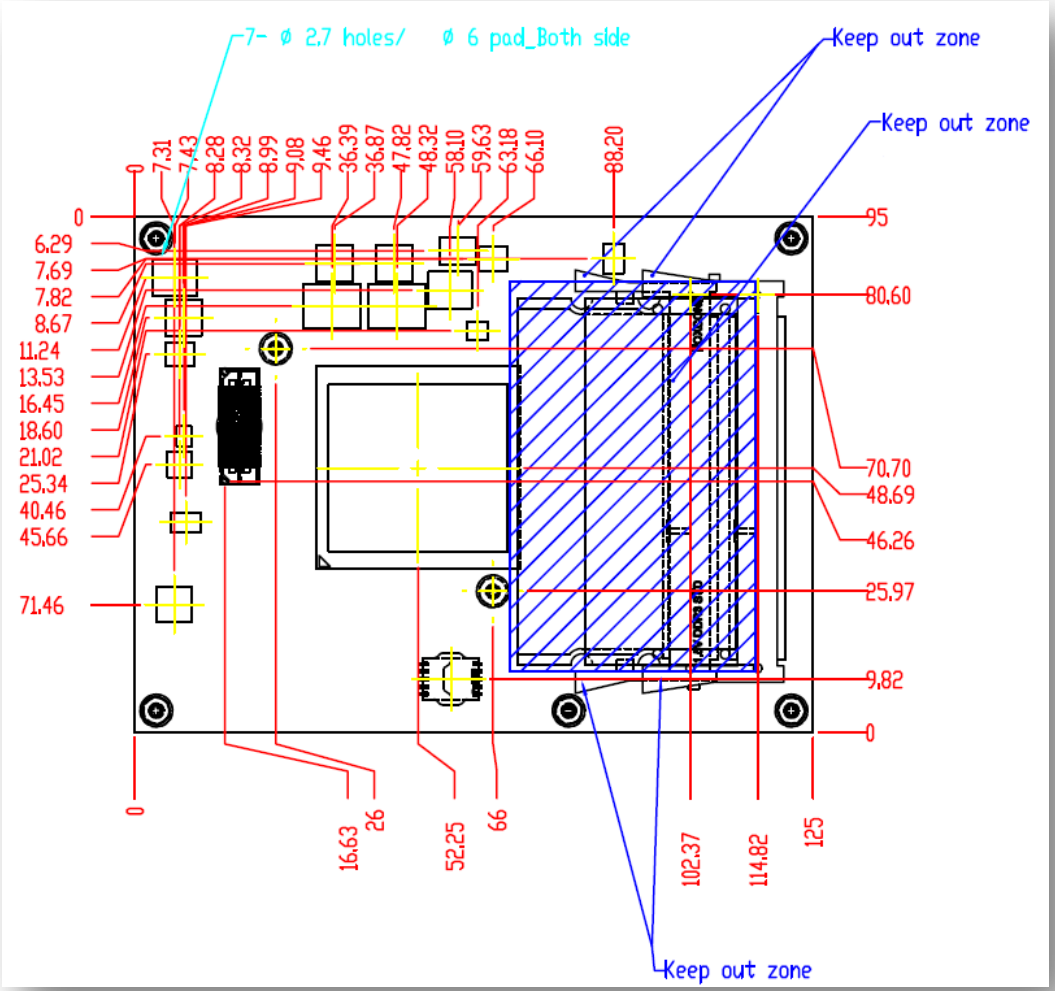


Figure 3 Mechanical Dimensions - Top

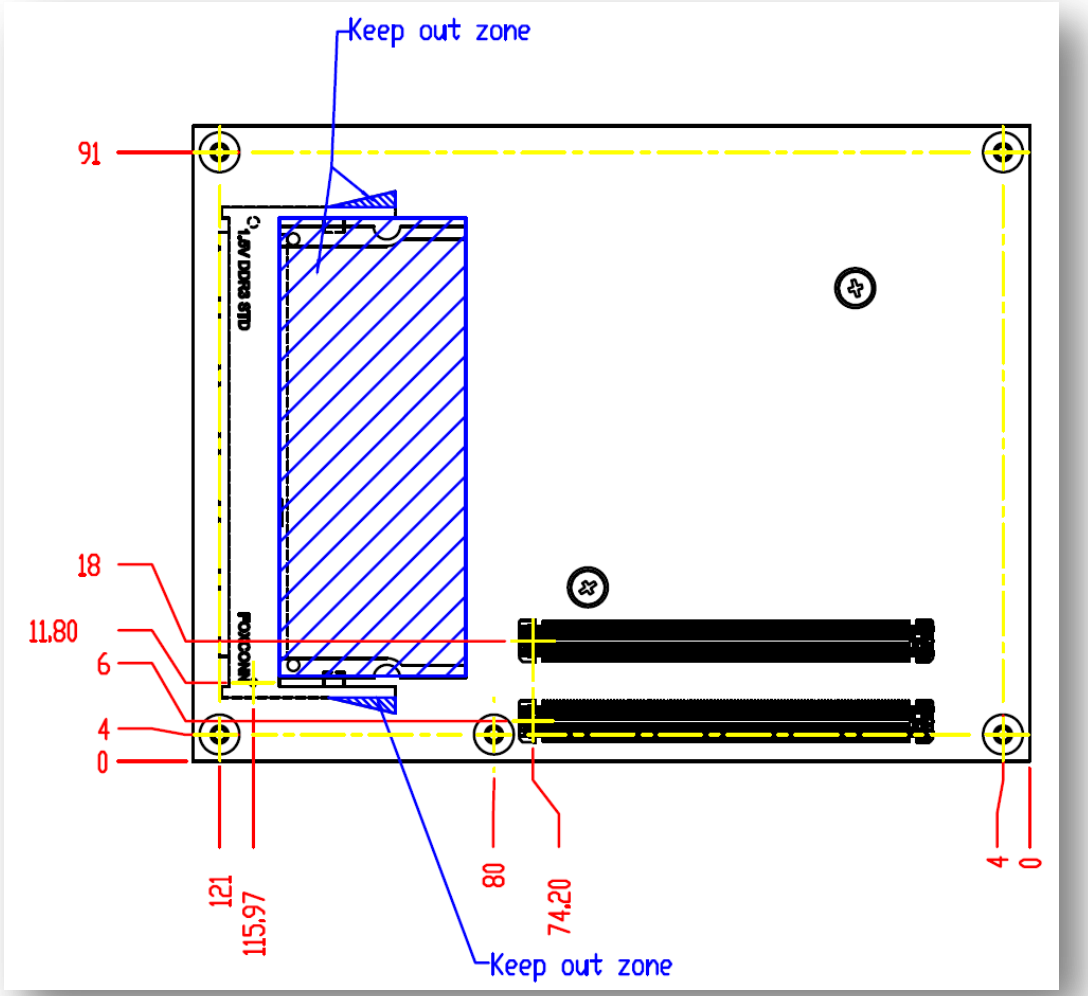


Figure 4 Mechanical Dimensions - Bottom

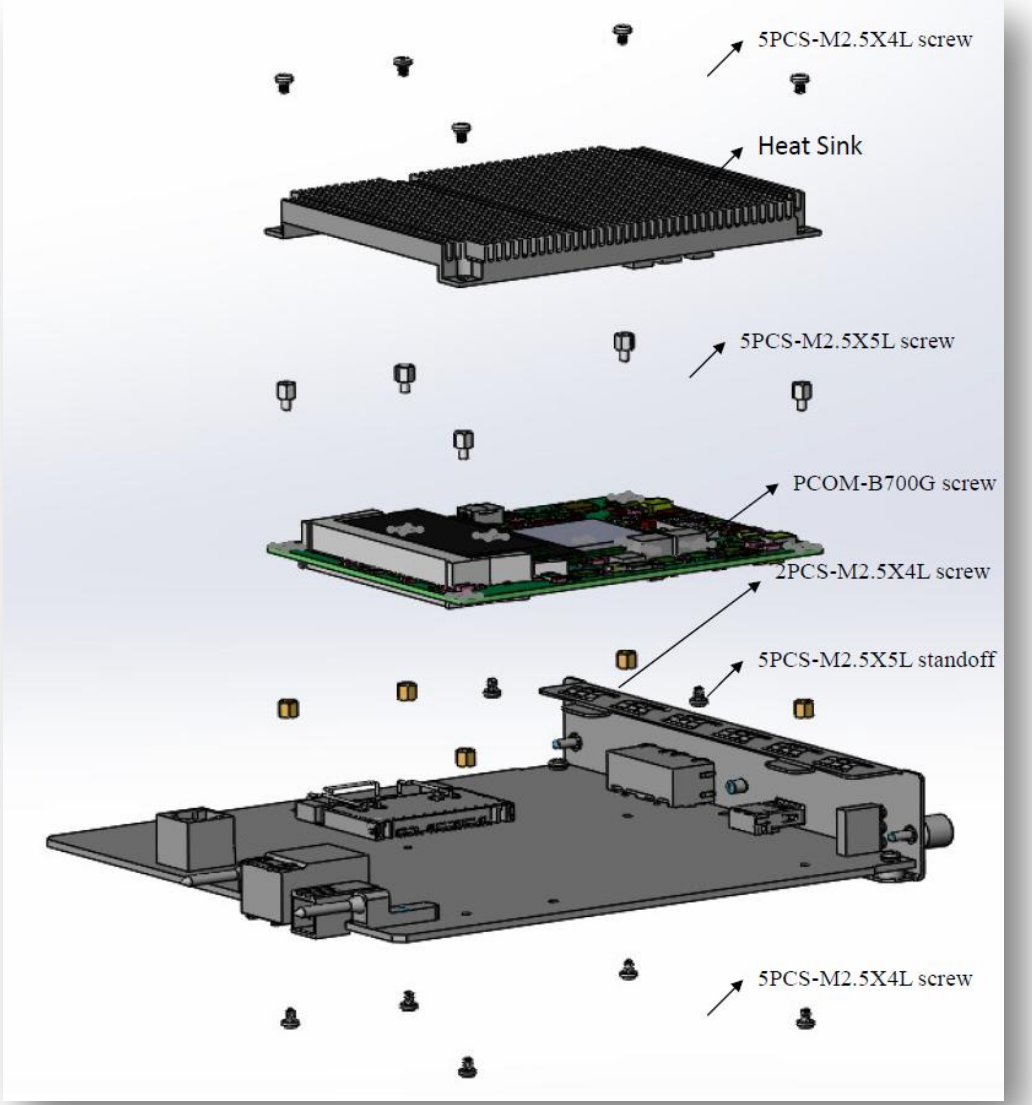


Figure 5 Mechanical Dimensions - Assembly view

Net weight

Module	.0g +/- 2%
Cooler (H/S+FAN)	.0g +/- 2%

Table 6 Weight

3.6 3 SODIMM socket design

PCOM-B700G has designed additional Memory SODIMM socket at the bottom, which supports up to DDR4 48GB capacity. Before inserting the DDR4 SODIMM memory, please refer to below SODIMM arrangement and note that, there are 2 SODIMM socket of channel 0, the CH0 SODIMM1 (the bottom one) works only if CH0 SDDIMM0 (the top one) is inserted.

3.7 Environmental Specifications

Storage Temperature	-20°C ~85°C
Operation Temperature	0°C ~60°C Extended : -40°C ~+85°C (Processor dependent)
Storage Humidity	0%~95%
Operation Humidity	0%~95%

Table 7 Environmental Specifications

3.8 Ordering Guide

PCOM-B700GVG

Product	Ordering P/N	Status
PCOM-B700G-D1507	AB1-3G79	Available
PCOM-B700G-D1508	AB1-3G78	Available
PCOM-B700G-D1517	AB1-3G77	Available

PCOM-B700G-D1519	**AB1-3G80**	**Available (Wide-Temp)**
PCOM-B700G-D1527	AB1-3F51	Available
PCOM-B700G-D1537	AB1-3G81	Available
PCOM-B700G-D1539	**AB1-3F52**	**Available (Wide-Temp)**
PCOM-B700G-D1548	AB1-3F53	Available
PCOM-B700G-D1559	**AB1-3G82**	**Available (Wide-Temp)**
PCOM-B700G-D1577	AB1-3G83	Available

Table 8 Ordering Guide - PCOM-B700G

Accessory

Accessory	Ordering P/N	Status
PCOM-B700G Cooler	B9971570	Available
Evaluation Carrier PCOM-C700	AB1-3F19Z	Available

Table 9 Ordering Guide - Accessory

PCOM-C700 - PCOM-B700GVG Evaluation carrier (EVA Board)

PCOM-C700 is designed for functions verification of PCOM-B700G, which 10GbE function pin compliance with PICMG R3.0.

4 Heat sink / Cooler

Heat sink Dimensions

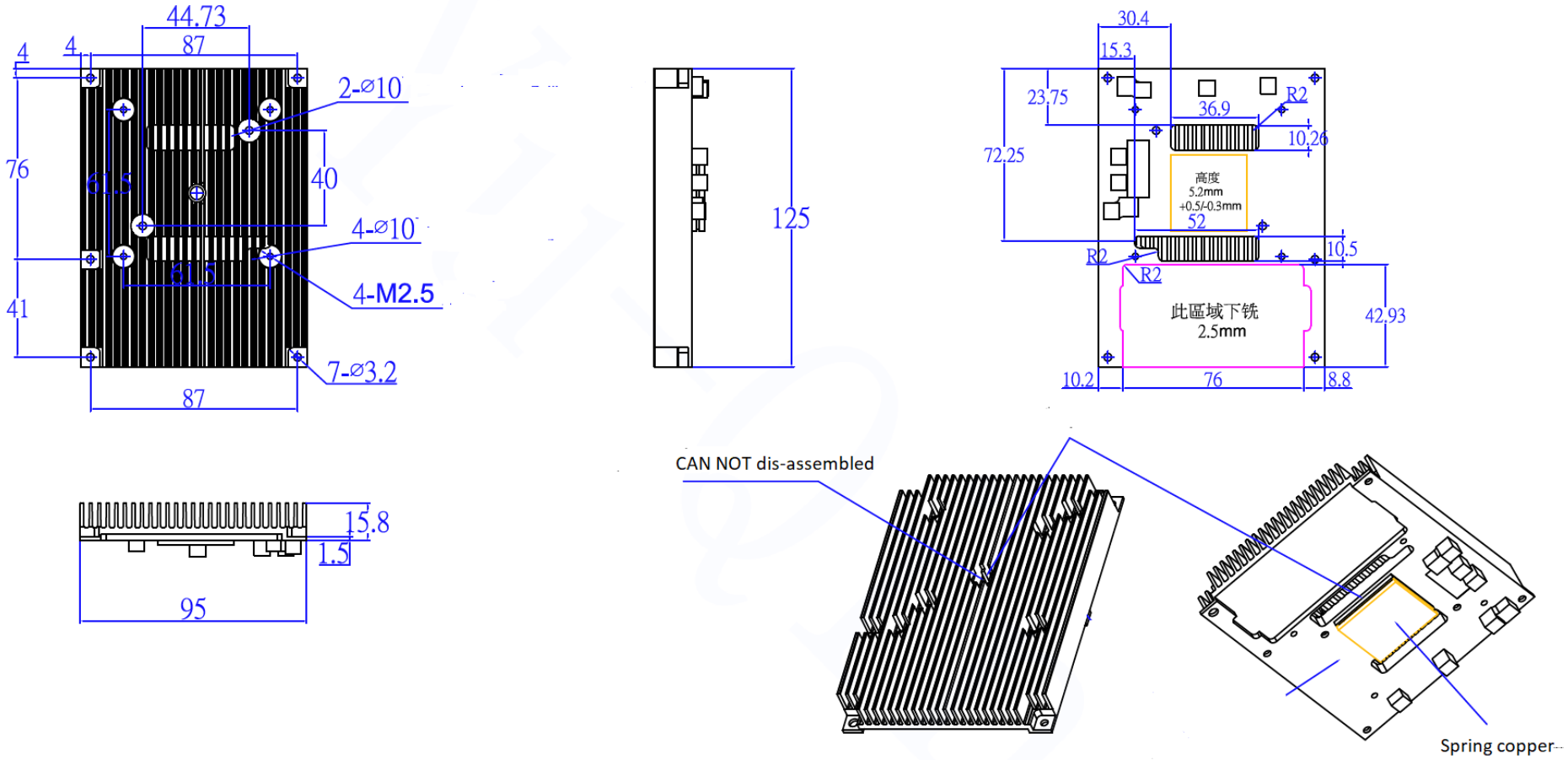


Figure 6 Heat sink / cooler mechanical dimensions

4.1 H/S Assembly guide

Please refer Figure 7 Mechanical Dimensions - Assembly view

4.2 Packaging

Package	Appearance	Size
Anti-Static bubble bag		180x135mm
White Paper Box		210x151x40mm
Shipping Box (10 pcs White paper box)		595x300x195mm

5 Signal Descriptions and Pin out Tables

Signal Tables Terminology Descriptions

I	Input to the Module
O	Output from the Module
I/O	Bi-direction input / output signal
OD	Open Drain output
CMOS	Logic input or output. Input thresholds and output levels shall be 80% of supply rail for high side and 20% of the relevant supply rail for low side.
PCIE	PCI Express compatible differential signal. Please refer to the PCI Express Specification for details. PCIE transmit pins (Module outputs) shall be AC coupled on the Module. PCIE receive pins (Module inputs) shall be DC coupled on the COM Express® Module and shall be assumed to be AC coupled off Module, close to the signal source. If the target PCI Express device resides on the Carrier Board, the Module PCIE receive lanes (target PCIE device transmit lanes) shall be AC coupled near the device on the Carrier Board. If the Carrier Board implements a PCIE slot, then these signals shall be AC coupled on the add-in card, not on the Carrier Board.
SATA	SATA compatible differential signal. Please refer to the SATA Specification for details. All COM Express® SATA signals shall be AC coupled on the Module.
LVDS	Low Voltage Differential Signal – 330mV nominal; 450mV maximum differential signal.
Analog	Inputs and Outputs used for LAN, and VGA are analog signals.
PU	Pull-up resistor on PCOM-B700G
PD	Pull-down resistor on PCOM-B700G

Table 10 Signal Tables Terminology Descriptions

#Note : Reserved / Not connected pins are highlighted as gray color.

Pin	Signal	Description	I/O	Type	Power / Tolerance	PU / PD	Note
A1	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A2	GBE0_MDI3-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A3	GBE0_MDI3+	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A4	GBE0_LINK100#	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A5	GBE0_LINK1000#	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
A6	GBE0_MDI2-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A7	GBE0_MDI2+	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A8	GBE0_LINK#	Gigabit Ethernet Controller 0 link indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
A9	GBE0_MDI1-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-

A10	GBE0_MDI1+	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A11	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A12	GBE0_MDI0-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A13	GBE0_MDI0+	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs	I/O	Analog	3.3V max Suspend	-	-
A14	GBE0_CTREF	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.	-	-	GND min 3.3V max	Placeholder 0 ohm to V_1P5_L1	-
A15	SUS_S3#	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.	O	CMOS	3.3V Suspend / 3.3V	PD 10kohm	-
A16	SATA0_TX+	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A17	SATA0_TX-	Serial ATA or SAS Channel 0 transmit differential pair.	O	SATA	AC coupled on Module	-	-
A18	SUS_S4#	Indicates system is in Suspend to Disk state. Active low output.	O	CMOS	3.3V Suspend / 3.3V	-	-
A19	SATA0_RX+	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-

A20	SATA0_RX-	Serial ATA or SAS Channel 0 receive differential pair.	I	SATA	AC coupled on Module	-	-
A21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A22	PCIE_TX15+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A23	PCIE_TX15-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A24	SUS_S5#	Indicates system is in Soft Off state.	O	CMOS	3.3V Suspend / 3.3V	-	There is no SUS_S5# in Broadwell-DE.
A25	PCIE_TX14+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A26	PCIE_TX14-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A27	BATLOW#	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	I	CMOS	3.3V Suspend / 3.3V	PU 1K ohm to 3VSB	-
A28	(S)ATA_ACT#	SATA activity indicator, active low.	I/O	CMOS	3.3V / 3.3V	PU 4.7K ohm to 3.3V	-
A29	RSVD	Reserved Pin	-	-	-	-	-
A30	RSVD	Reserved Pin	-	-	-	-	-
A31	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A32	RSVD	Reserved Pin	-	-	-	-	-

A33	RSVD	Reserved Pin	-	-	-	-	-
A34	BIOS_DIS0# / ESPI_SAFS	Selection straps to determine the BIOS boot device.The Carrier should only float these or pull them low. Shared pin with ESPI_SAFS	I	CMOS	NA	PU 10K ohm to 3.3V	-
A35	THRMTRIP#	Active low output indicating that the CPU has entered thermal shutdown	O	CMOS	3.3V / 3.3V	PU 1K ohm to 3VSB	-
A36	PCIE_TX13+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A37	PCIE_TX13-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A38	GND	GND	-	-	-	-	-
A39	PCIE_TX12+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A40	PCIE_TX12-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A41	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A42	USB2-	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A43	USB2+	USB differential pairs, channels 2. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-

A44	USB_2_3_OC#	USB over-current sense, USB channels 2 and 3. A pull-up for this line shallbe present on the Module. Do not pull this line high on the Carrier Board	I	CMOS	3.3V Suspend / 3.3V	PU 10K ohm to 3VSB	-
A45	USB0-	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A46	USB0+	USB differential pairs, channels 0. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
A47	VCC_RTC	Real-time clock circuit-power input. Nominally +3.0V.	-	PWR	-	-	-
A48	RSVD	Reserved Pin	-	-	-	-	-
A49	GBE0_SDP	Gigabit Ethernet Controller 0 Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 4.3.4 for details.	I/O	CMOS	3.3V Suspend / 3.3V	PU 10K ohm to 3VSB	-
A50	LPC_SERIRQ / ESPI_CS1#	LPC serial interrupt / Shared pin with ESPI_CS1#	I/O	CMOS	3.3V / 3.3V	PU 10K ohm to 3.3V	-
A51	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A52	PCIE_TX5+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A53	PCIE_TX5-	PCI Express Differential Transmit	O	PCIE	AC coupled on Module	-	-

		Pairs					
A54	GPI0	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A55	PCIE_TX4+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A56	PCIE_TX4-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A57	GND	GND	-	-	-	-	-
A58	PCIE_TX3+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A59	PCIE_TX3-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A60	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A61	PCIE_TX2+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A62	PCIE_TX2-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A63	GPI1	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A64	PCIE_TX1+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A65	PCIE_TX1-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A66	GND	GND	-	-	-	-	-

A67	GPI2	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A68	PCIE_TX0+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A69	PCIE_TX0-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A70	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A71	PCIE_TX8+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A72	PCIE_TX8-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A73	GND	GND	-	-	-	-	-
A74	PCIE_TX9+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A75	PCIE_TX9-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A76	GND	GND	-	-	-	-	-
A77	PCIE_TX10+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A78	PCIE_TX10-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A79	GND	GND	-	-	-	-	-
A80	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A81	PCIE_TX11+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
A82	PCIE_TX11-	PCI Express Differential Transmit	O	PCIE	AC coupled on Module	-	-

		Pairs					
A83	GND	GND	-	-	-	-	-
A84	NCSI_TX_EN	NCSI Transmit Enable (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PD 270 ohm	-
A85	GPI3	General purpose input pins. Pulled high internally on the Module.	I	CMOS	3.3V / 3.3V	PU 10k ohm to 3.3V	-
A86	RSVD	Reserved Pin	-	-	-	-	-
A87	RSVD	Reserved Pin	-	-	-	-	-
A88	PCIE_CLK_REF+	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A89	PCIE_CLK_REF-	Reference clock output for all PCI Express and PCI Express Graphics lanes.	O	PCIE	PCIE	-	-
A90	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A91	SPI_POWER	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier	O	-	3.3V Suspend / 3.3V	-	-
A92	SPI_MISO	Data in to Module from Carrier SPI	I	CMOS	3.3V Suspend / 3.3V	-	-

A93	GPO0	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
A94	SPI_CLK	Clock from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A95	SPI_MOSI	Data out from Module to Carrier SPI	O	CMOS	3.3V Suspend / 3.3V	-	-
A96	TPM_PP	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I	CMOS	3.3V / 3.3V	-	-
A97	TYPE10#	Dual use pin. Indicates to the Carrier Board that a Type 10 module is installed. Indicates to the Carrier that a Rev 1.0/2.0 module is installed	-	-	-	-	-
A98	SER0_TX	General purpose serial port transmitter	O	CMOS	5V / 12V	Placeholder PD 4.7K	-
A99	SER0_RX	General purpose serial port receiver	I	CMOS	5V / 12V	PU 47K to 3.3V	-
A100	GND(FIXED)	GND(FIXED)	-	-	-	-	-
A101	SER1_TX	General purpose serial port transmitter / CAN_TX	O	CMOS	5V / 12V	Placeholder PD 4.7K	-
A102	SER1_RX	General purpose serial port receiver / CAN_RX	I	CMOS	5V / 12V	PU 47K to 3.3V	-

A103	LID#	LID button. Low active signal used by the ACPI operating system for a LID switch.	I	CMOS	3.3V Suspend / 12V	PU 47K to 3VSB	-
A104	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A105	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A106	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A107	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A108	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A109	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
A110	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B1	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B2	GBE0_ACT#	Gigabit Ethernet Controller 1 activity indicator, active low.	OD	CMOS	3.3V Suspend / 3.3V	-	-
B3	LPC_FRAME# / ESPI_CS0#	LPC frame indicates the start of an LPC cycle / Shared pin with ESPI_CS0#	O	CMOS	3.3V / 3.3V	PU 8.2k ohm to 3.3V	-
B4	LPC_AD0 / ESPI_IO_0	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-

B5	LPC_AD1 / ESPI_IO_1	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B6	LPC_AD2 / ESPI_IO_2	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B7	LPC_AD3 / ESPI_IO_3	LPC multiplexed address, command and data bus / Shared pin with ESPI IO	I/O	CMOS	3.3V / 3.3V	-	-
B8	LPC_DRQ0# / ESPI_ALERT0#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B9	LPC_DRQ1# / ESPI_ALERT1#	LPC serial DMA request / Shared pin with ESPI_ALERT	I	CMOS	3.3V / 3.3V	-	-
B10	LPC_CLK / ESPI_CK	LPC clock output - 33MHz nominal / Shared pin with ESPI_Clock	O	CMOS	3.3V / 3.3V	-	-
B11	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B12	PWRBTN#	Power button to bring system out of S5 (soft off), active on falling edge.	I	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
B13	SMB_CK	System Management Bus bidirectional clock line.	I/O	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-
B14	SMB_DAT	System Management Bus bidirectional data line.	I/O	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-

B15	SMB_ALERT#	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	I	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-
B16	SATA1_TX+	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B17	SATA1_TX-	Serial ATA or SAS Channel 1 transmit differential pair.	O	SATA	AC coupled on Module	-	-
B18	SUS_STAT# / ESPI_RESET#	Indicates imminent suspend operation; used to notify LPC devices / Shared pin with ESPI_RESET	O	CMOS	3.3V Suspend / 3.3V	-	-
B19	SATA1_RX+	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B20	SATA1_RX-	Serial ATA or SAS Channel 1 receive differential pair.	I	SATA	AC coupled on Module	-	-
B21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B22	PCIE_RX15+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B23	PCIE_RX15-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B24	PWR_OK	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow carrier based FPGAs or	I	CMOS	3.3V / 3.3V	-	-

		other configurable devices time to be programmed.					
B25	PCIE_RX14+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B26	PCIE_RX14-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B27	WDT	Output indicating that a watchdog time-out event has occurred.	O	CMOS	3.3V / 3.3V	-	-
B28	RSVD	Reserved Pin	-	-	-	-	-
B29	RSVD	Reserved Pin	-	-	-	-	-
B30	RSVD	Reserved Pin	-	-	-	-	-
B31	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B32	SPKR	Output for audio enunciator	O	CMOS	3.3V / 3.3V	-	-
B33	I2C_CK	General purpose I2C port clock output	I/O	CMOS	3.3V Suspend / 3.3V	PU 2.2k ohm to 3.3V	-
B34	I2C_DAT	General purpose I2C port data I/O line	I/O	CMOS	3.3V Suspend / 3.3V	PU 2.2k ohm to 3.3V	-
B35	THRM#	Input from off-Module temp sensor indicating an over-temp situation	I	CMOS	3.3V / 3.3V	PU 1k ohm to 3VSB	-
B36	PCIE_RX13+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B37	PCIE_RX13-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

B38	GND	GND	-	-	-	-	-
B39	PCIE_RX12+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B40	PCIE_RX12-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B41	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B42	USB3-	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B43	USB3+	USB differential pairs, channels 3. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B44	USB_0_1_OC#	USB over-current sense, USB channels 0 and 1. A pull-up for this line shallbe present on the Module. Do not pull this line high on the Carrier Board	I	CMOS	3.3V Suspend / 3.3V	PU 10 kohm to 3VSB	-
B45	USB1-	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-
B46	USB1+	USB differential pairs, channels 1. All USB ports except USB7, if implemented, shall be host ports.	I/O	USB	3.3V Suspend / 3.3V	-	-

B47	ESPI_EN	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If pulled down by the Carrier LPC mode is selected. If pulled up or left floating, eSPI is selected if available. This signal is pulled up on the Module. This signal is a “don’t care” for Modules that do not support eSPI	I	CMOS	NA	-	-
B48	USB0_HOST_PRSNT	Module USB client may may detect the presence of a USB host on USB0. A high value indicates that a host is present.	I	CMOS	3.3V Suspend/ 3.3V	-	-
B49	SYS_RESET#	Reset button input. Active low request for module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used	I	CMOS	3.3V Suspend / 3.3V	PU 4.7k ohm to 3VSB	-

B50	CB_RESET#	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and mayresult from a low SYS_RESET#input, a low PWR_OKinput, a VCC_12Vpower input that falls below the minimum specification, a watchdog timeout, or maybe initiated by the Module software.	O	CMOS	3.3V Suspend / 3.3V	PU 1k ohm to 3VSB (OD)	-
B51	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B52	PCIE_RX5+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B53	PCIE_RX5-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B54	GPO1	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B55	PCIE_RX4+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B56	PCIE_RX4-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B57	GPO2	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B58	PCIE_RX3+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B59	PCIE_RX3-	PCI Express Differential Receive	I	PCIE	AC coupled off Module	-	-

		Pairs					
B60	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B61	PCIE_RX2+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B62	PCIE_RX2-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B63	GPO3	General purpose output pins. Upon a hardware reset, these outputs should be low.	O	CMOS	3.3V / 3.3V	-	-
B64	PCIE_RX1+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B65	PCIE_RX1-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B66	WAKE0#	PCI Express wake up signal.	I	CMOS	3.3V Suspend / 3.3V	PU 1k ohm to 3VSB	-
B67	WAKE1#	General purpose wake up signal. Maybe used to implement wake-up on PS2 keyboard or mouse activity	I	CMOS	3.3V Suspend / 3.3V	PU 10k ohm to 3VSB	-
B68	PCIE_RX0+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B69	PCIE_RX0-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B70	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B71	PCIE_RX8+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

B72	PCIE_RX8-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B73	GND	GND	-	-	-	-	-
B74	PCIE_RX9+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B75	PCIE_RX9-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B76	GND	GND	-	-	-	-	-
B77	PCIE_RX10+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B78	PCIE_RX10-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B79	GND	GND	-	-	-	-	-
B80	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B81	PCIE_RX11+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B82	PCIE_RX11-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
B83	GND	GND	-	-	-	-	-
B84	VCC_5V_SBY	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B85	VCC_5V_SBY	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B86	VCC_5V_SBY	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-
B87	VCC_5V_SBY	Standby power input: +5.0V nominal.	-	PWR	+5.0V	-	-

B88	BIOS_DIS1# / ESPI_BBS	Selection straps to determine the BIOS boot device.The Carrier should only float these or pull them low / Shared pin with ESPI_BBS	I	CMOS	NA	PU 10k ohm to 3.3V	-
B89	NCSI_RX_ER	NC-SI Receive error	O	-	3.3V Suspend / 3.3V	-	-
B90	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B91	NCSI_CLK_IN	NC-SI Clock reference for receive, transmit, and control Interface. (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	-	-
B92	NCSI_RXD1	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	PU 5.1K to 1.05V	-
B93	NCSI_RXD0	NC-SI Receive Data (from NC to BMC).	O	-	3.3V Suspend / 3.3V	PU 5.1K to 1.05V	-
B94	NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that the transmitted data from NC to BMC is valid.	O	-	3.3V Suspend / 3.3V	PD 270 ohm	-
B95	NCSI_TXD1	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PU 10K to 1.05V	-
B96	NCSI_TXD0	NC-SI Transmit Data (from BMC to NC). (PD 10K on Carrier when NC-SI is not used on Carrier)	I	-	3.3V Suspend / 3.3V	PU 10K to 1.05V	-

B97	SPI_CS#	Chip select for Carrier Board SPI - maybe sourced from chipset SPI0 or SPI1	O	CMOS	3.3V Suspend / 3.3V	-	-
B98	NCSI_ARB_IN	NC-SI hardware arbitration input.	I	-	3.3V Suspend / 3.3V	PD 10k ohm	-
B99	NCSI_ARB_OUT	NC-SI hardware arbitration output.	O	-	3.3V Suspend / 3.3V	PU 10K to 1.05V	-
B100	GND(FIXED)	GND(FIXED)	-	-	-	-	-
B101	FAN_PWNOUT	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM	O	CMOS	3.3V / 12V	PU 10K to 3.3V	-
B102	FAN_TACHIN	Fan tachometer input for a fan with a two pulse output.	I	CMOS	3.3V / 12V	PU 10K to 3.3V	-
B103	SLEEP#	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I	CMOS	3.3V Suspend / 12V	PU 10K to 3VSB	-
B104	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B105	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B106	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B107	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B108	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-

B109	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
B110	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C1	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C2	GND	GND	-	-	-	-	-
C3	USB_SSRX0-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C4	USB_SSRX0+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C5	GND	GND	-	-	-	-	-
C6	USB_SSRX1-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C7	USB_SSRX1+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C8	GND	GND	-	-	-	-	-
C9	USB_SSRX2-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C10	USB_SSRX2+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C11	GND(FIXED)					-	-

C12	USB_SSRX3-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C13	USB_SSRX3+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	I	PCIE	AC coupled off Module	-	-
C14	GND	GND	-	-	-	-	-
C15	10G_PHY_MDC_SCL3	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C16	10G_PHY_MDC_SCL2	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C17	10G_SDP2	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	-	-
C18	GND	GND	-	-	-	-	-

C19	PCIE_RX6+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C20	PCIE_RX6-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C22	PCIE_RX7+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C23	PCIE_RX7-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C24	10G_INT2	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	-	-
C25	GND	GND	-	-	-	-	-
C26	10G_KR_RX3+	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C27	10G_KR_RX3-	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C28	GND	GND	-	-	-	-	-
C29	10G_KR_RX2+	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C30	10G_KR_RX2-	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C31	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C32	10G_SFP_SDA3	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an	I/O	OD	3.3V Suspend / 3.3V	-	-

		external Optical SFP Module					
C33	10G_SFP_SDA2	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	-	-
C34	10G_PHY_RST_23	Output signal that resets an optical PHY on port 2 and port3 (Not used with copper PHY)	O	-	3.3V Suspend / 3.3V	-	-
C35	10G_PHY_RST_01	Output signal that resets an optical PHY on port 0 and port1 (Not used with copper PHY)	O	-	3.3V Suspend / 3.3V	-	-
C36	10G_LED_SDA	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.	I/O	OD	3.3V Suspend / 3.3V	-	-
C37	10G_LED_SCL	I2C Clock,of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs	I/O	OD	3.3V Suspend / 3.3V	-	-
C38	10G_SFP_SDA1	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an	I/O	OD	3.3V Suspend / 3.3V	PU 4.7K to 3VSB	-

		external Optical SFP Module					
C39	10G_SFP_SDA0	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 4.7K to 3VSB	-
C40	10G_SDP0	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	PU 1K to 3VSB	-
C41	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C42	10G_KR_RX1+	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C43	10G_KR_RX1-	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C44	GND	GND	-	-	-	-	-
C45	10G_PHY_MDC_SCL1	MDIO Mode: Management Data I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C46	10G_PHY_MDC_SCL0	MDIO Mode: Management Data	O	-	3.3V Suspend / 3.3V	-	-

		I/O interface mode clock signal for serial data transfers between the MAC and an external PHY.					
		I2C Mode: I2C clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
C47	10G_INT0	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	-	-
C48	GND	GND	-	-	-	-	-
C49	10G_KR_RX0+	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C50	10G_KR_RX0-	10GBASE-KR ports, receive input differential pairs.	I	KR	AC coupled on Module	-	-
C51	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C52	PCIE_RX16+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C53	PCIE_RX16-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C54	TYPE0#	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	-	-
C55	PCIE_RX17+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C56	PCIE_RX17-	PCI Express Differential Receive	I	PCIE	AC coupled off Module	-	-

		Pairs					
C57	TYPE1#	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	-	-
C58	PCIE_RX18+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C59	PCIE_RX18-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C60	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C61	PCIE_RX19+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C62	PCIE_RX19-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C63	RSVD	Reserved Pin	-	-	-	-	-
C64	RSVD	Reserved Pin	-	-	-	-	-
C65	PCIE_RX20+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C66	PCIE_RX20-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C67	RAPID_SHUTDOWN	Trigger for Rapid Shutdown. Must be driven to 5V though a <=50 ohm source impedance for a	I	CMOS	5.0V Suspend/ 5.0V	-	-
C68	PCIE_RX21+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C69	PCIE_RX21-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C70	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C71	PCIE_RX22+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C72	PCIE_RX22-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C73	GND	GND	-	-	-	-	-
C74	PCIE_RX23+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C75	PCIE_RX23-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C76	GND	GND	-	-	-	-	-
C77	RSVD	Reserved Pin	-	-	-	-	-
C78	PCIE_RX24+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C79	PCIE_RX24-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C80	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C81	PCIE_RX25+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C82	PCIE_RX25-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C83	RSVD	Reserved Pin	-	-	-	-	-
C84	GND	GND	-	-	-	-	-
C85	PCIE_RX26+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C86	PCIE_RX26-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-

C87	GND	GND	-	-	-	-	-
C88	PCIE_RX27+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C89	PCIE_RX27-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C90	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C91	PCIE_RX28+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C92	PCIE_RX28-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C93	GND	GND	-	-	-	-	-
C94	PCIE_RX29+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C95	PCIE_RX29-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C96	GND	GND	-	-	-	-	-
C97	RSVD	Reserved Pin	-	-	-	-	-
C98	PCIE_RX30+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C99	PCIE_RX30-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C100	GND(FIXED)	GND(FIXED)	-	-	-	-	-
C101	PCIE_RX31+	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C102	PCIE_RX31-	PCI Express Differential Receive Pairs	I	PCIE	AC coupled off Module	-	-
C103	GND	GND	-	-	-	-	-

C104	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C105	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C106	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C107	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C108	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C109	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
C110	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D1	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D2	GND	GND	-	-	-	-	-
D3	USB_SSTX0-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D4	USB_SSTX0+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D5	GND	GND	-	-	-	-	-
D6	USB_SSTX1-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-

D7	USB_SSTX1+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D8	GND	GND	-	-	-	-	-
D9	USB_SSTX2-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D10	USB_SSTX2+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D11	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D12	USB_SSTX3-	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D13	USB_SSTX3+	Additional transmit signal differential pairs for the SuperSpeed USB data path.	O	PCIE	AC coupled on Module	-	-
D14	GND	GND	-	-	-	-	-
D15	10G_PHY_MDIO_SDA3	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-

D16	10G_PHY_MDIO_SDA2	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
D17	10G_SDP3	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	-	-
D18	GND	GND	-	-	-	-	-
D19	PCIE_TX6+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D20	PCIE_TX6-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D21	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D22	PCIE_TX7+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D23	PCIE_TX7-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D24	10G_INT3	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	-	-
D25	GND	GND	-	-	-	-	-
D26	10G_KR_TX3+	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-

D27	10G_KR_TX3-	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D28	GND	GND	-	-	-	-	-
D29	10G_KR_TX2+	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D30	10G_KR_TX2-	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D31	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D32	10G_SFP_SCL3	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	-	-
D33	10G_SFP_SCL2	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	-	-
D34	10G_PHY_SEL_23	Phy mode select pin: If high Phy2 and Phy3 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode, this pin should be left not connected on the Carrier. For I2C mode pull down with 1K on Carrier	I	-	3.3V Suspend / 3.3V	-	-

D35	10G_PHY_SEL_01	Phy mode select pin: If high Phy0 and Phy1 are configured by MDIO. If low Phy2 and Phy3 are configured by I2C. For MDIO mode, this pin should be left not connected on the Carrier. For I2C mode pull down with 1K on Carrier	I	-	3.3V Suspend / 3.3V	-	-
D36	RSVD	RSVD	-	-	-	-	-
D37	RSVD	RSVD	-	-	-	-	-
D38	10G_SFP_SCL1	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 4.7K to 3VSB	-
D39	10G_SFP_SCL0	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module	I/O	OD	3.3V Suspend / 3.3V	PU 4.7K to 3VSB	-
D40	10G_SDP1	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal	I/O	-	3.3V Suspend / 3.3V	PU 1K to 3VSB	-
D41	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D42	10G_KR_TX1+	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D43	10G_KR_TX1-	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-

D44	GND	GND	-	-	-	-	-
D45	10G_PHY_MDIO_SDA1	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
D46	10G_PHY_MDIO_SDA0	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY.	O	-	3.3V Suspend / 3.3V	-	-
		I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY.	I/O OD	-	3.3V Suspend / 3.3V	-	-
D47	10G_INT1	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller	I	-	3.3V Suspend / 3.3V	-	-
D48	GND	GND	-	-	-	-	-
D49	10G_KR_TX0+	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D50	10G_KR_TX0-	10GBASE-KR ports, transmit output differential pairs.	O	KR	AC coupled on Carrier	-	-
D51	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D52	PCIE_TX16+	PCI Express Differential Transmit	O	PCIE	AC coupled on Module	-	-

		Pairs					
D53	PCIE_TX16-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D54	RSVD	Reserved Pin	-	-	-	-	-
D55	PCIE_TX17+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D56	PCIE_TX17-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D57	TYPE2#	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module.	-	-	-	Connect to GND	-
D58	PCIE_TX18+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D59	PCIE_TX18-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D60	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D61	PCIE_TX19+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D62	PCIE_TX19-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D63	RSVD	Reserved Pin	-	-	-	-	-
D64	RSVD	Reserved Pin	-	-	-	-	-
D65	PCIE_TX20+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D66	PCIE_TX20-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-

D67	GND	GND	-	-	-	-	-
D68	PCIE_TX21+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D69	PCIE_TX21-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D70	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D71	PCIE_TX22+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D72	PCIE_TX22-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D73	GND	GND	-	-	-	-	-
D74	PCIE_TX23+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D75	PCIE_TX23-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D76	GND	GND	-	-	-	-	-
D77	RSVD	Reserved Pin	-	-	-	-	-
D78	PCIE_TX24+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D79	PCIE_TX24-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D80	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D81	PCIE_TX25+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D82	PCIE_TX25-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D83	RSVD	Reserved Pin	-	-	-	-	-

D84	GND	GND	-	-	-	-	-
D85	PCIE_TX26+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D86	PCIE_TX26-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D87	GND	GND	-	-	-	-	-
D88	PCIE_TX27+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D89	PCIE_TX27-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D90	GND(FIXED)	GND(FIXED)	-	-	-	-	-
D91	PCIE_TX28+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D92	PCIE_TX28-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D93	GND	GND	-	-	-	-	-
D94	PCIE_TX29+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D95	PCIE_TX29-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D96	GND	GND	-	-	-	-	-
D97	RSVD	Reserved Pin	-	-	-	-	-
D98	PCIE_TX30+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D99	PCIE_TX30-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D100	GND(FIXED)	GND(FIXED)	-	-	-	-	-

D101	PCIE_TX31+	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D102	PCIE_TX31-	PCI Express Differential Transmit Pairs	O	PCIE	AC coupled on Module	-	-
D103	GND	GND	-	-	-	-	-
D104	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D105	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D106	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D107	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D108	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D109	VCC_12V	Primary power input: +12V nominal.	-	PWR	+12V	-	-
D110	GND(FIXED)	GND(FIXED)	-	-	-	-	-

Table 11 Pin out description

6 BIOS Setup Items

PCOM-B700GVG is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, PCOM-B700GVG communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

6.1 Entering Setup -- Launch System Setup

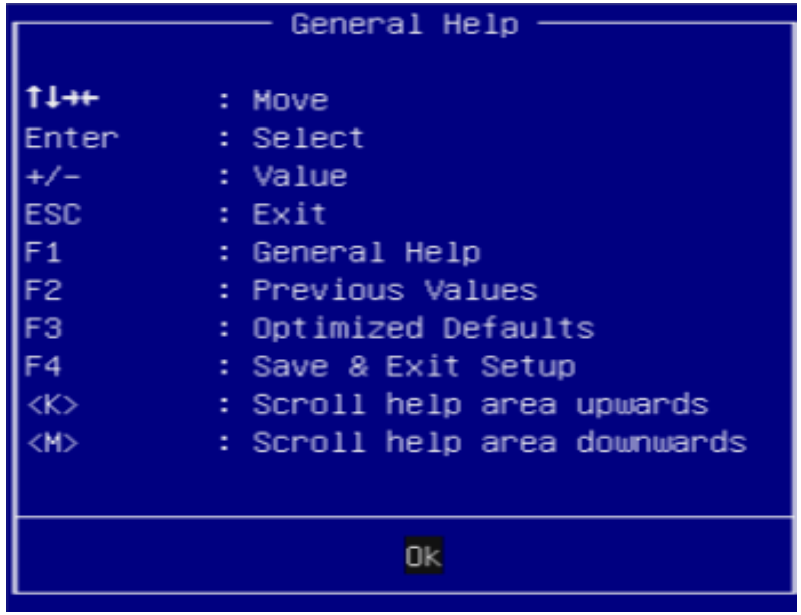
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

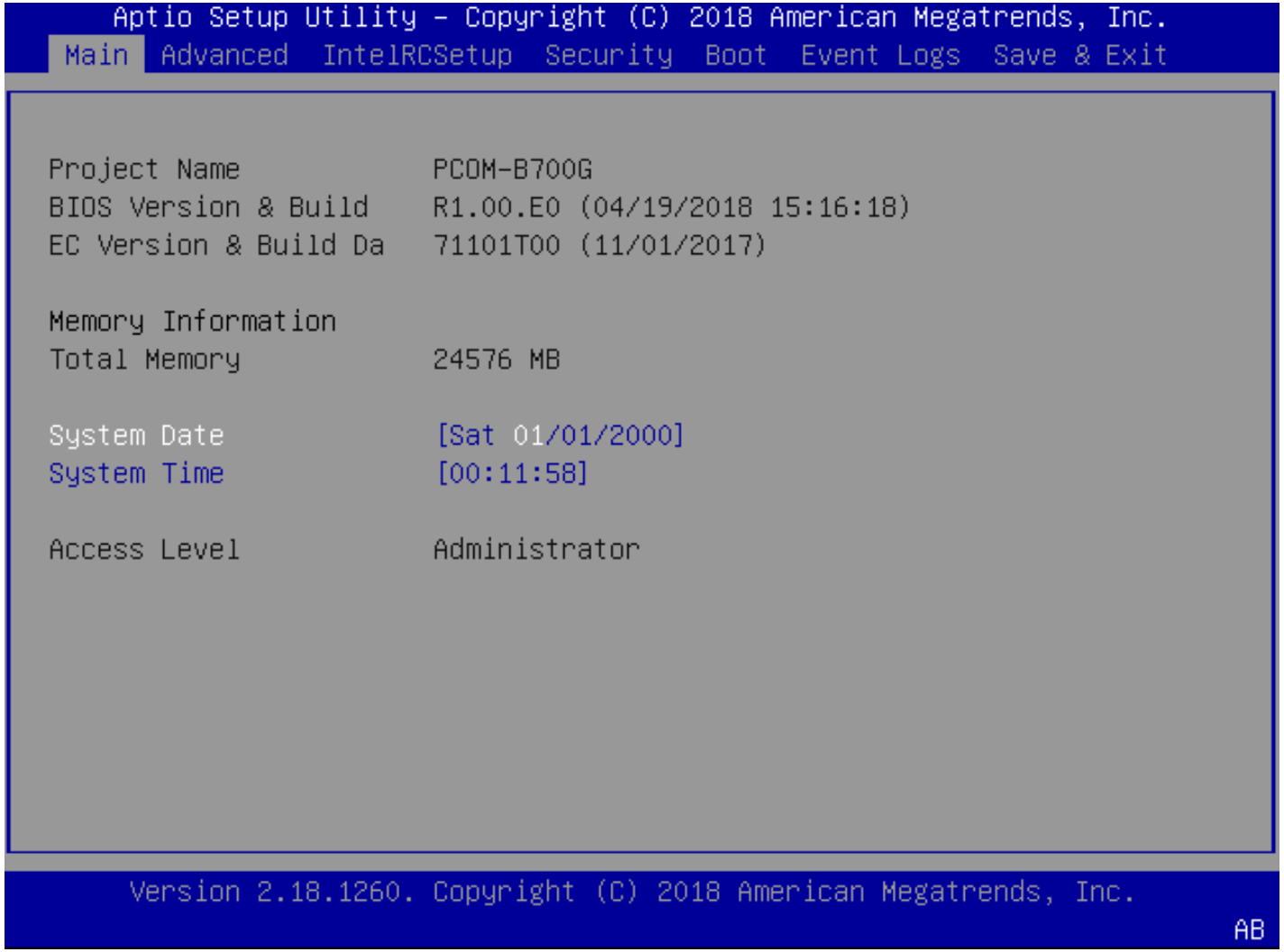
If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run General Help or Resume

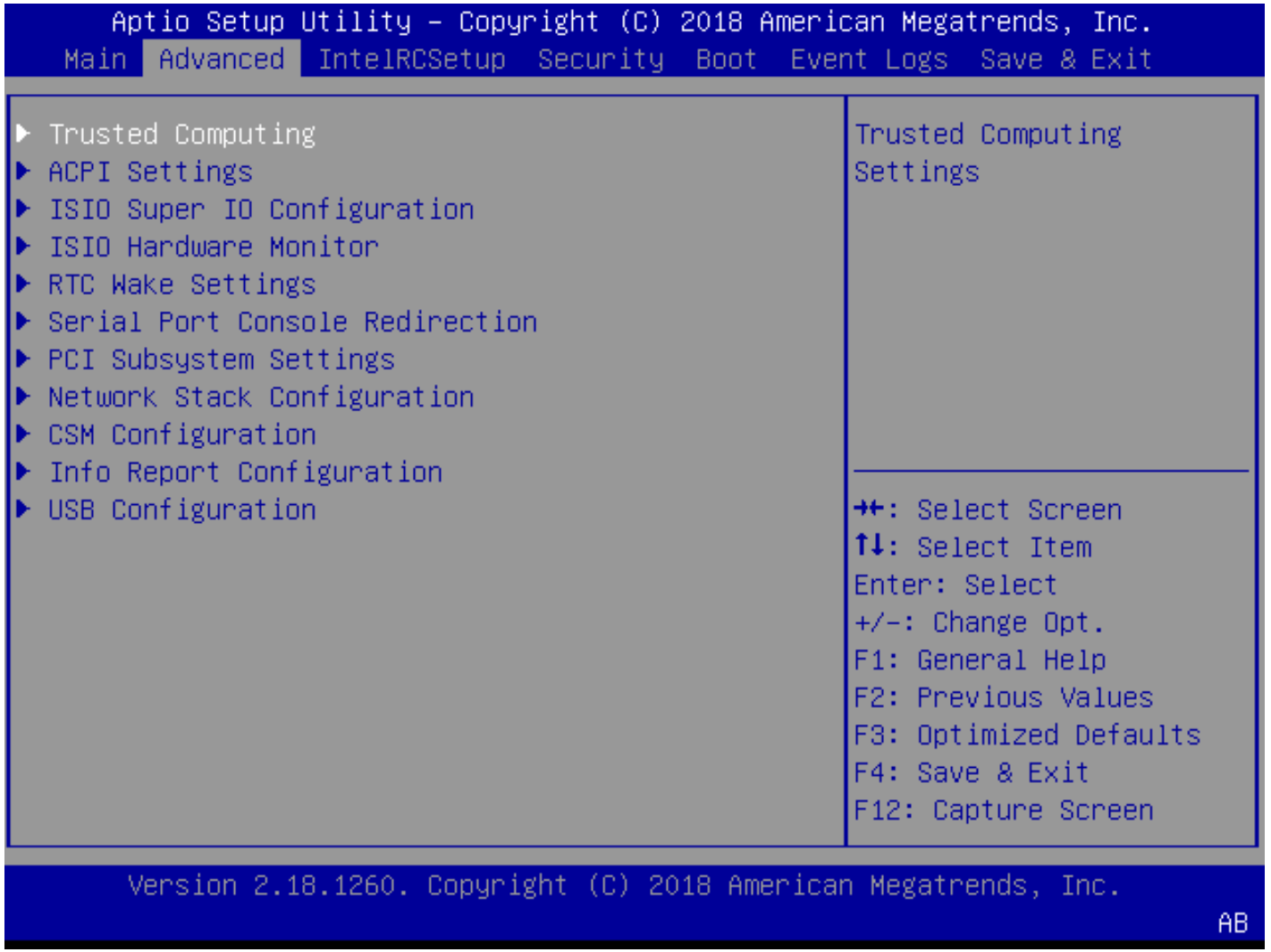
The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



6.2 Main


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
Main Advanced IntelRCSetup Security Boot Event Logs Save & Exit
Project Name PCOM-B700G
BIOS Version & Build R1.00.E0 (04/19/2018 15:16:18)
EC Version & Build Da 71101T00 (11/01/2017)
Memory Information
Total Memory 24576 MB
System Date [Sat 01/01/2000]
System Time [00:11:58]
Access Level Administrator
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.
AB

6.3 Advanced


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
Main Advanced IntelRCSetup Security Boot Event Logs Save & Exit
Trusted Computing
ACPI Settings
ISIO Super IO Configuration
ISIO Hardware Monitor
RTC Wake Settings
Serial Port Console Redirection
PCI Subsystem Settings
Network Stack Configuration
CSM Configuration
Info Report Configuration
USB Configuration
Trusted Computing Settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
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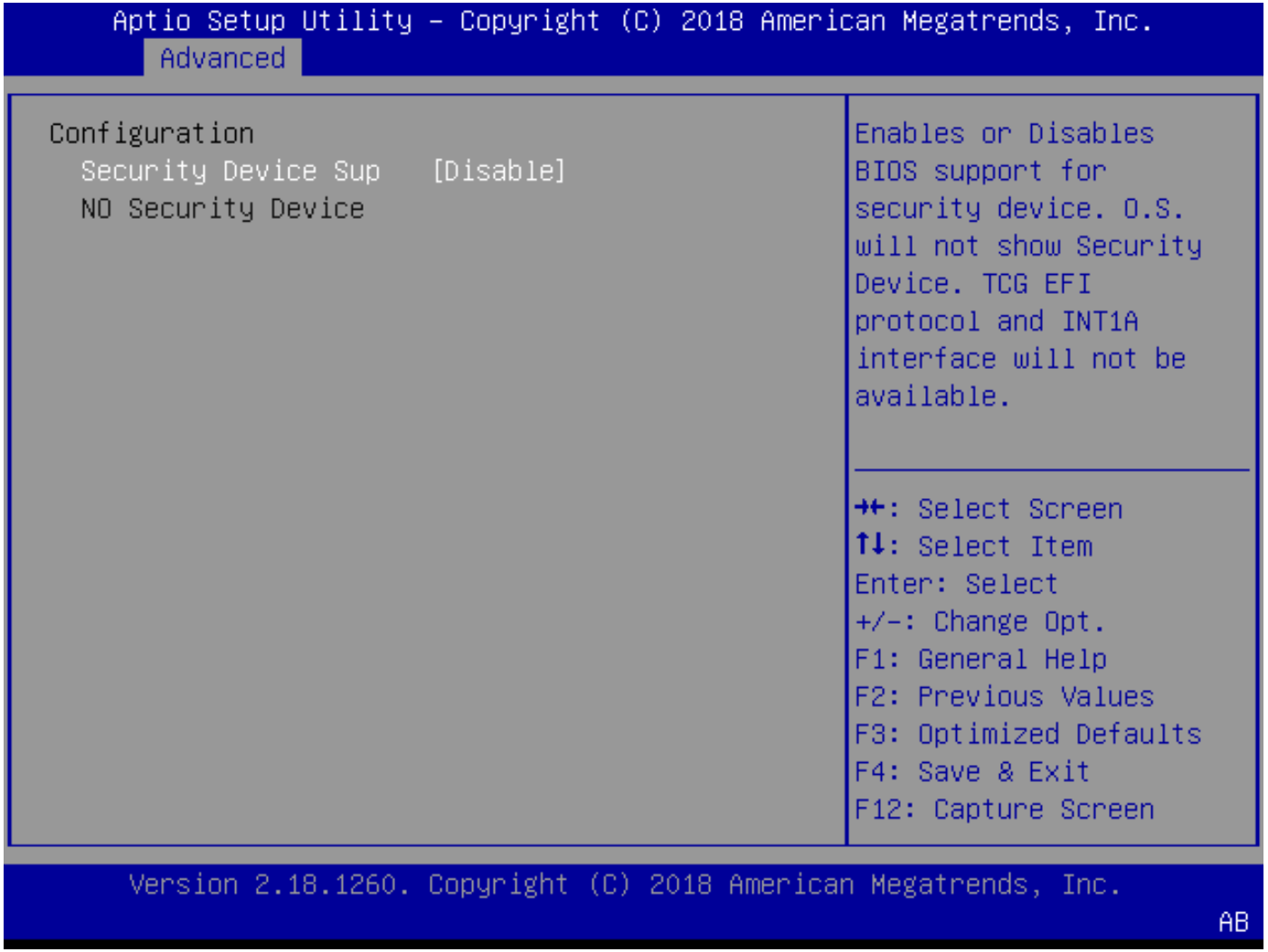
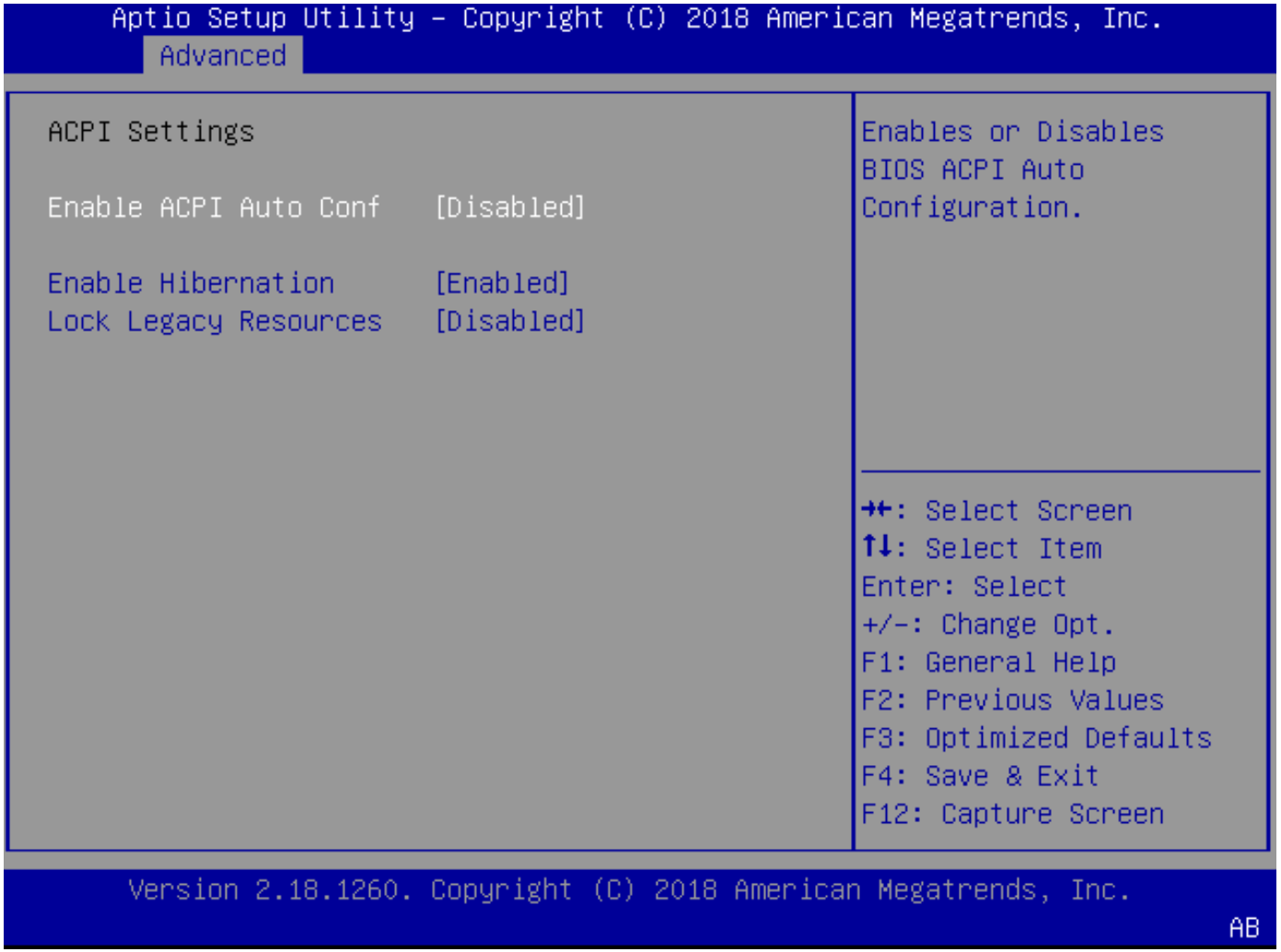
AB

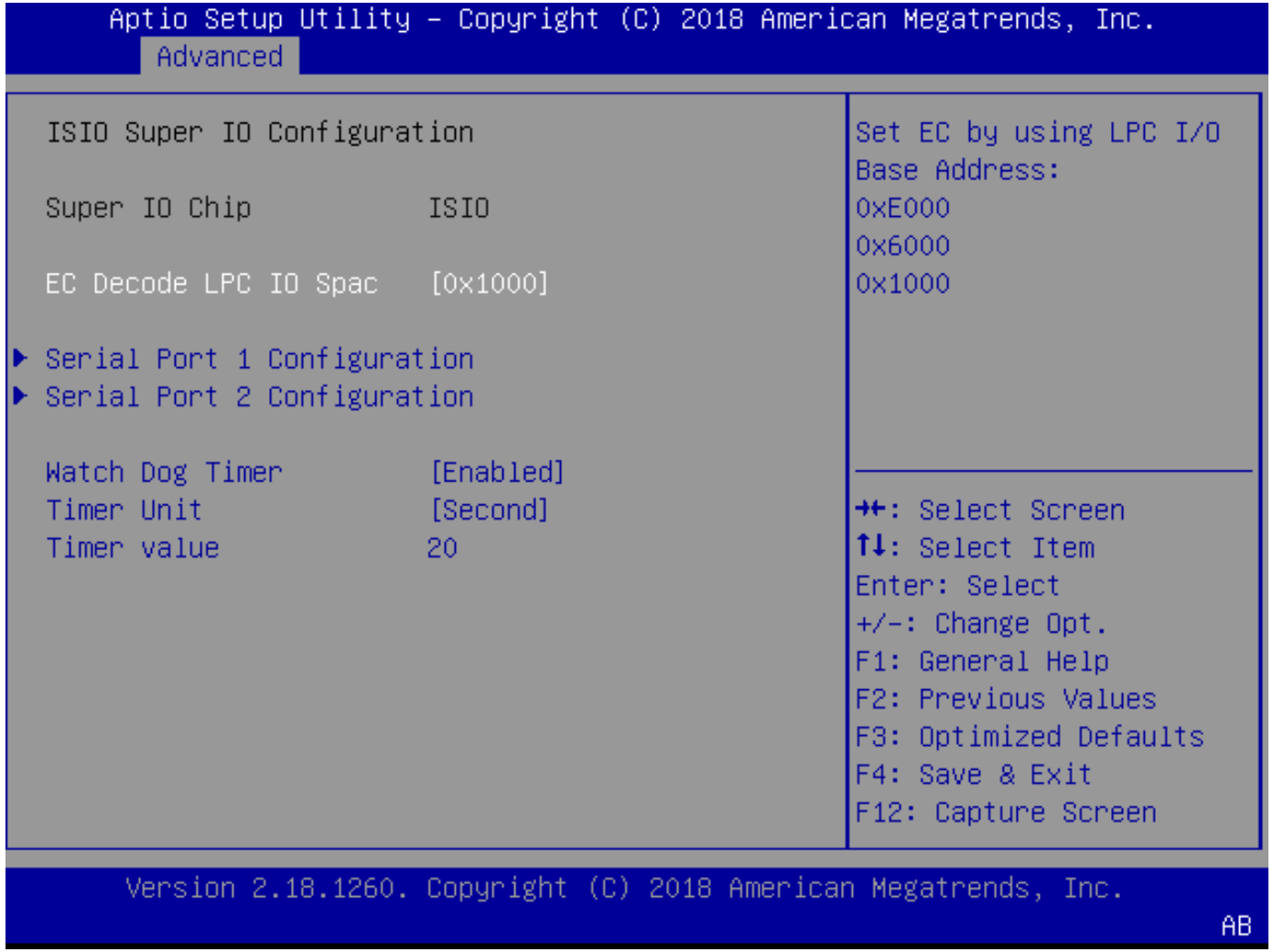
Trusted Computing



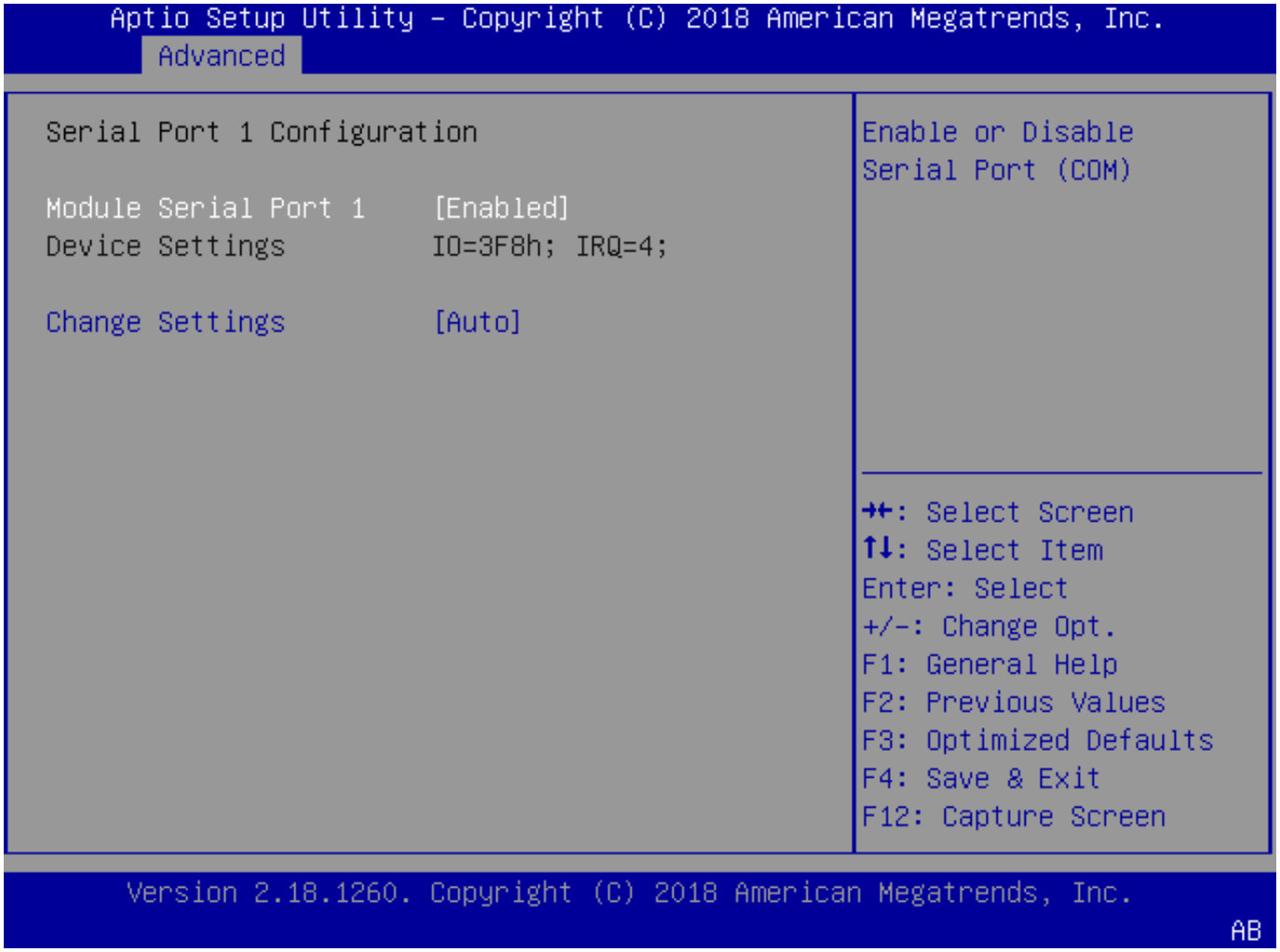
ACPI Settings



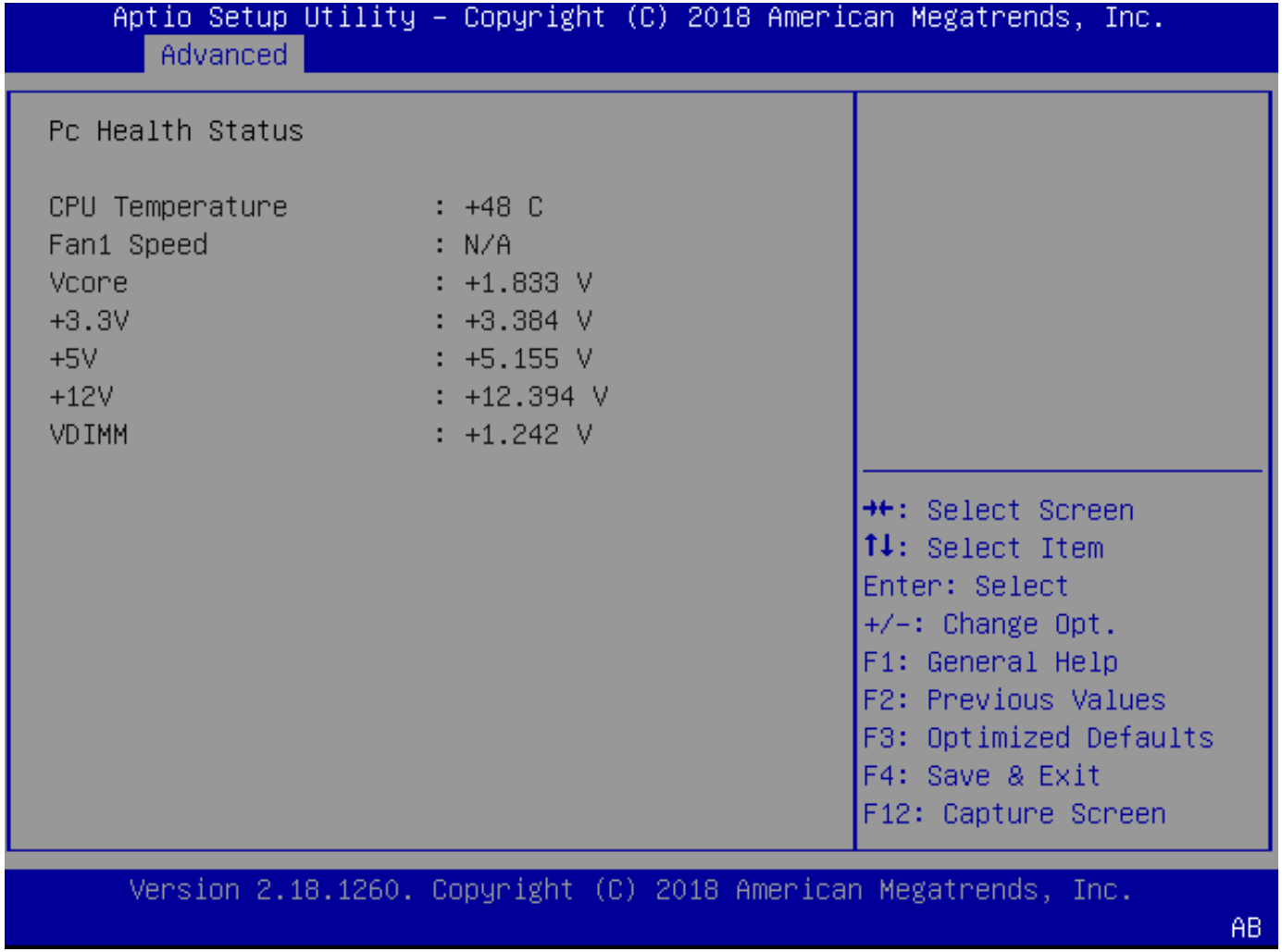
ISIO Super IO Configuration



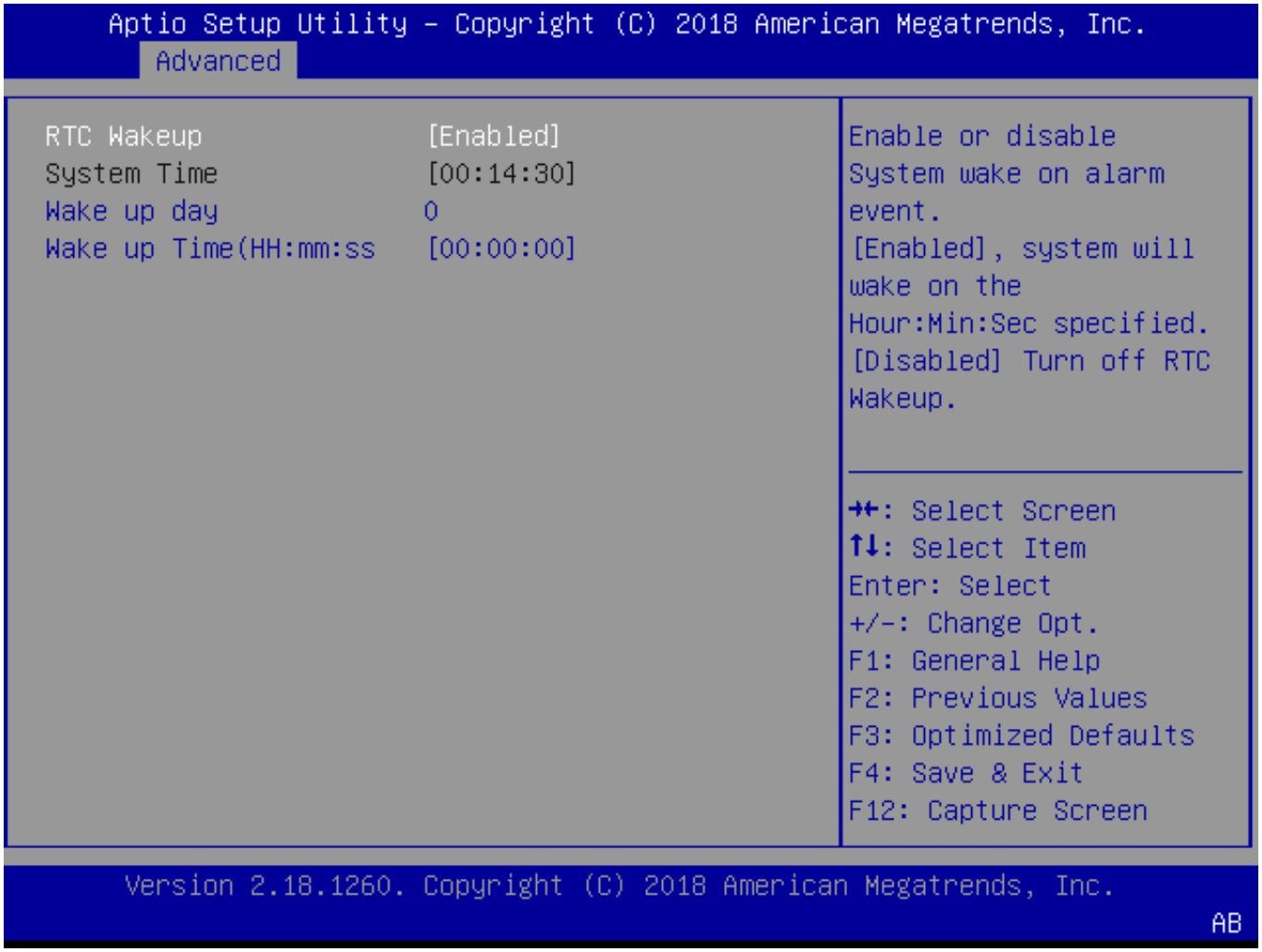
Serial Port (1~2) Configuration



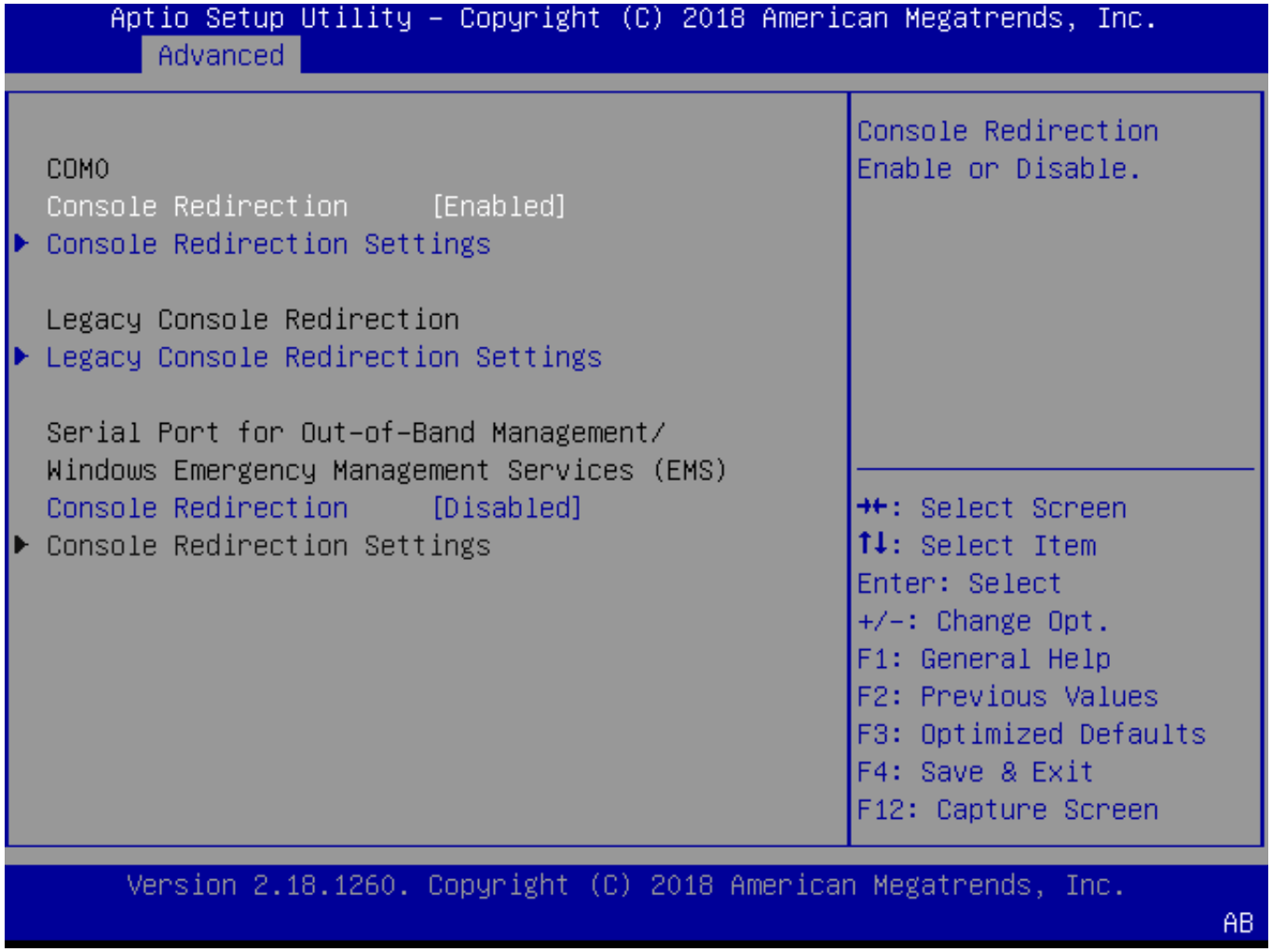
ISIO Hardware Monitor



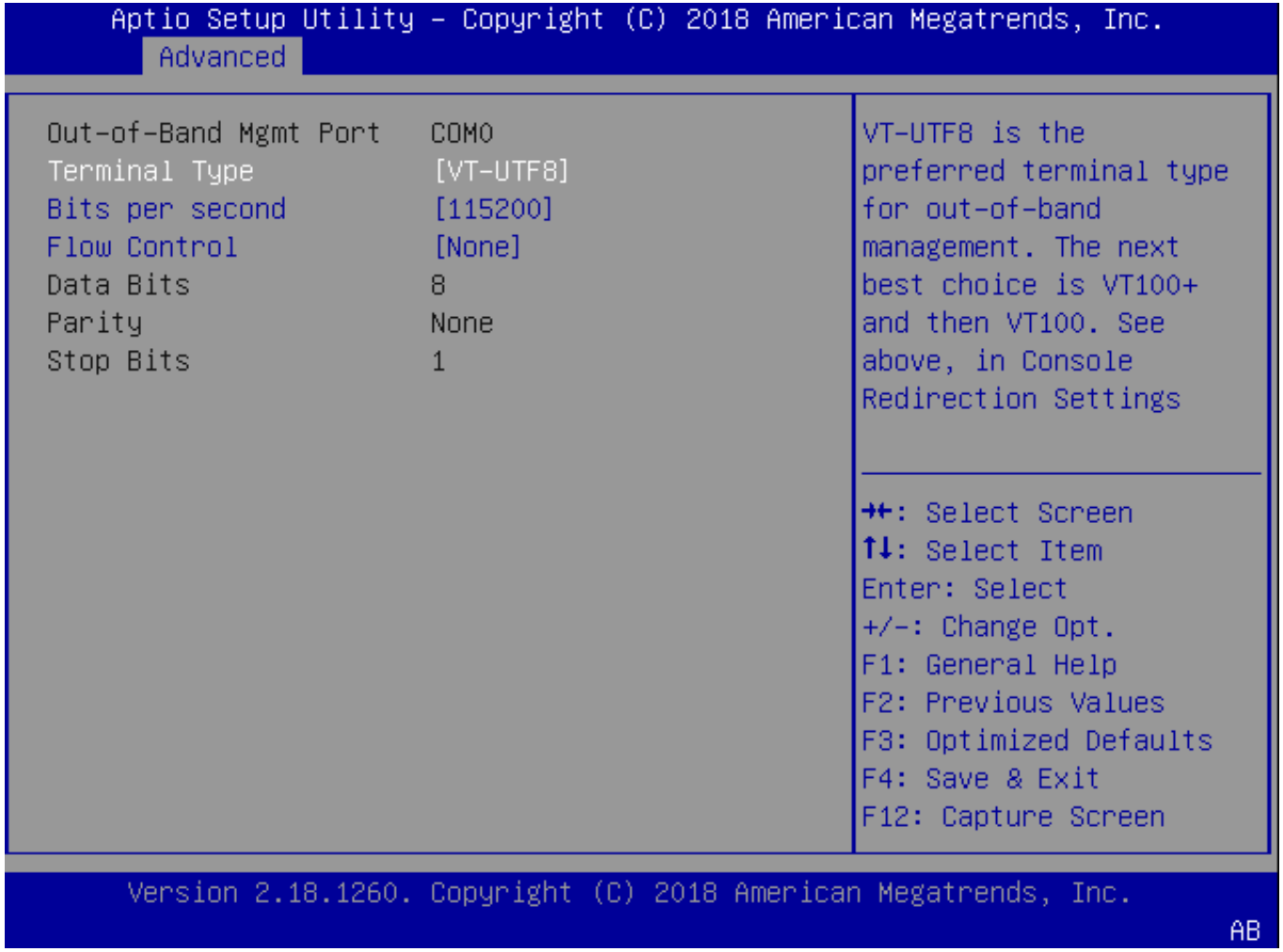
RTC Wakeup


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
Advanced
RTC Wakeup [Enabled]
System Time [00:14:30]
Wake up day 0
Wake up Time(HH:mm:ss [00:00:00]
Enable or disable System wake on alarm event.
[Enabled], system will wake on the Hour:Min:Sec specified.
[Disabled] Turn off RTC Wakeup.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.
AB

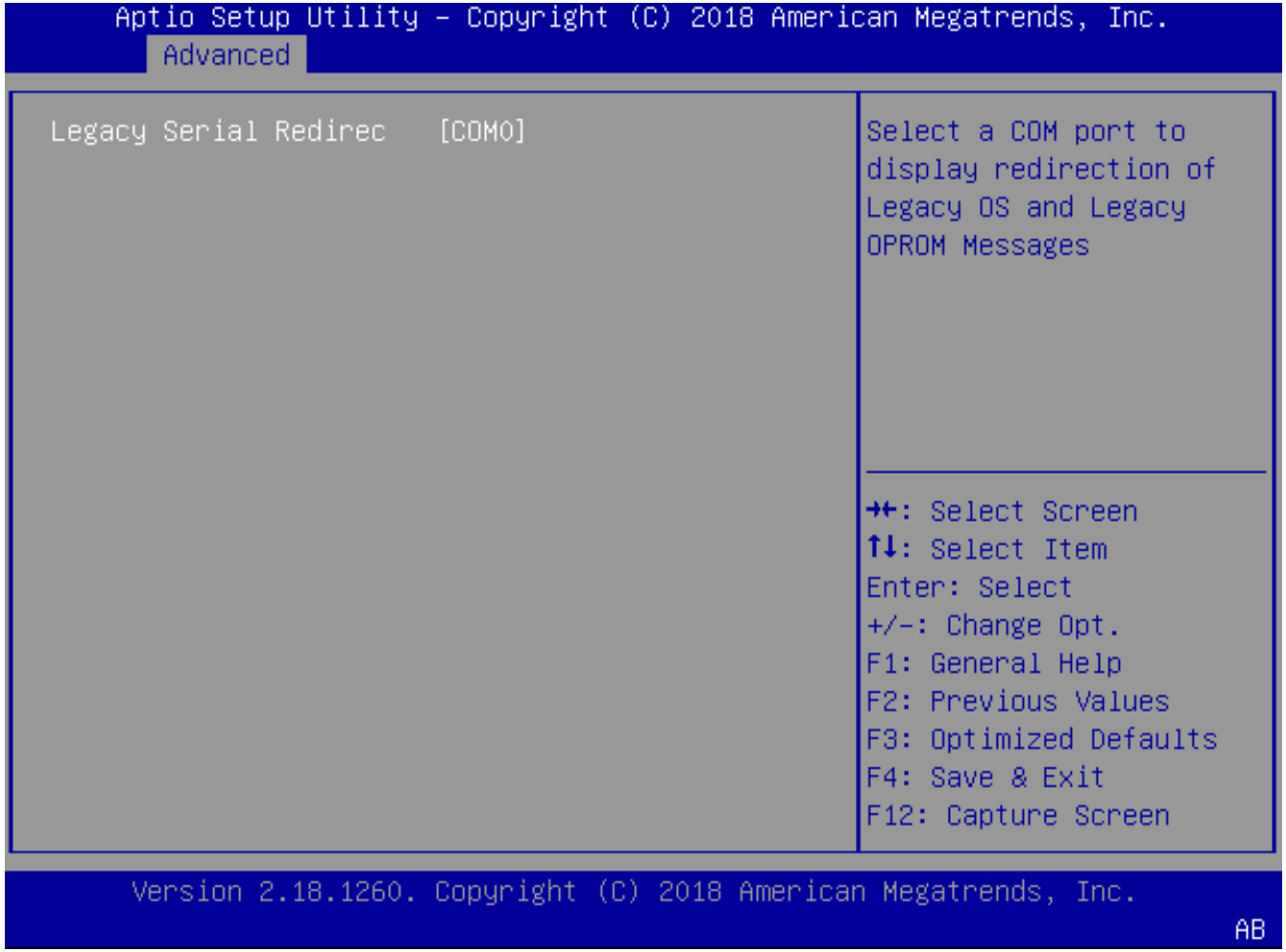
Serial Port Console Redirection



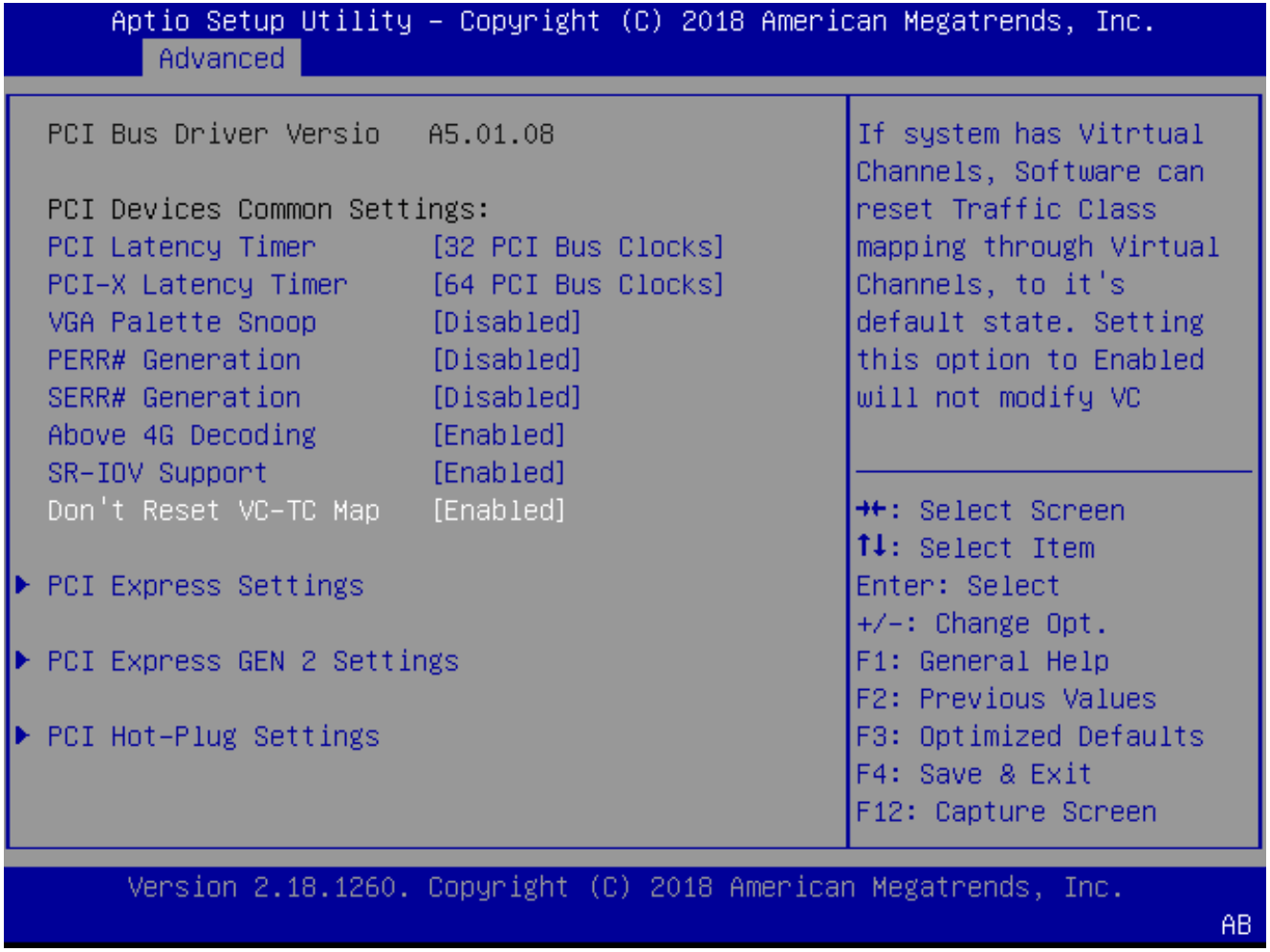
Console Redirection Settings



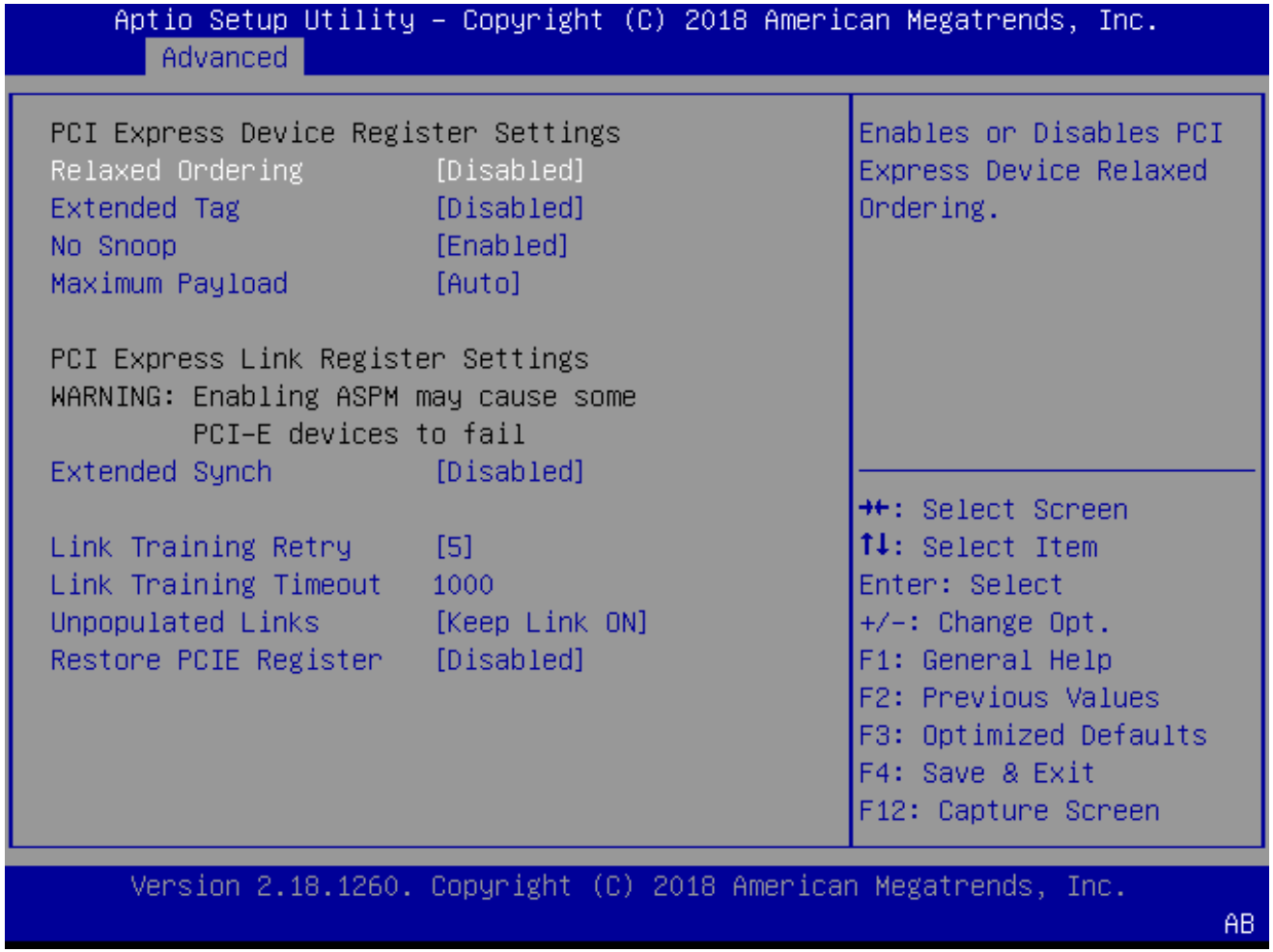
Legacy Console Redirection Settings



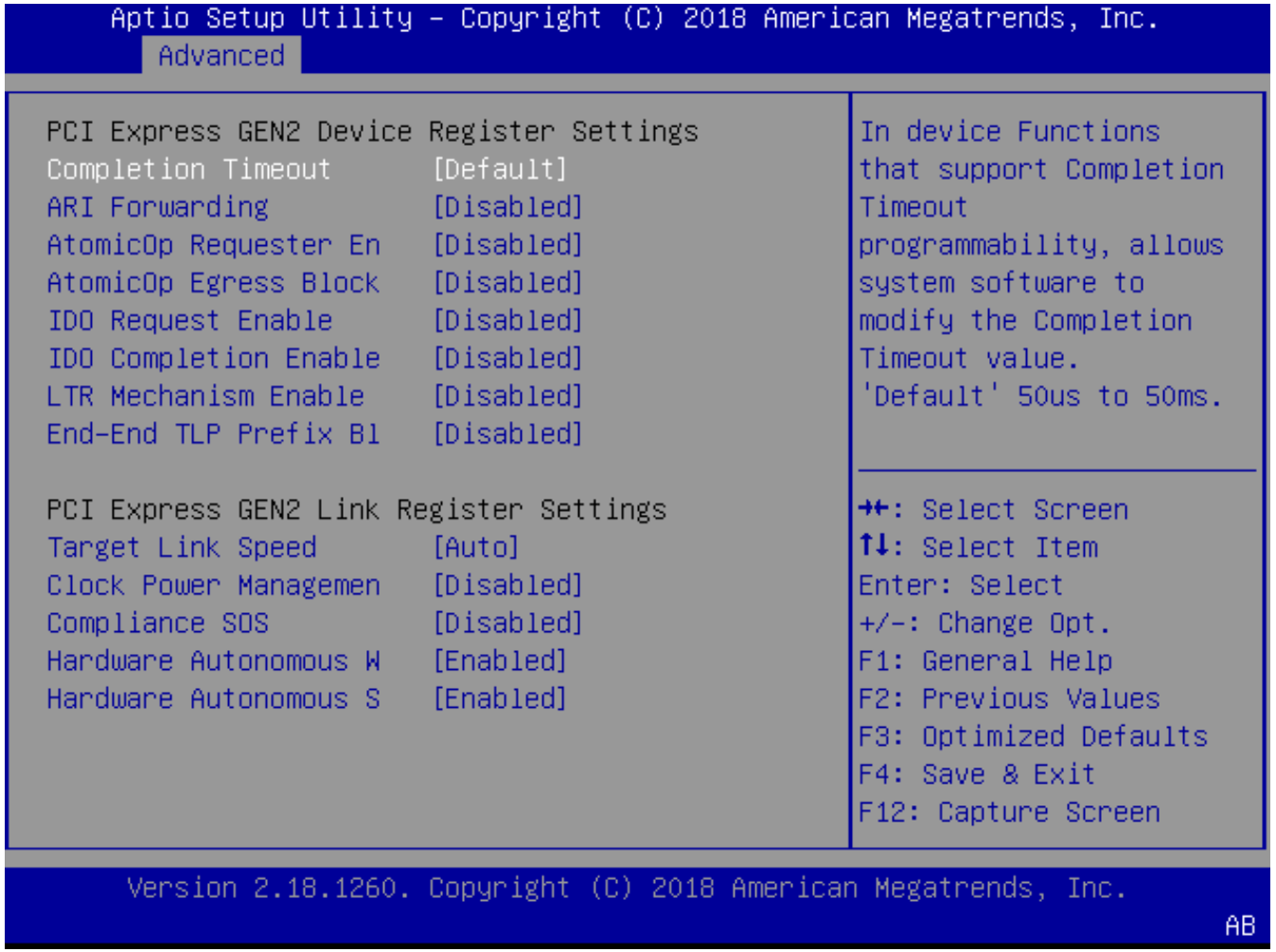
PCI Subsystem Settings



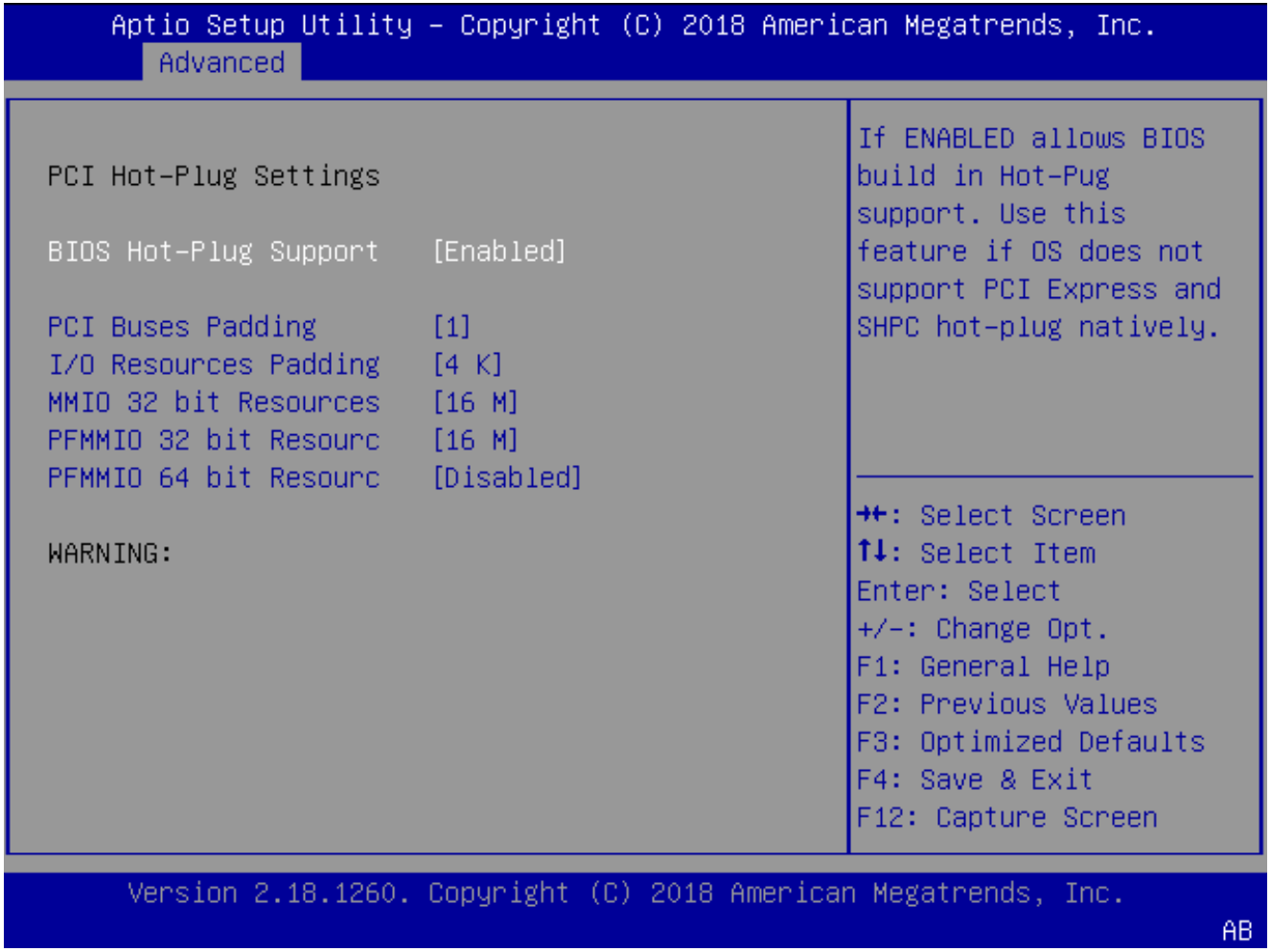
PCI Express Settings



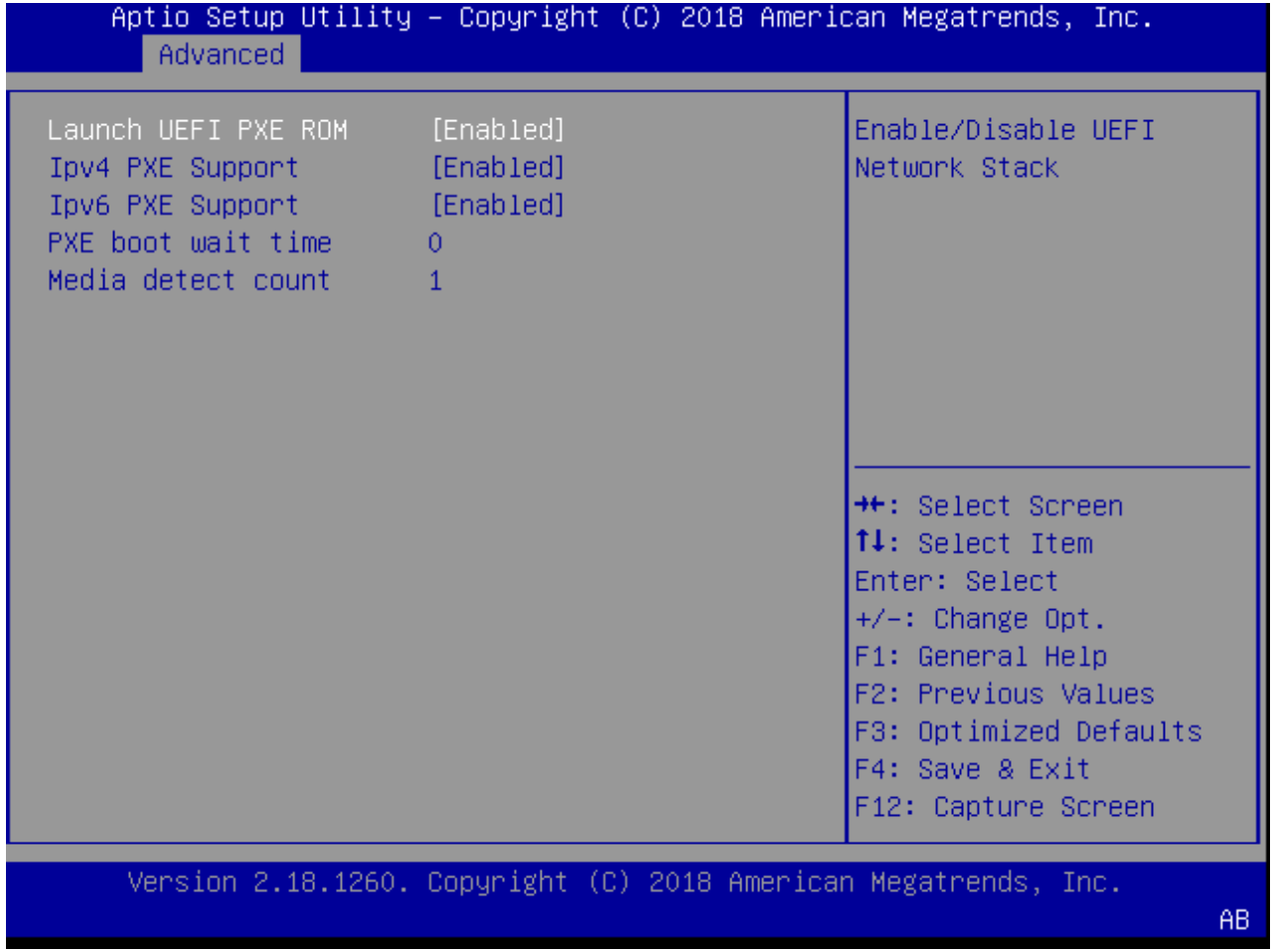
PCI Express GEN 2 Settings



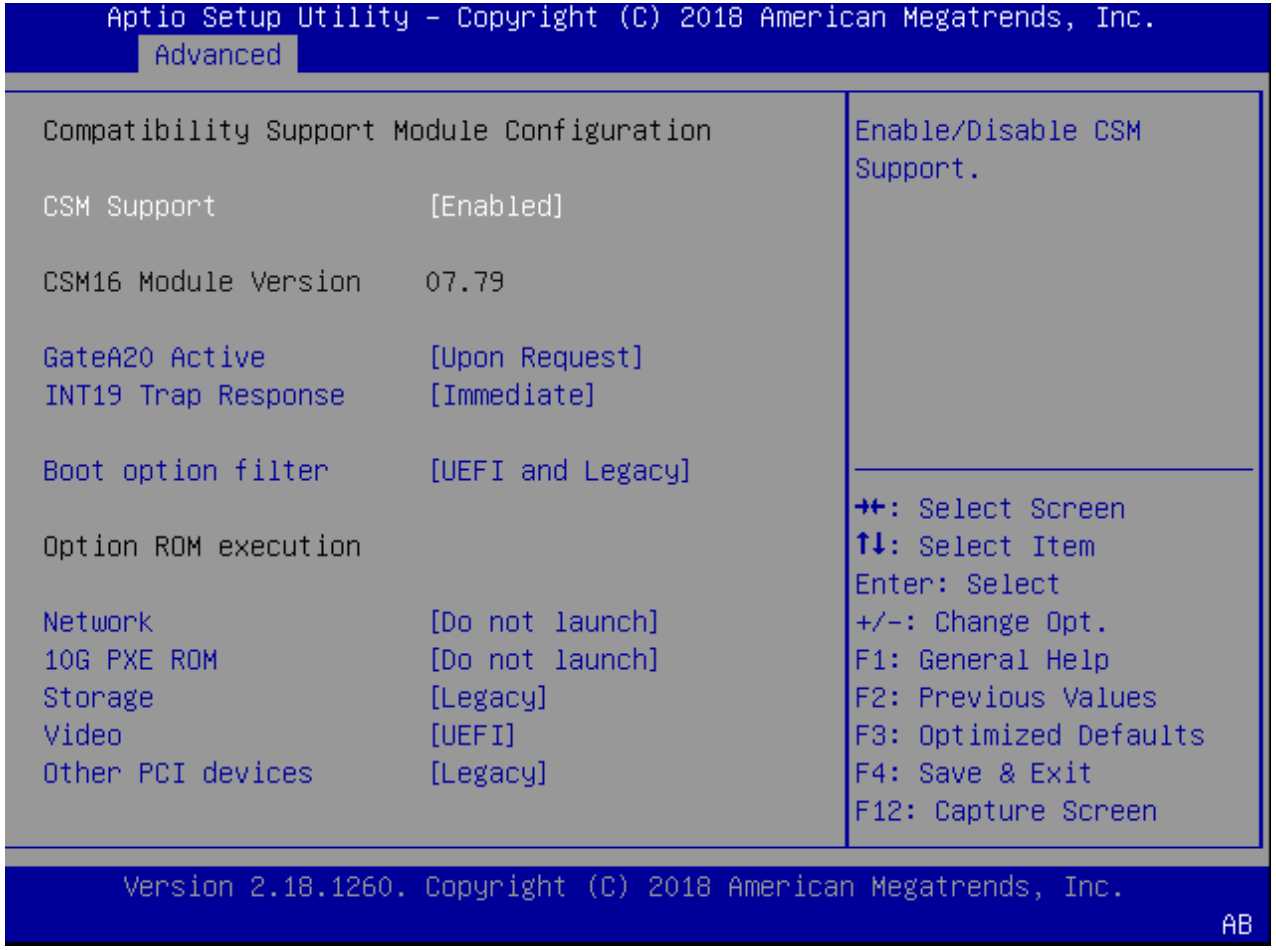
PCI Hot-Plug Settings



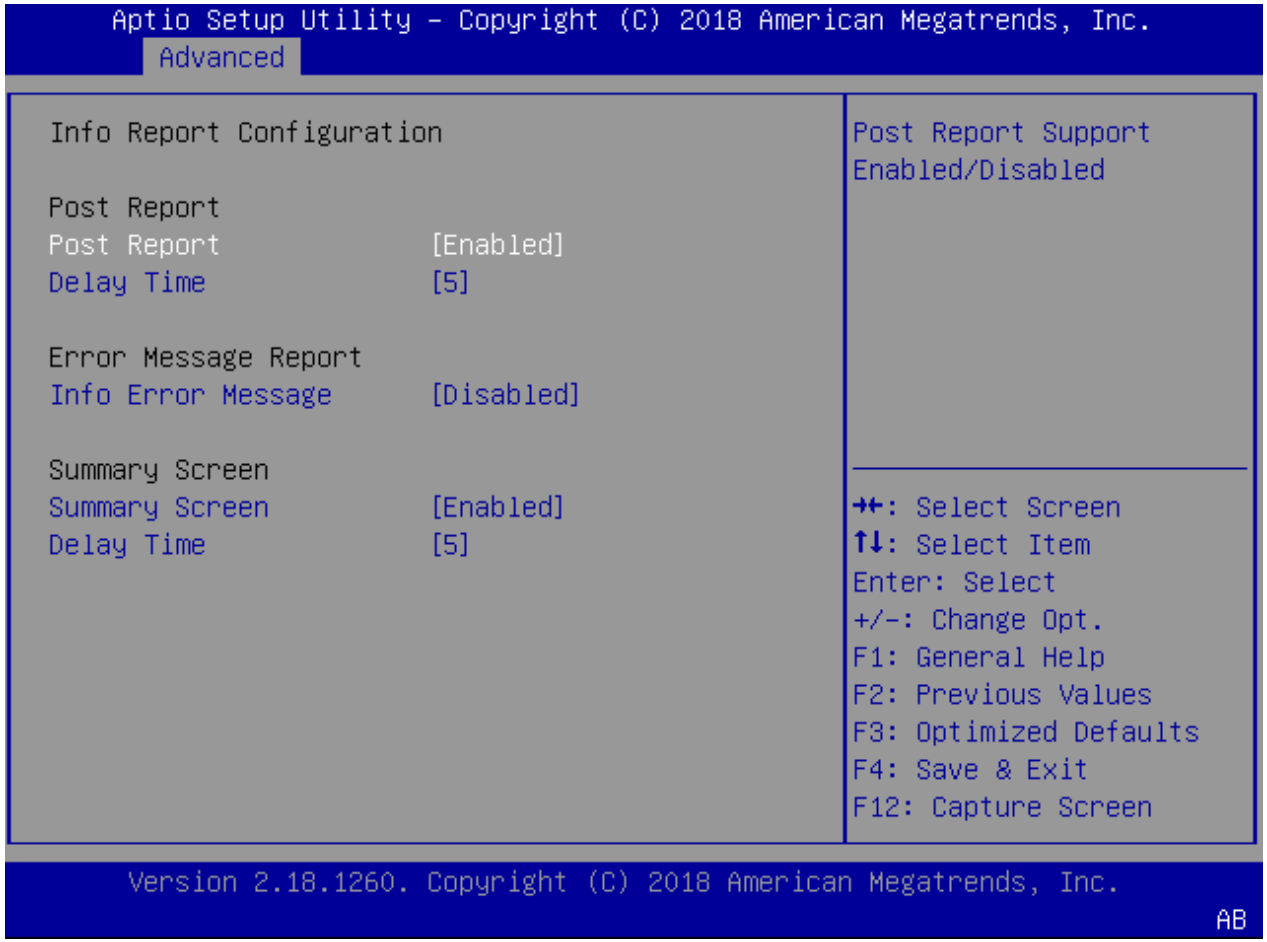
Network Stack Configuration



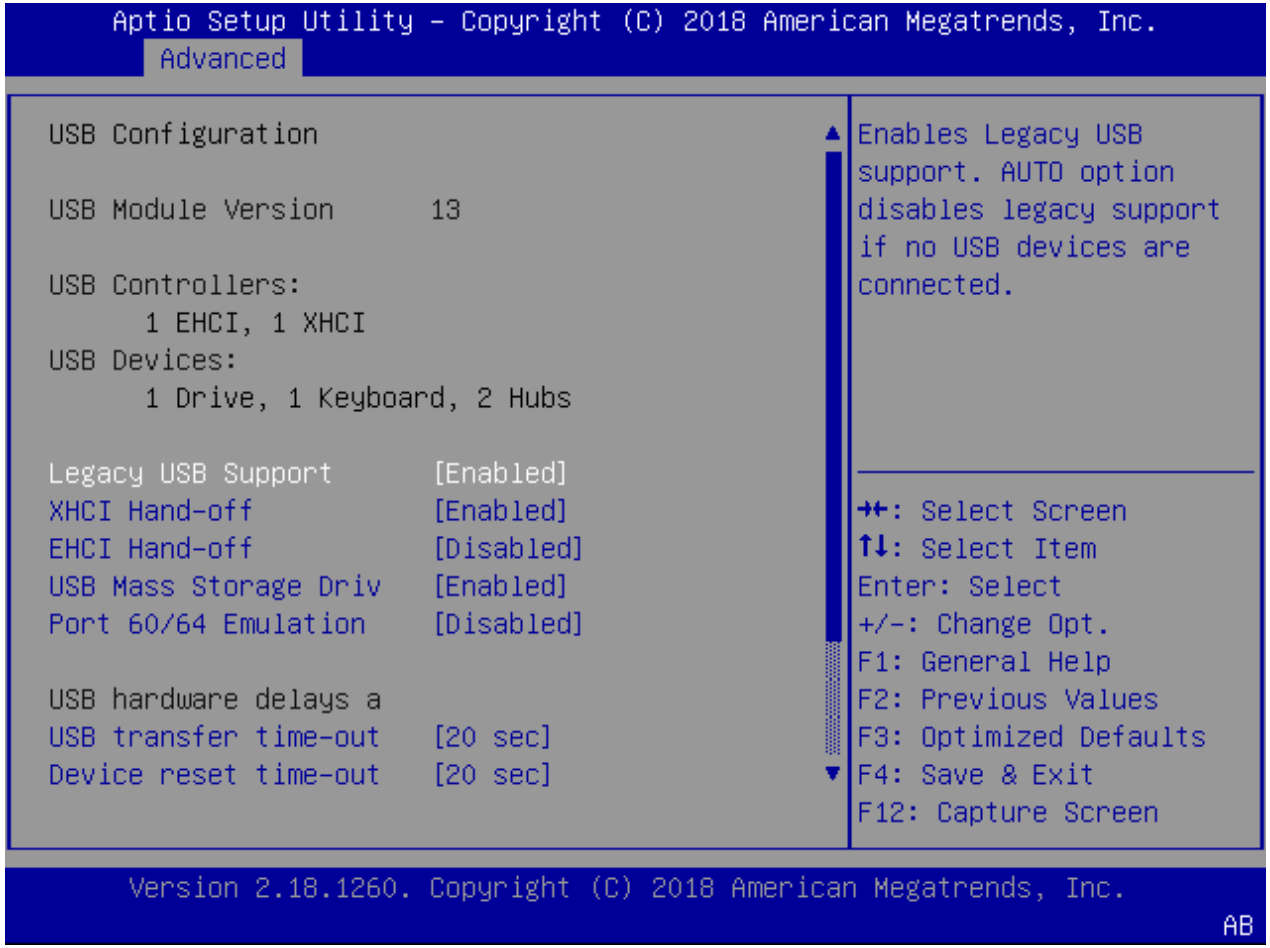
CSM Configuration



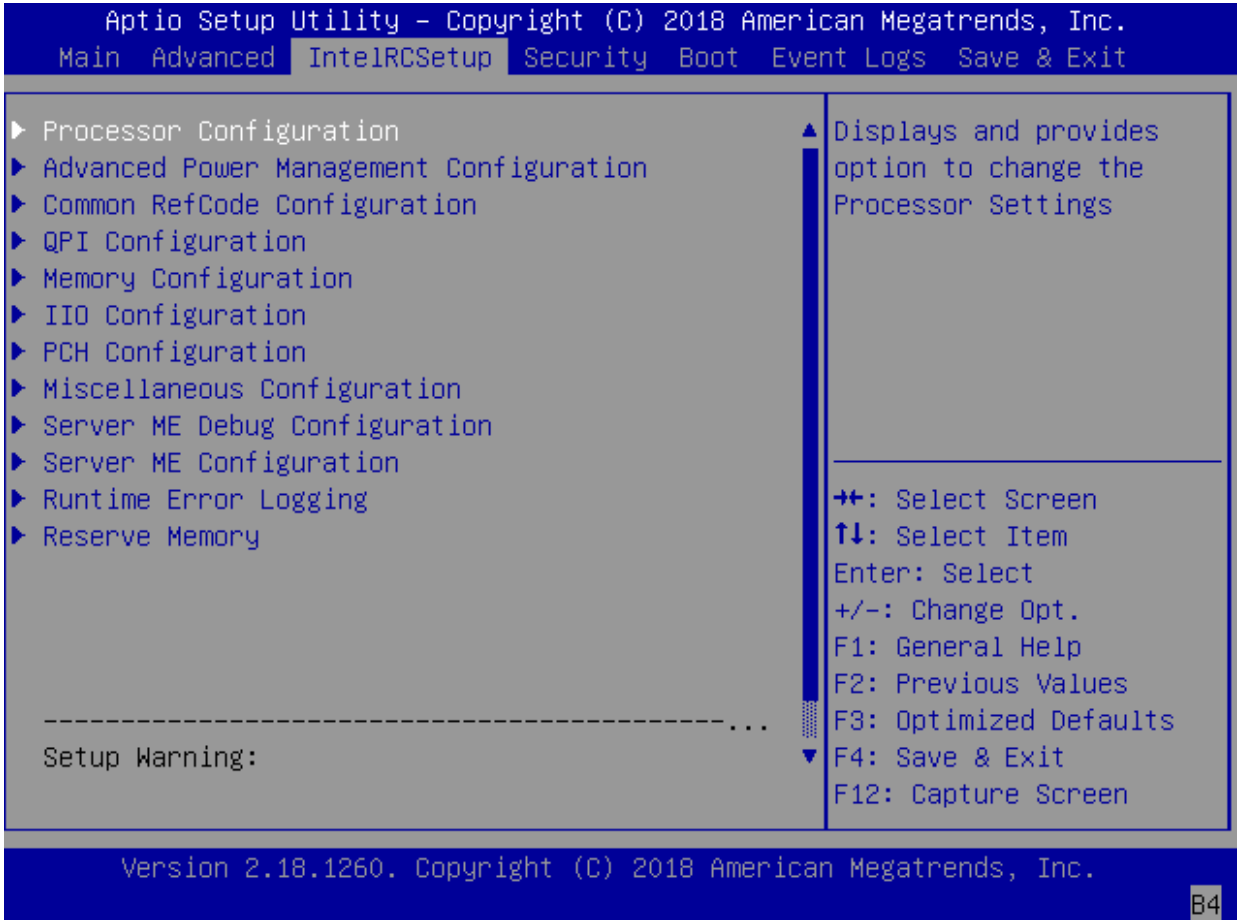
Info Report Configuration



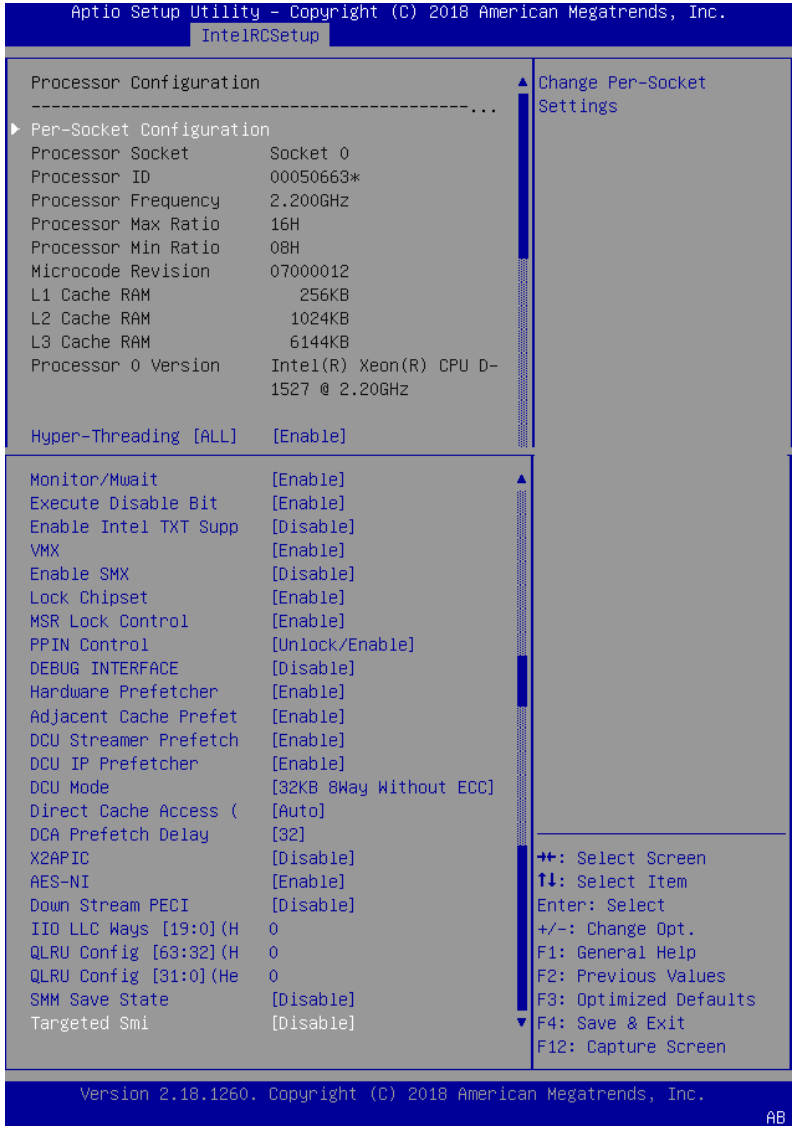
USB Configuration



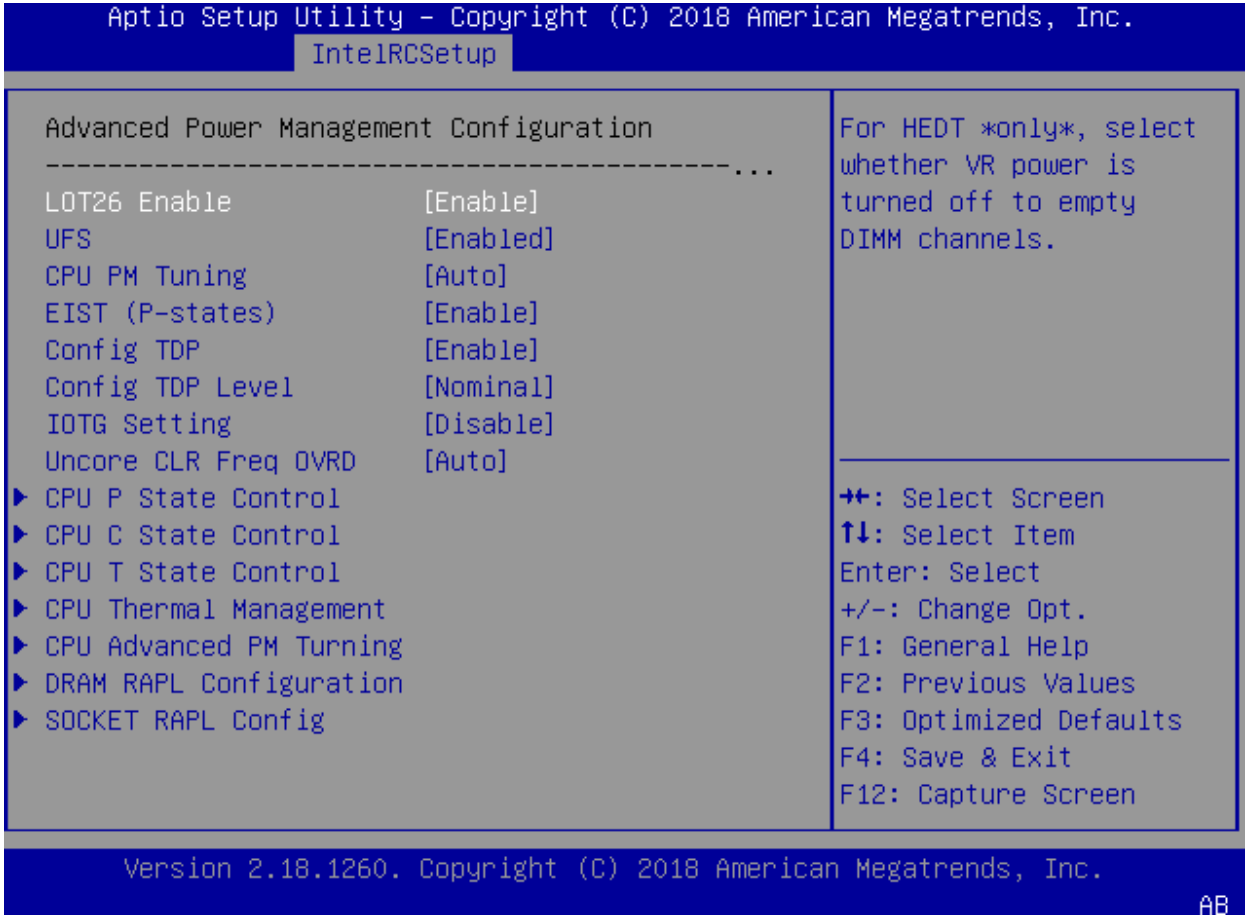
6.4 IntelRCSetup



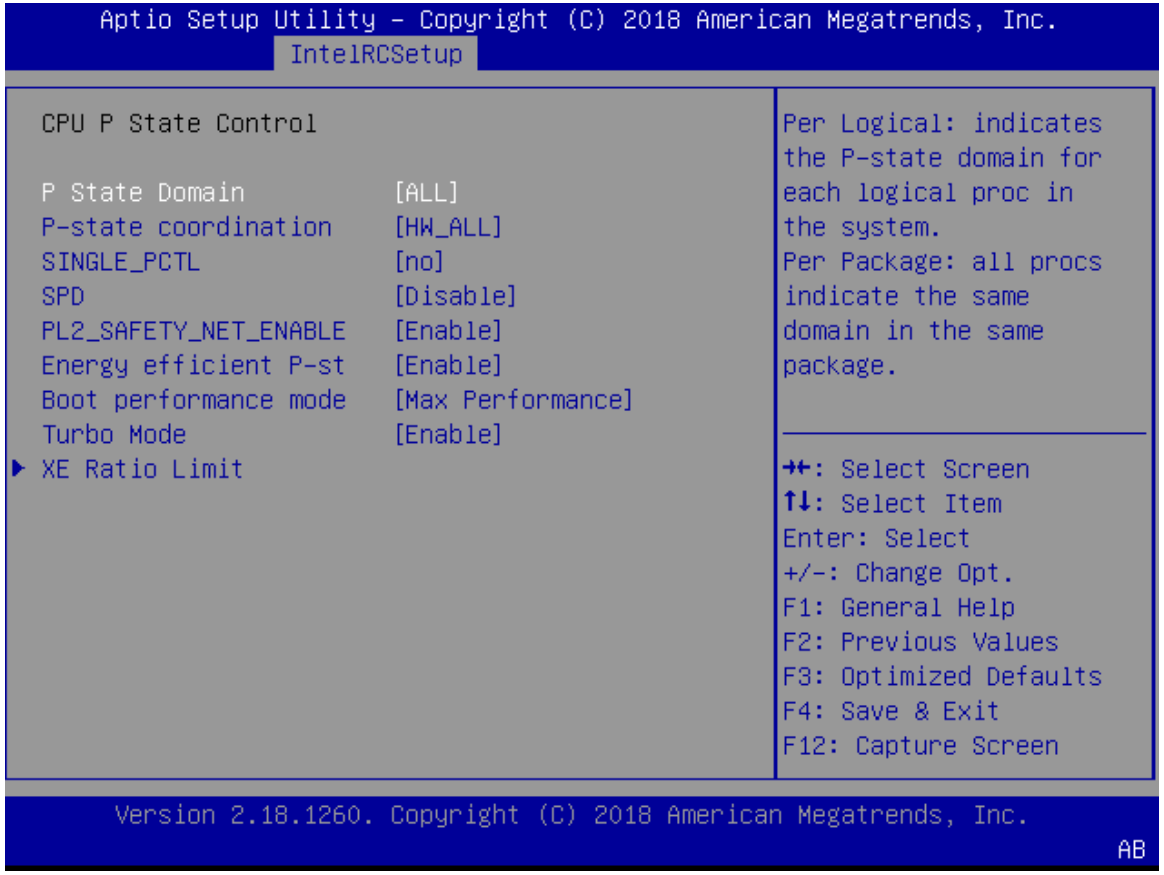
Processor Configuration



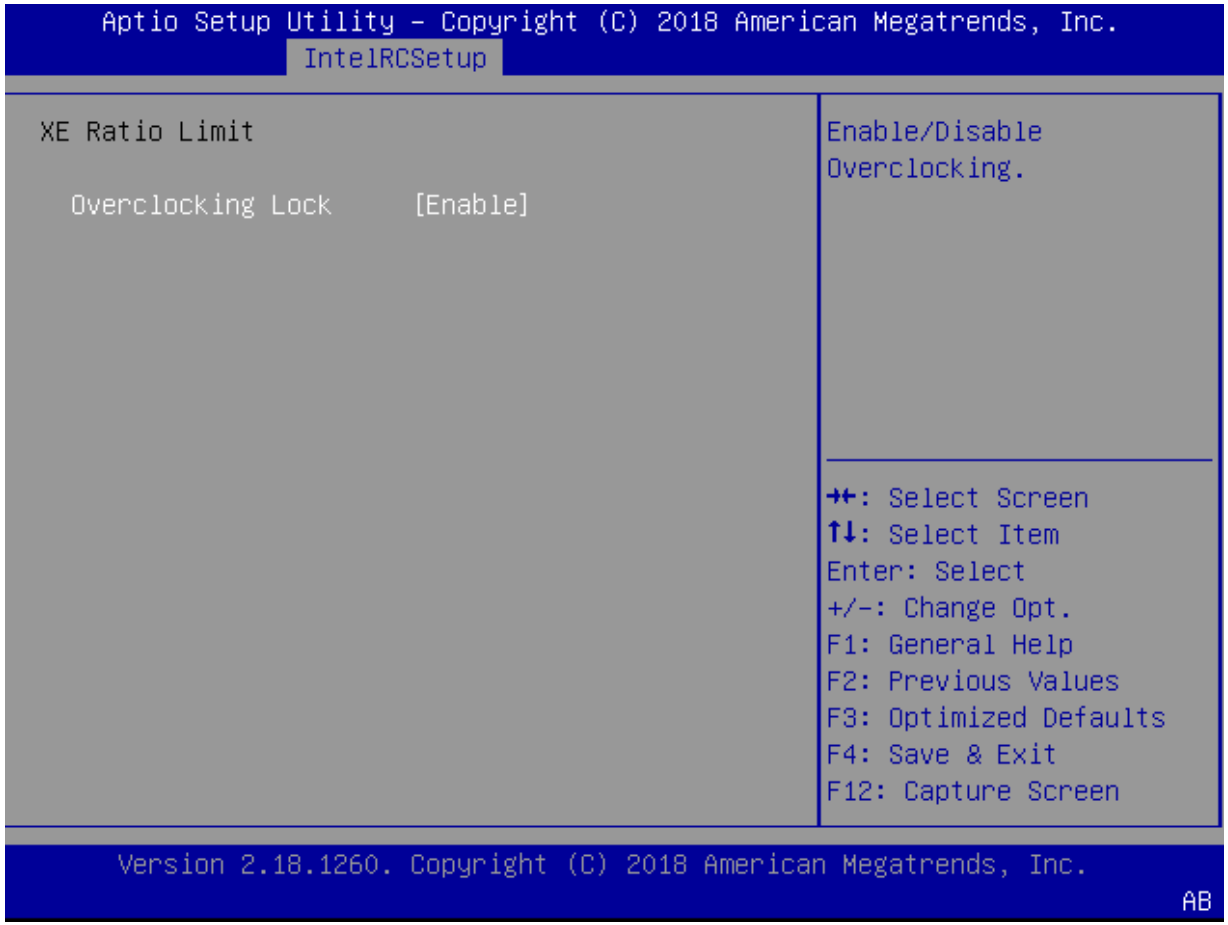
Advanced Power Management Configuration



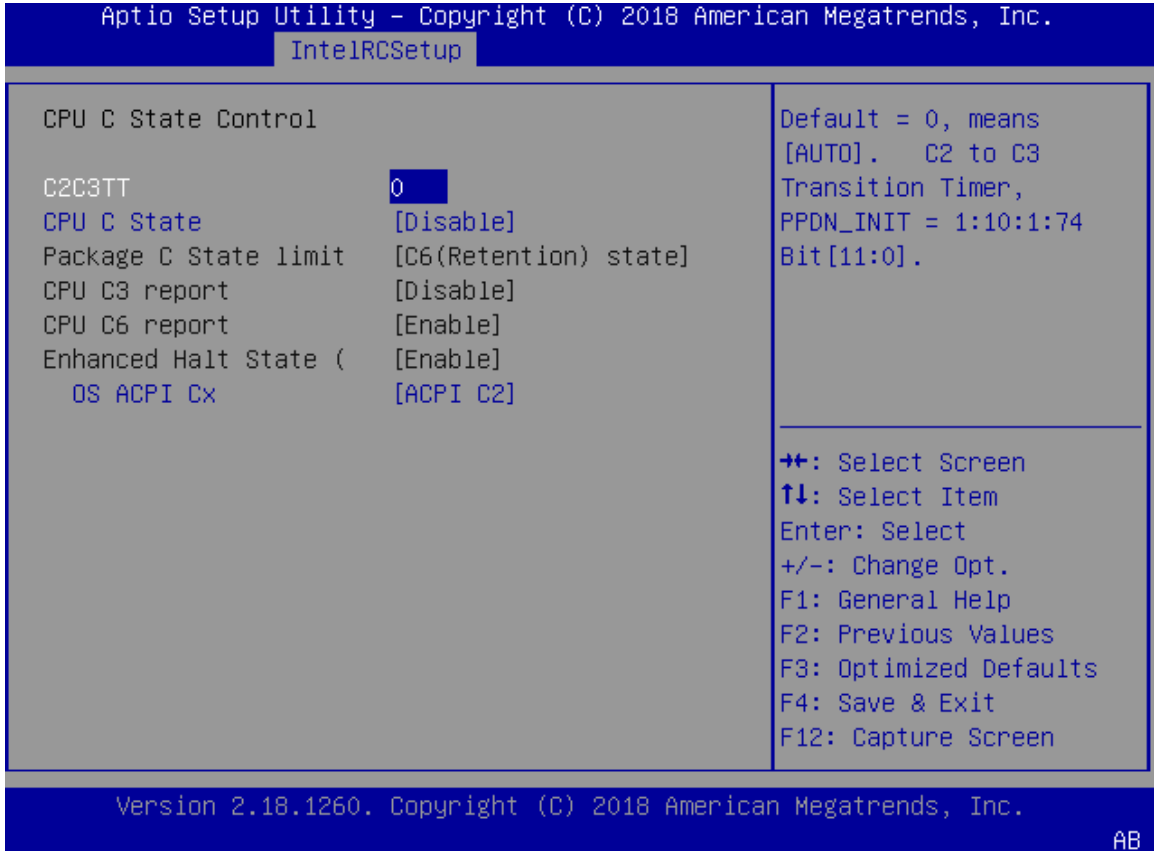
CPU P State Control



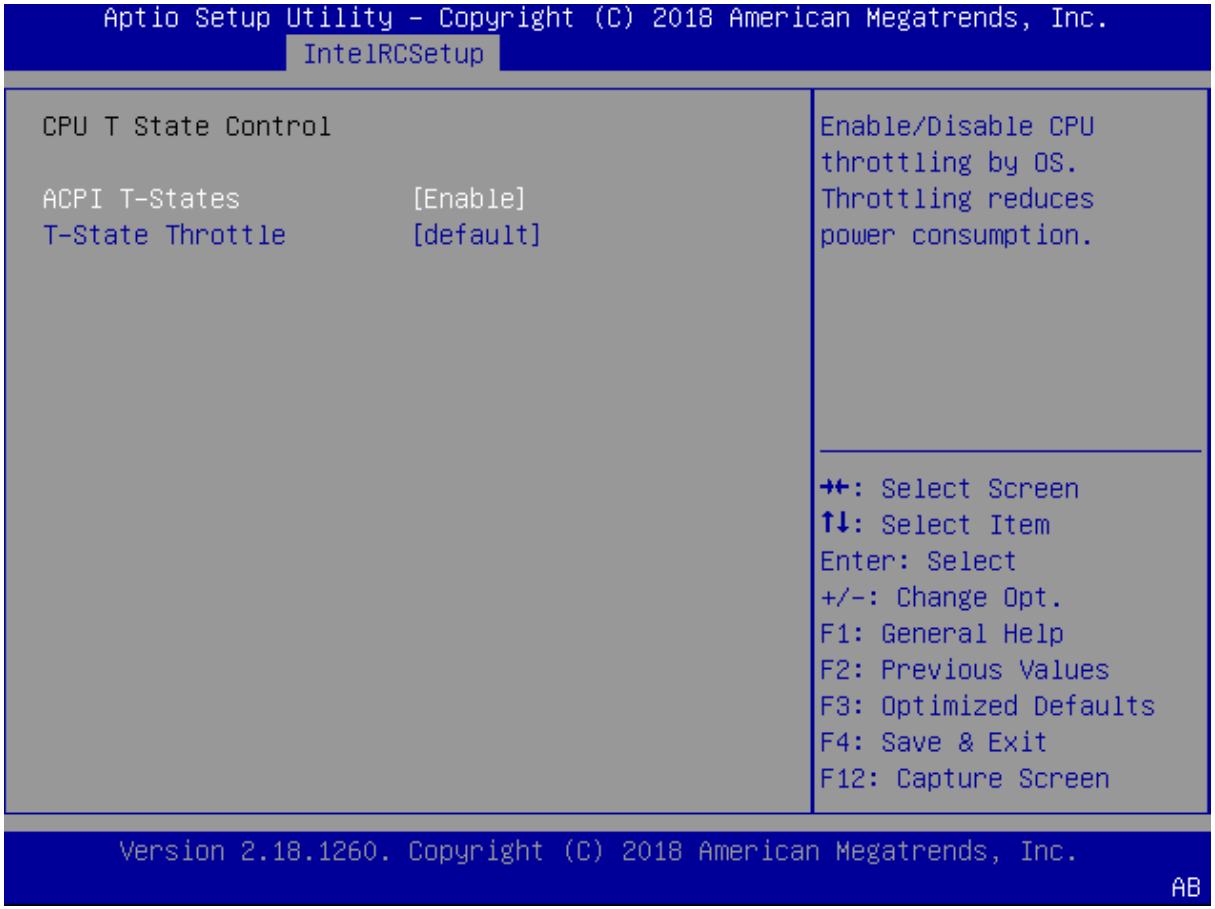
XE Ratio Limit



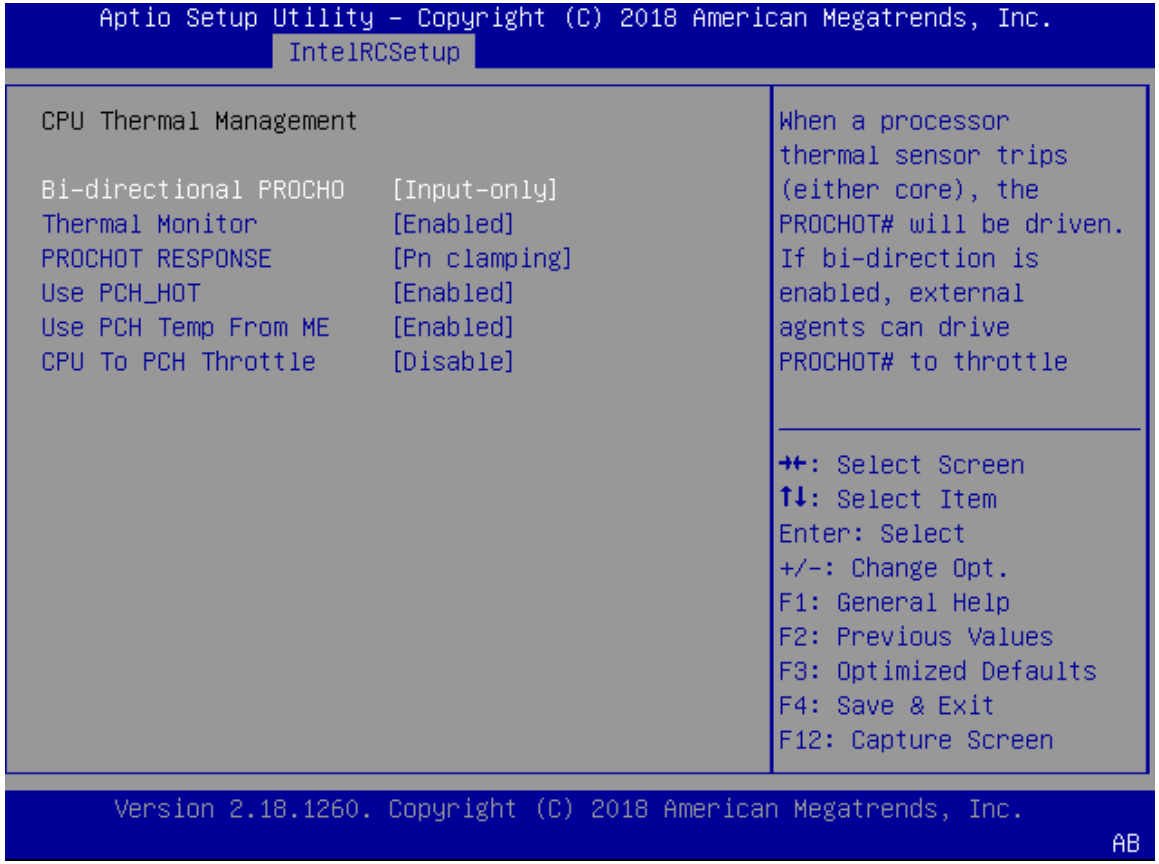
CPU C State Control



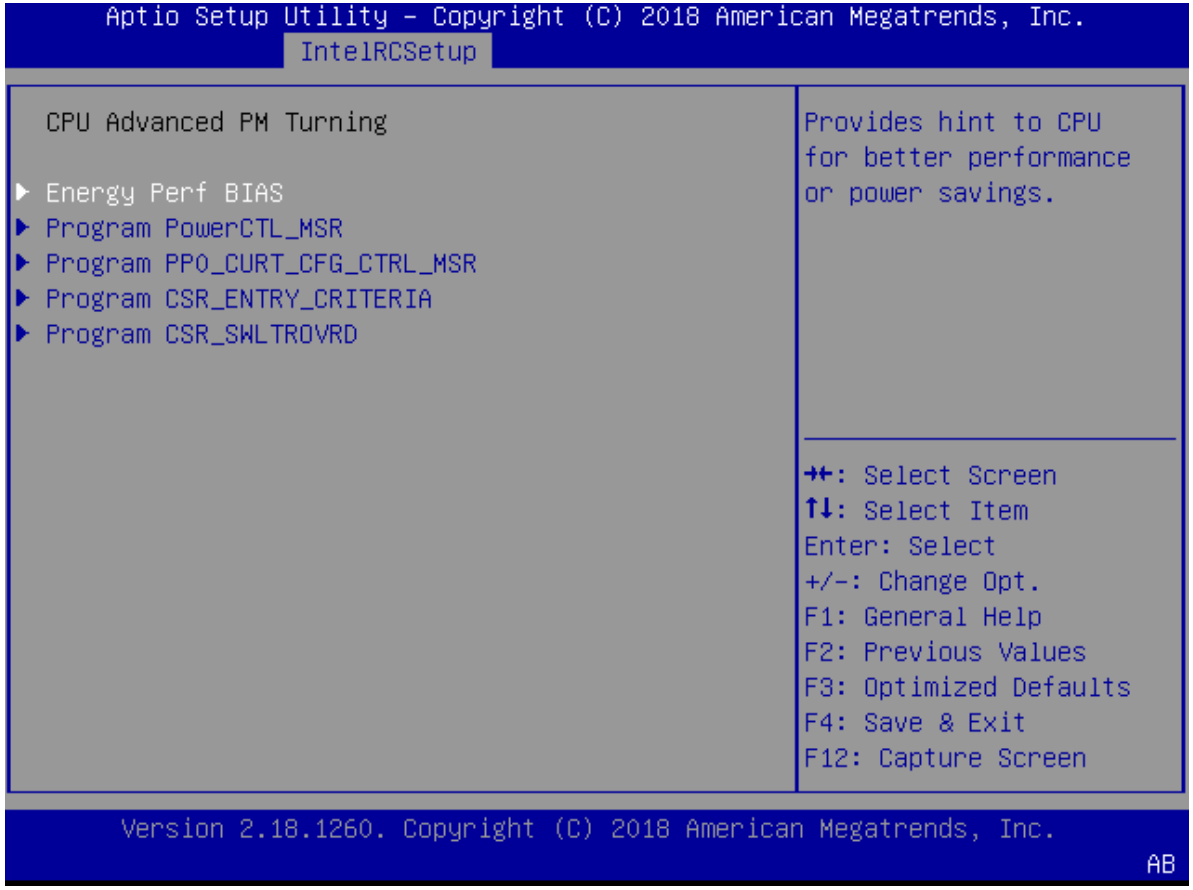
CPU T State Control



CPU Thermal Management

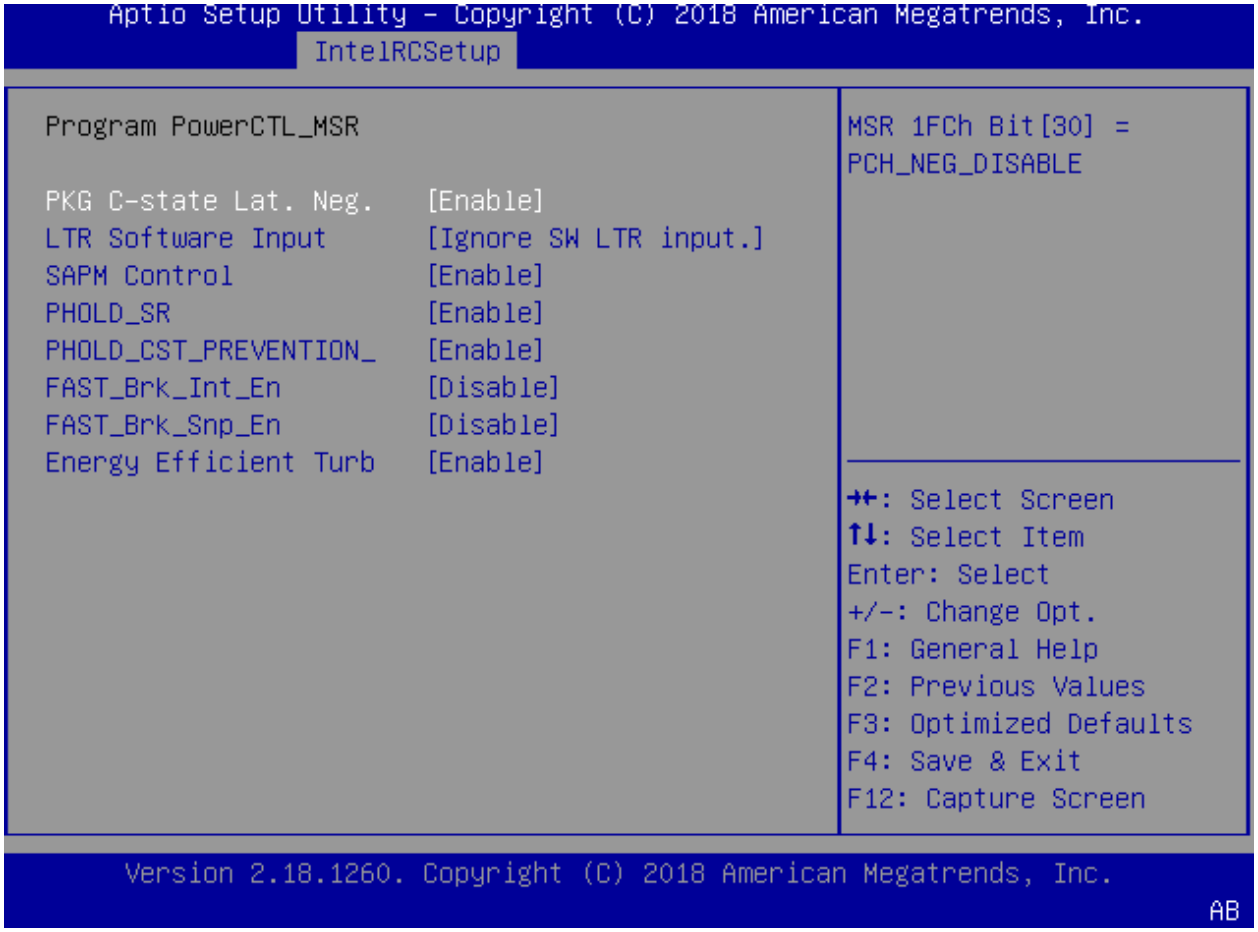


CPU Advanced PM Turning

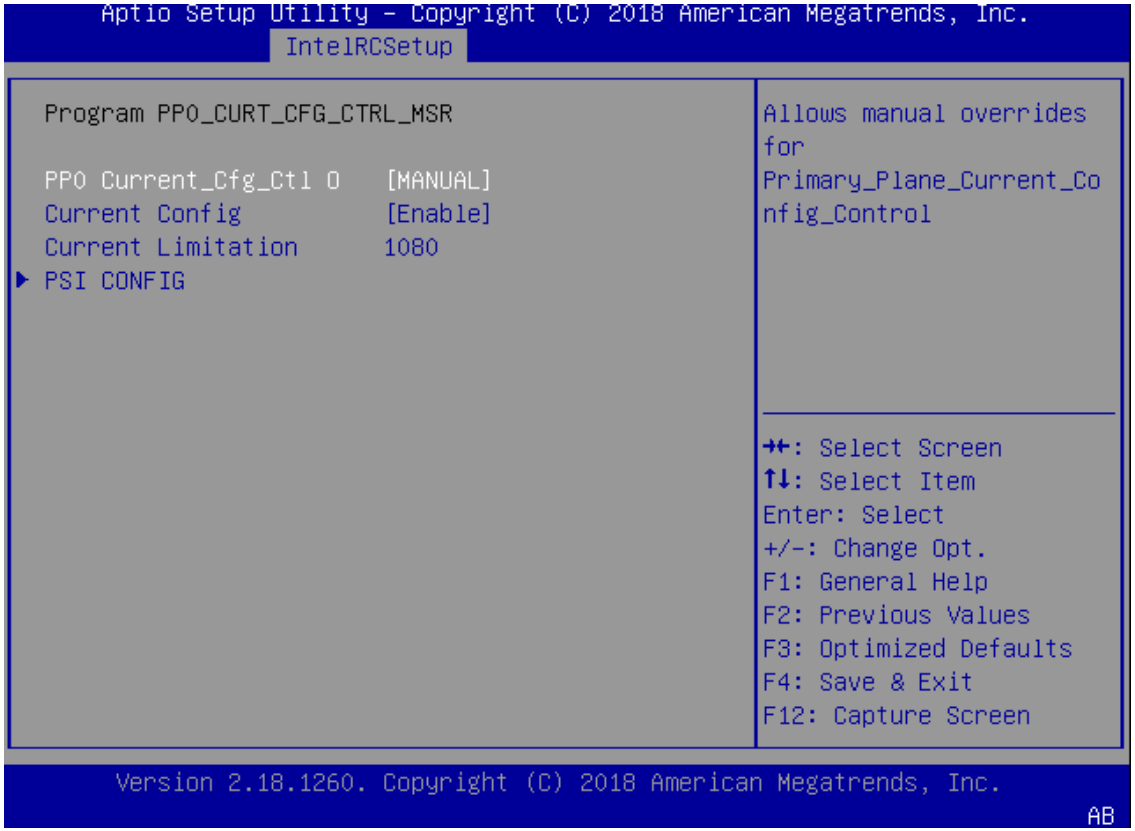


Energy Perf BIAS

Program PowerCTL_MSR



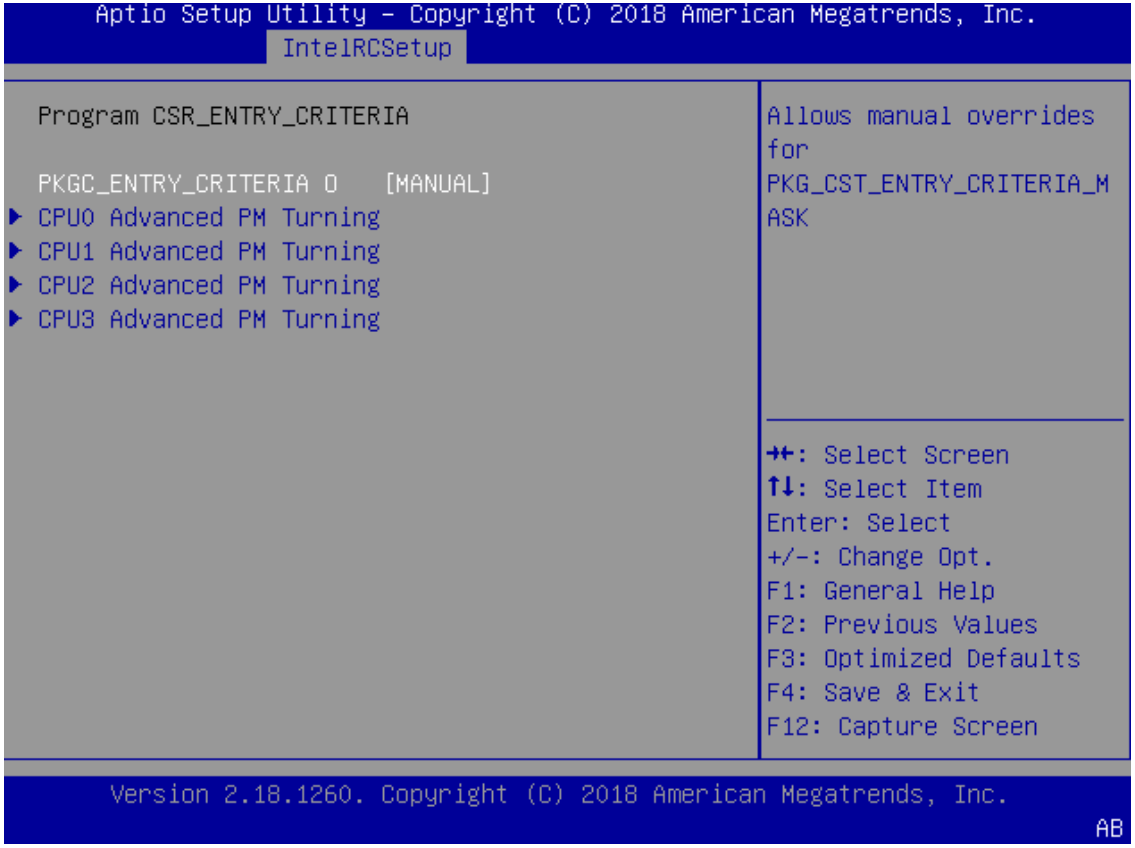
Program PPO_CURT_CFG_CTRL_MSR



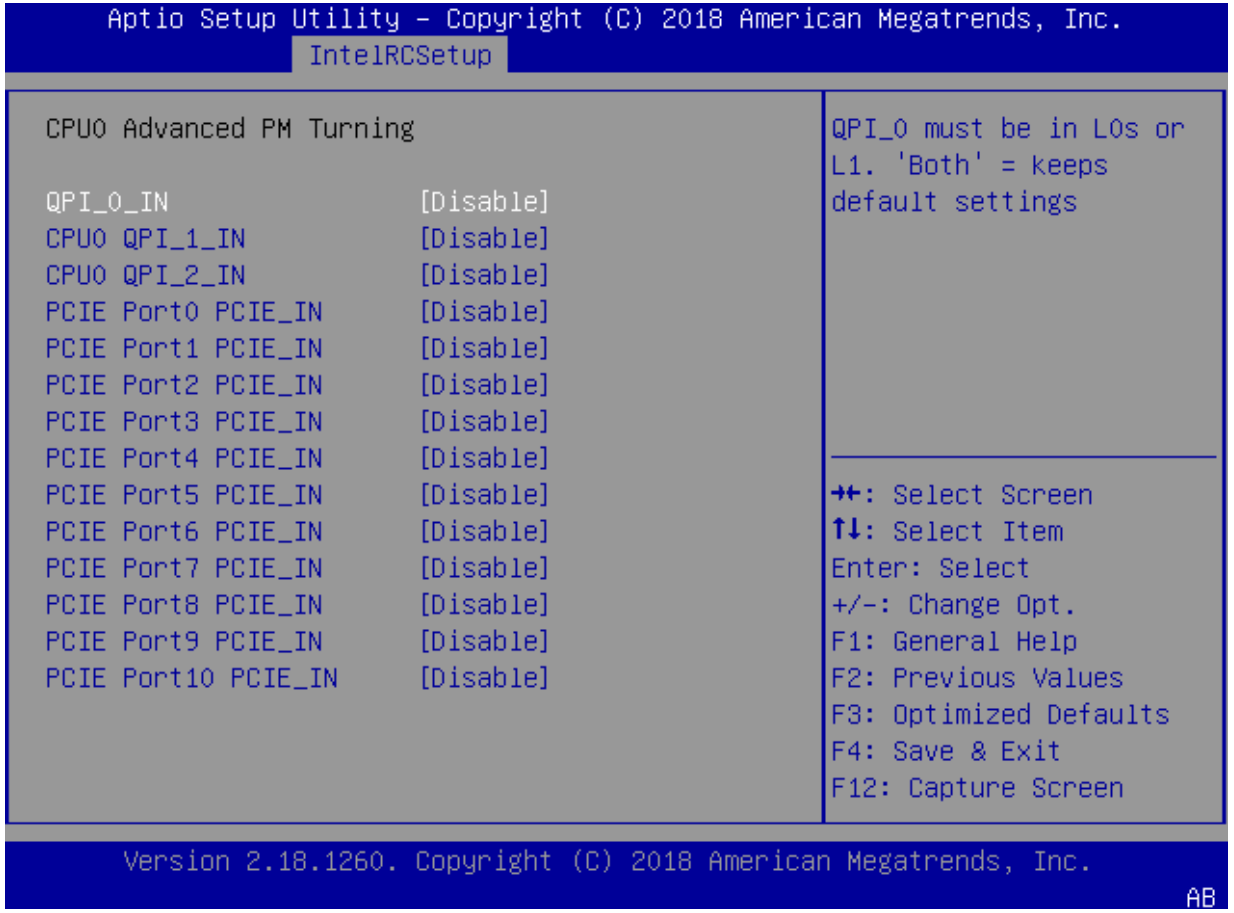
PSI CONFIG


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
IntelRCSetup
PSI CONFIG
PSI3 Threshold 1
PSI2 Threshold 5
PSI1 Threshold 20
Lock Indication [Disable]
PSI3 Threshold
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.
AB

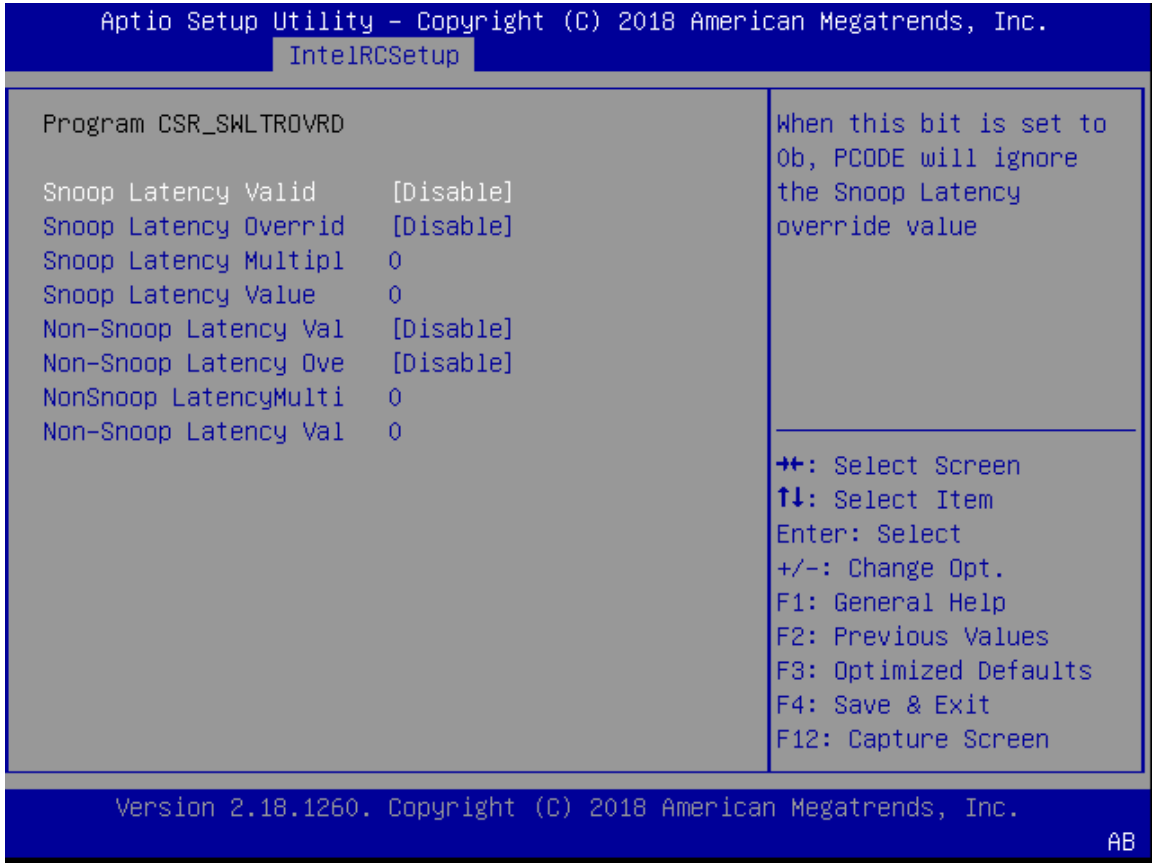
Program CSR_ENTRY_CRITERIA



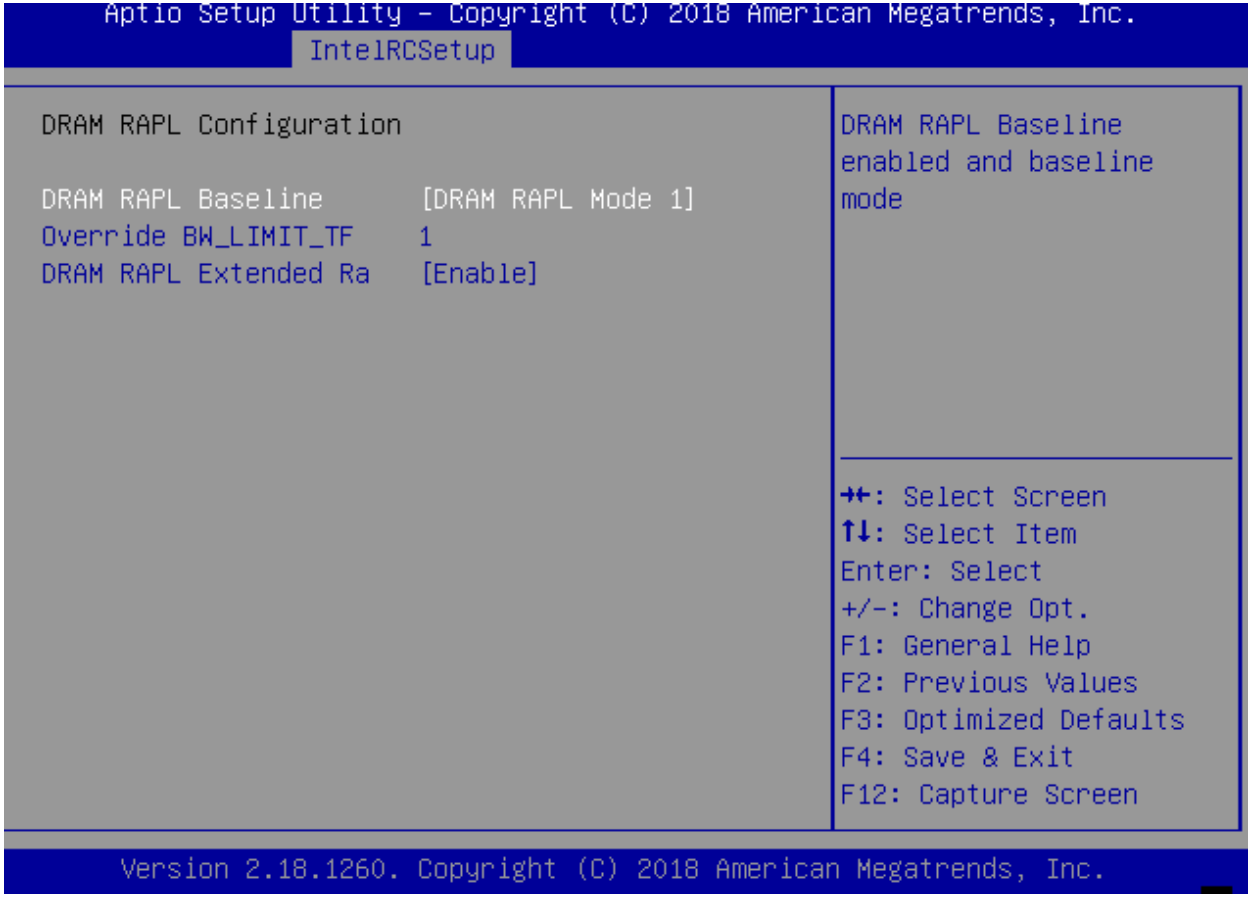
CPU(0~3) Advanced PM Turning



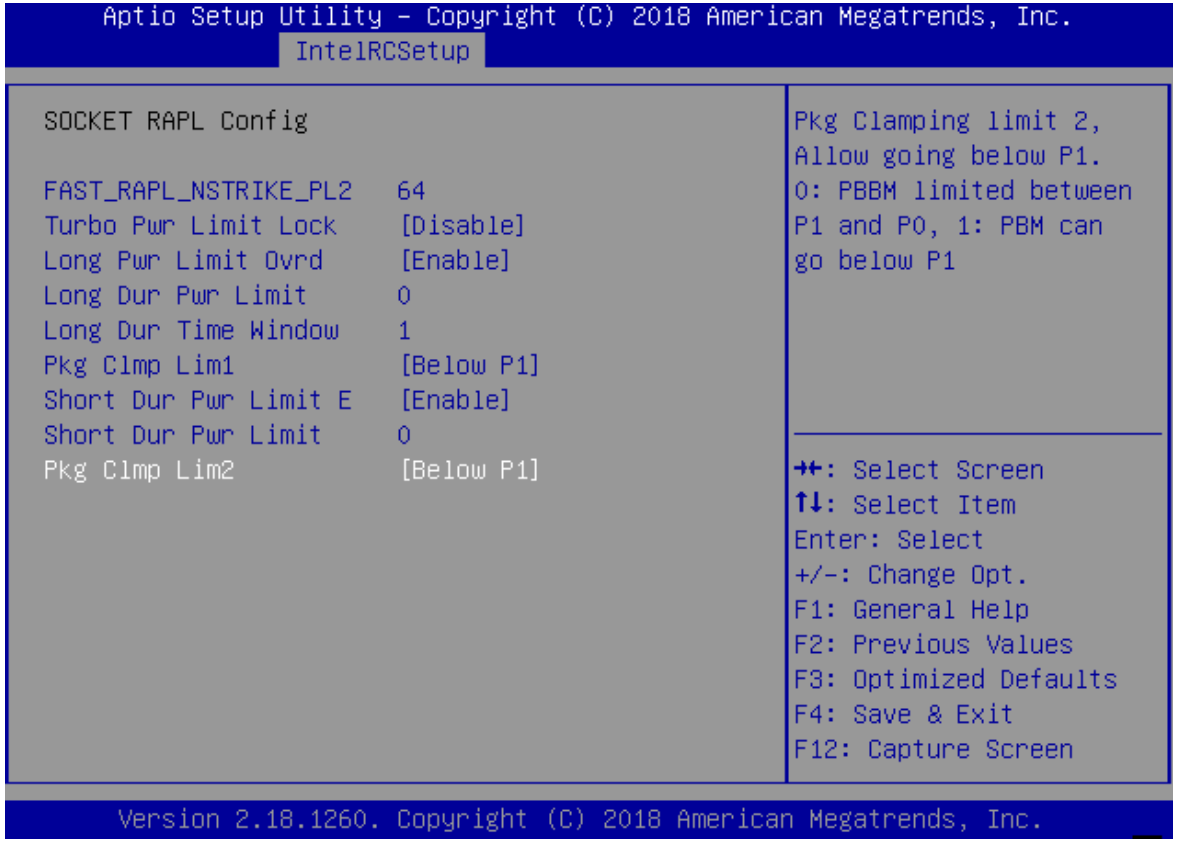
Program CSR_SWL TROVRD



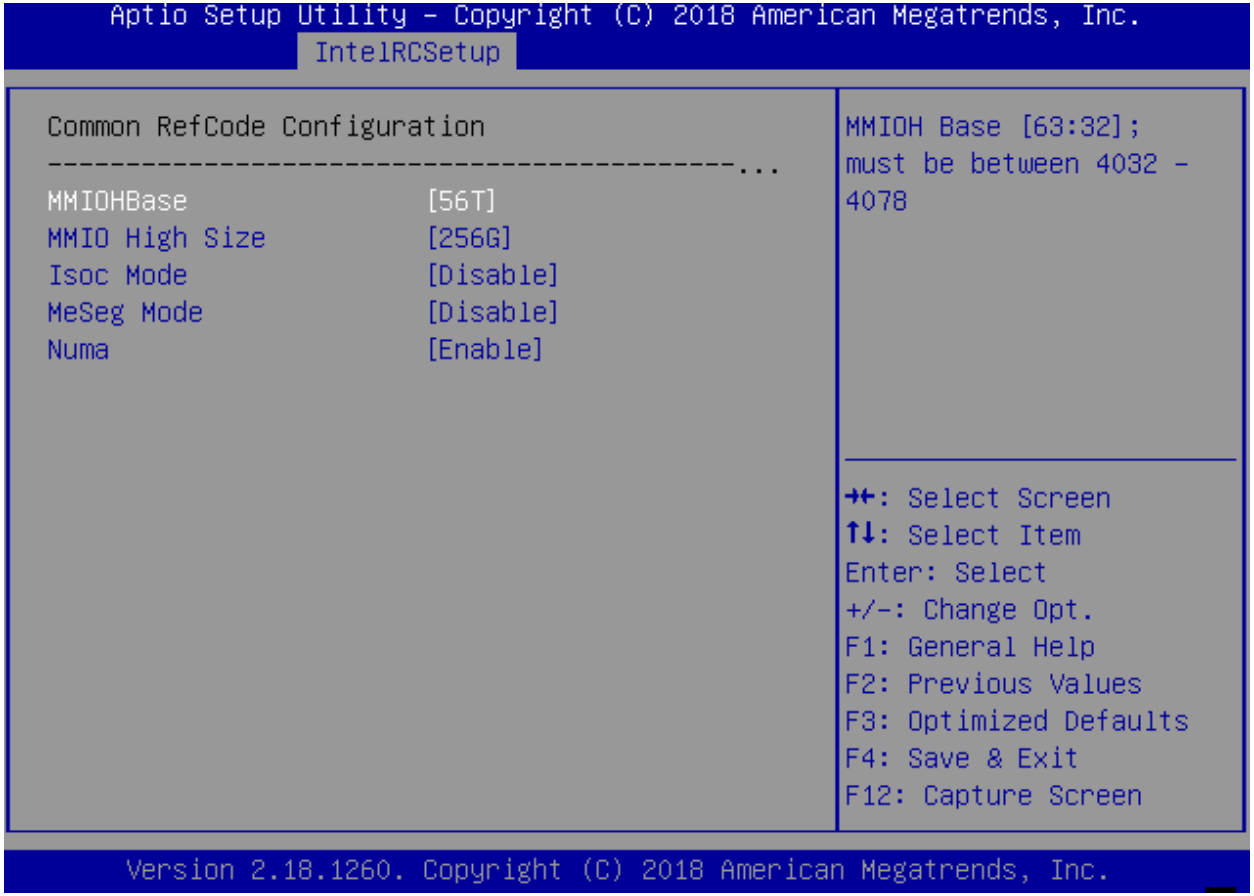
DRAM RAPL Configuration



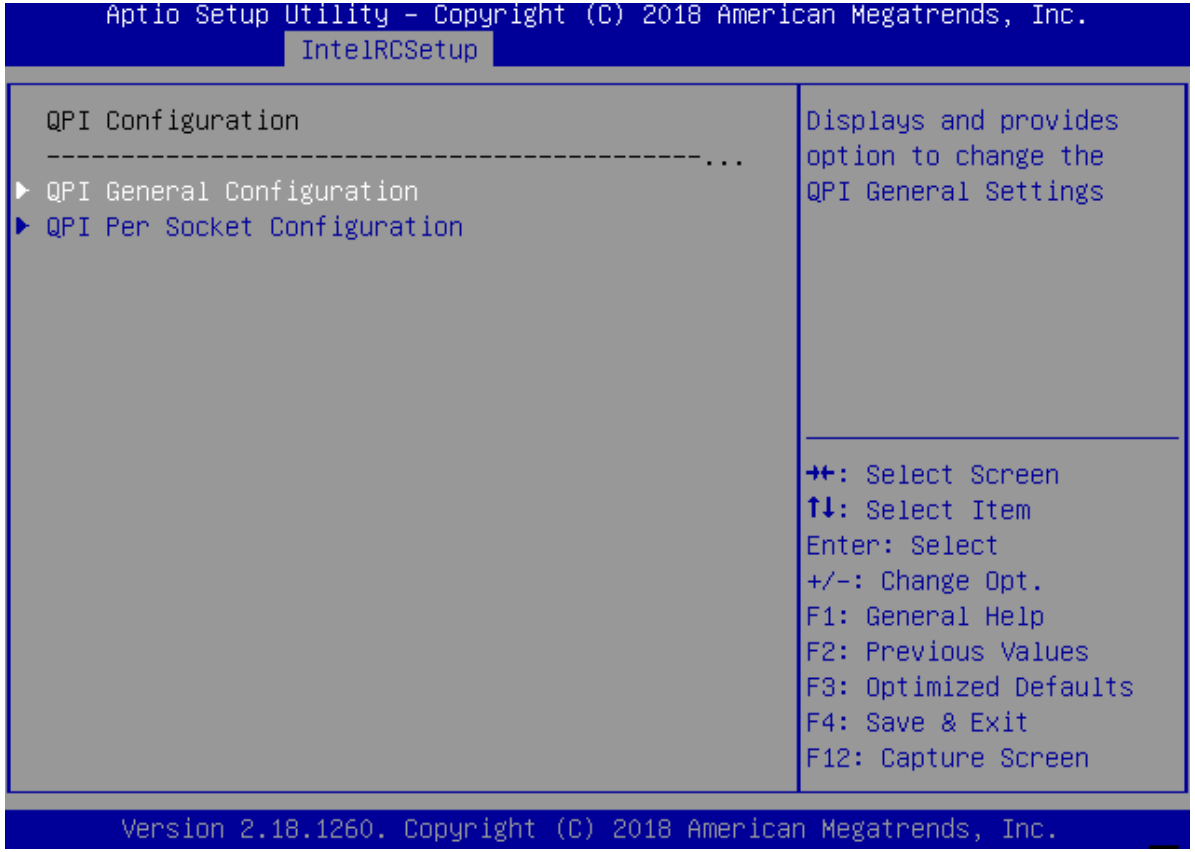
SOCKET RAPL Config



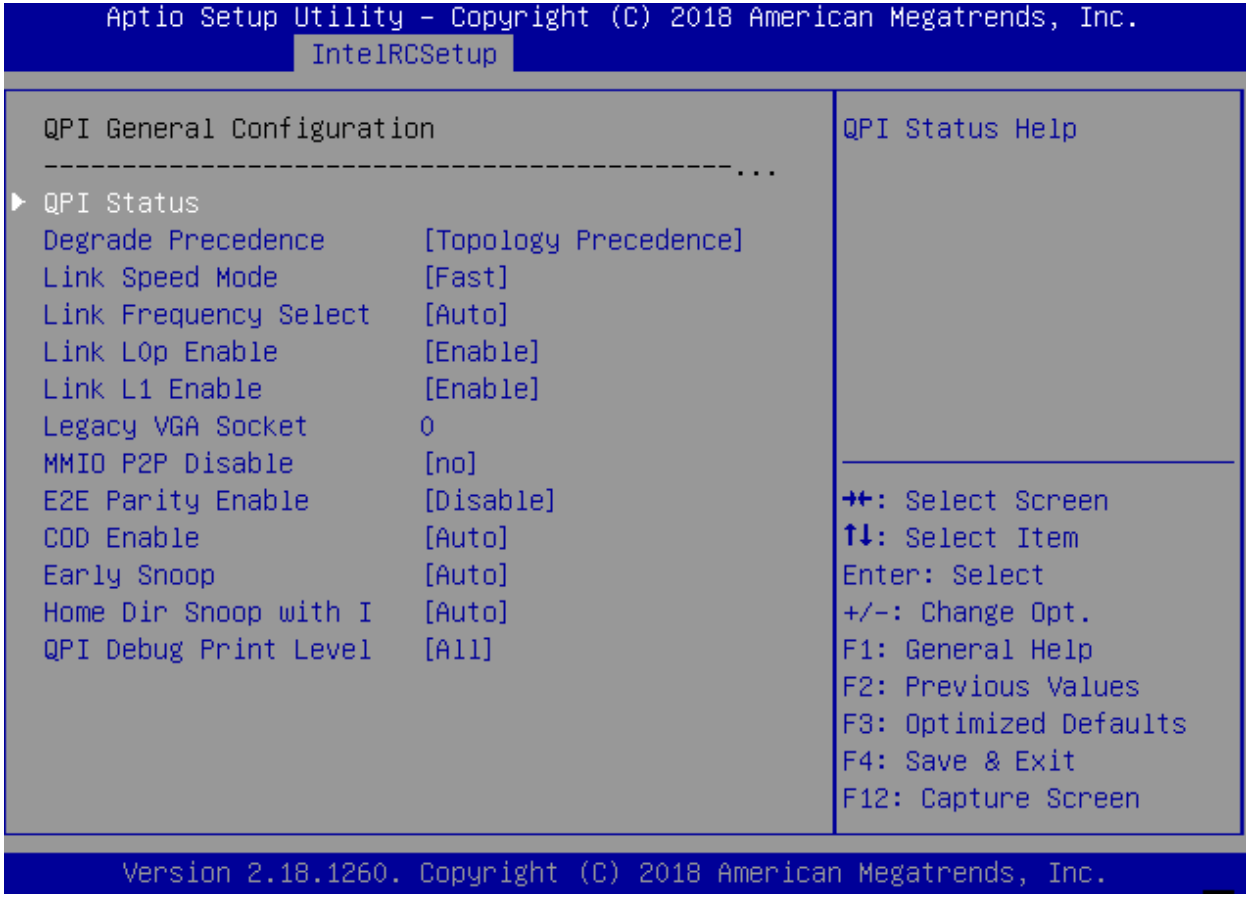
Common Refcode Configuration



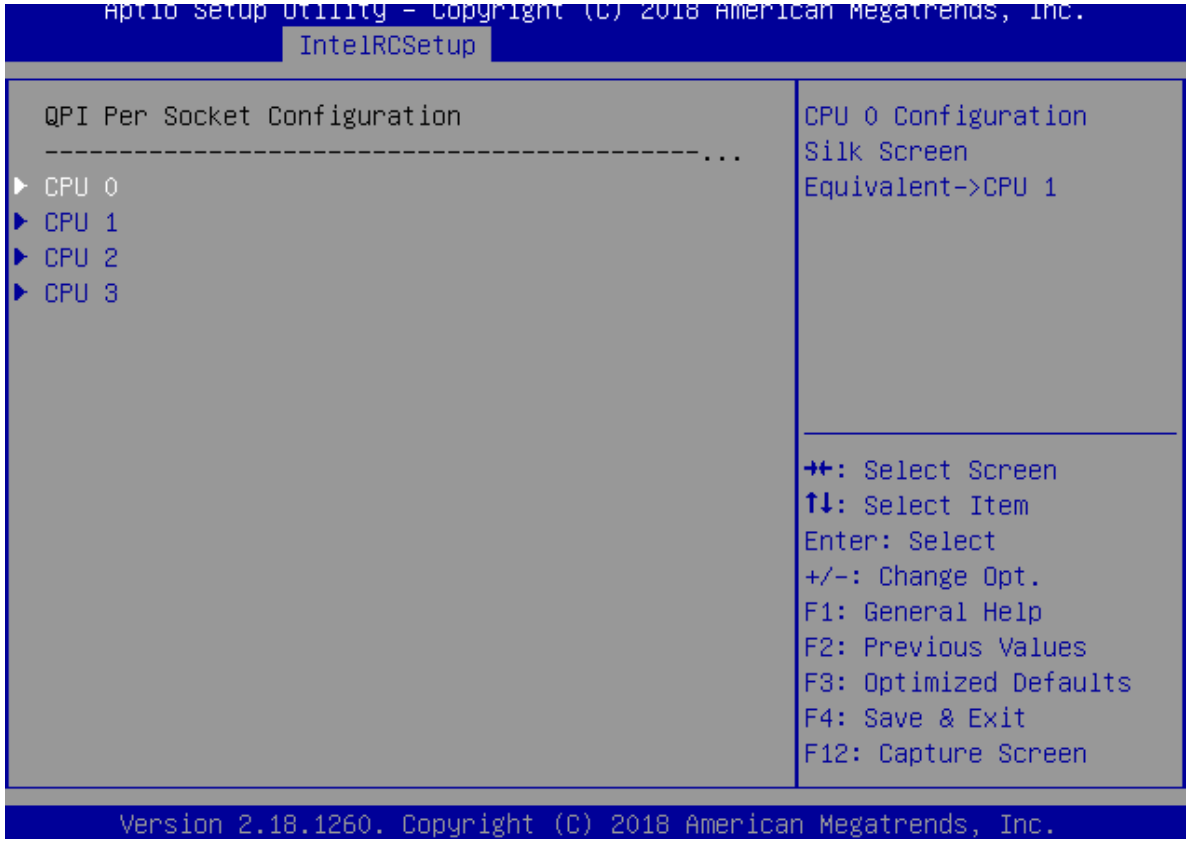
QPI Configuration



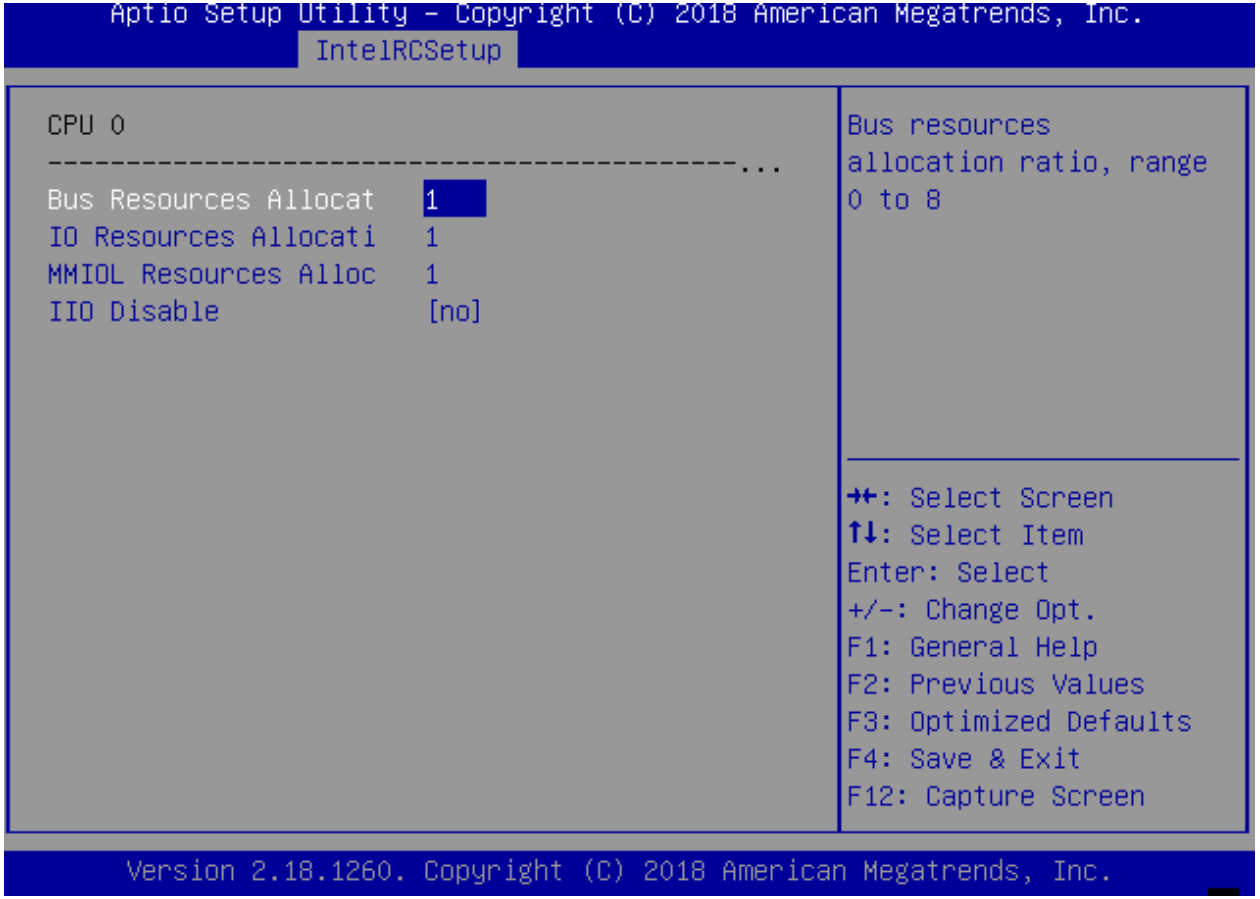
QPI General Configuration



QPI Per Socket Configuration

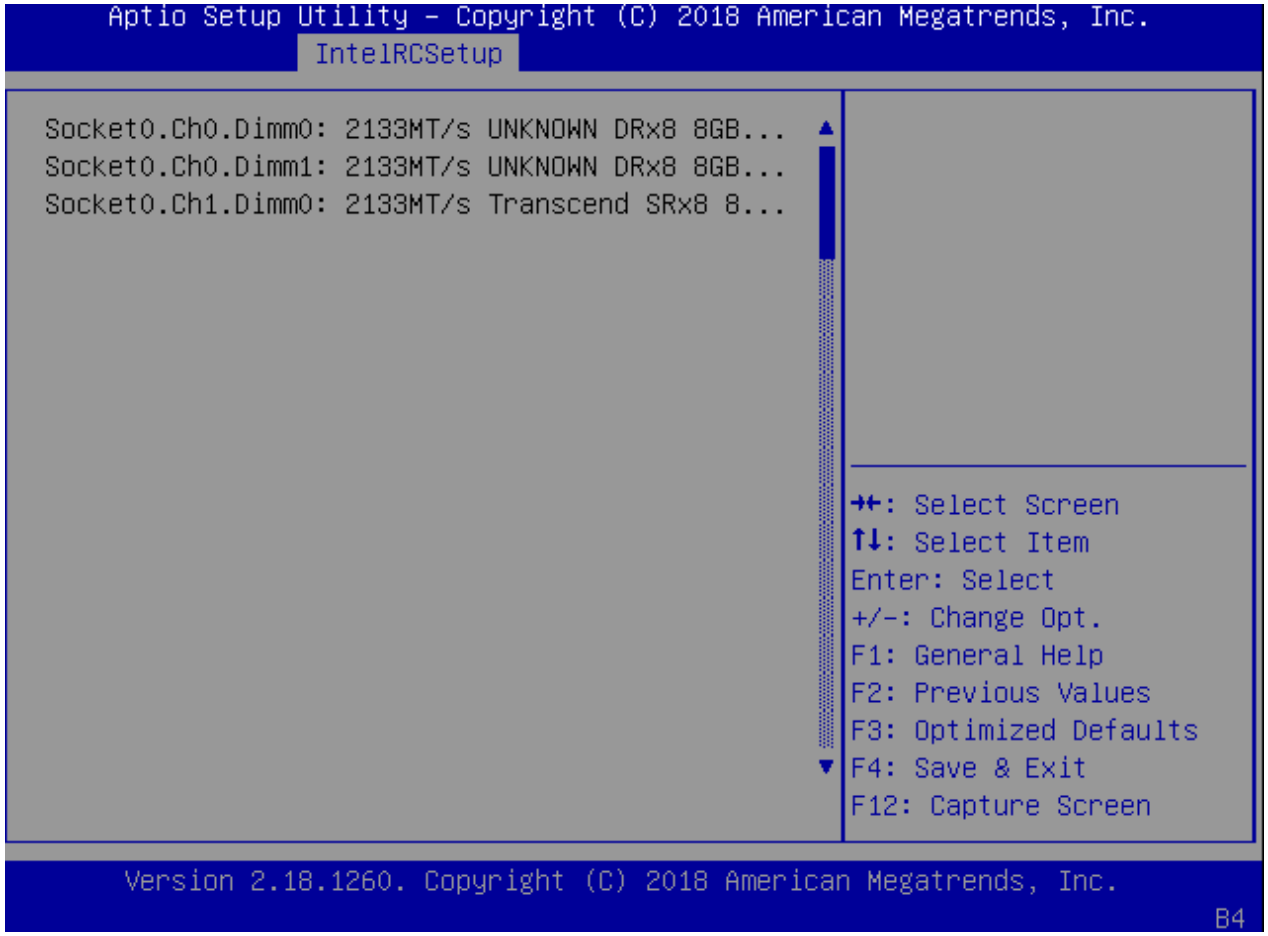


CPU (0~3)

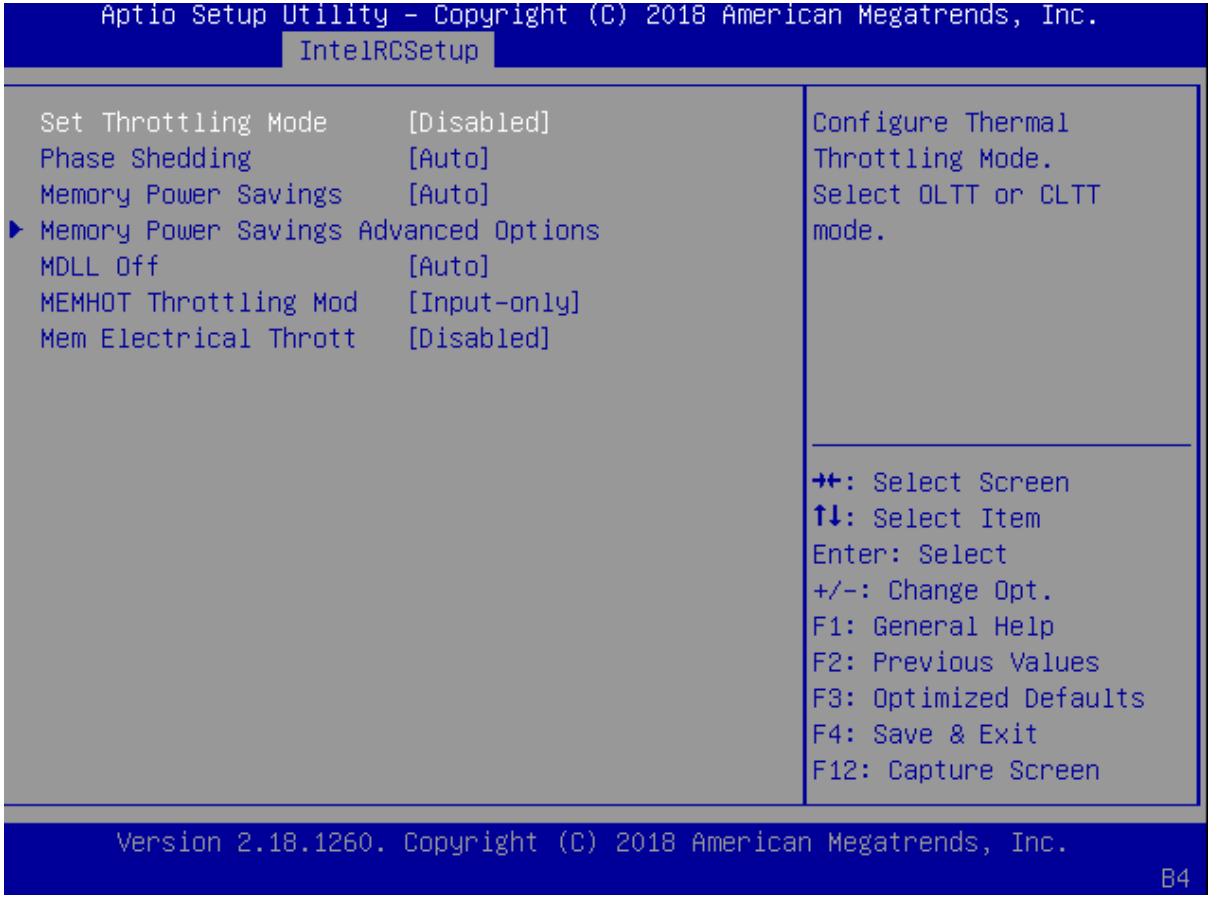

Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
IntelRCSetup
CPU 0
Bus Resources Allocat 1
IO Resources Allocati 1
MMIOL Resources Alloc 1
IIO Disable [no]
Bus resources allocation ratio, range 0 to 8
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.

Memory Configuration

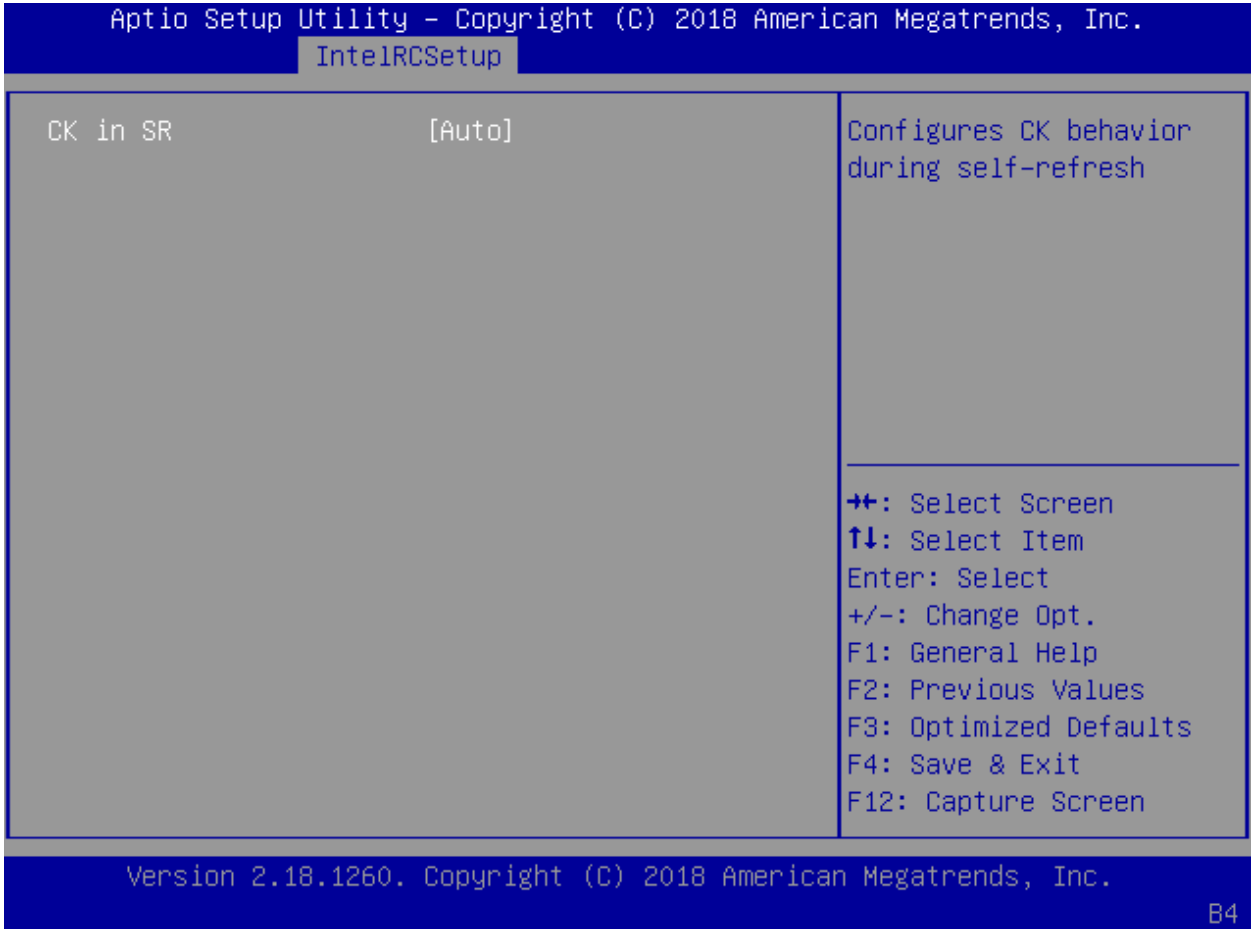
Memory Topology



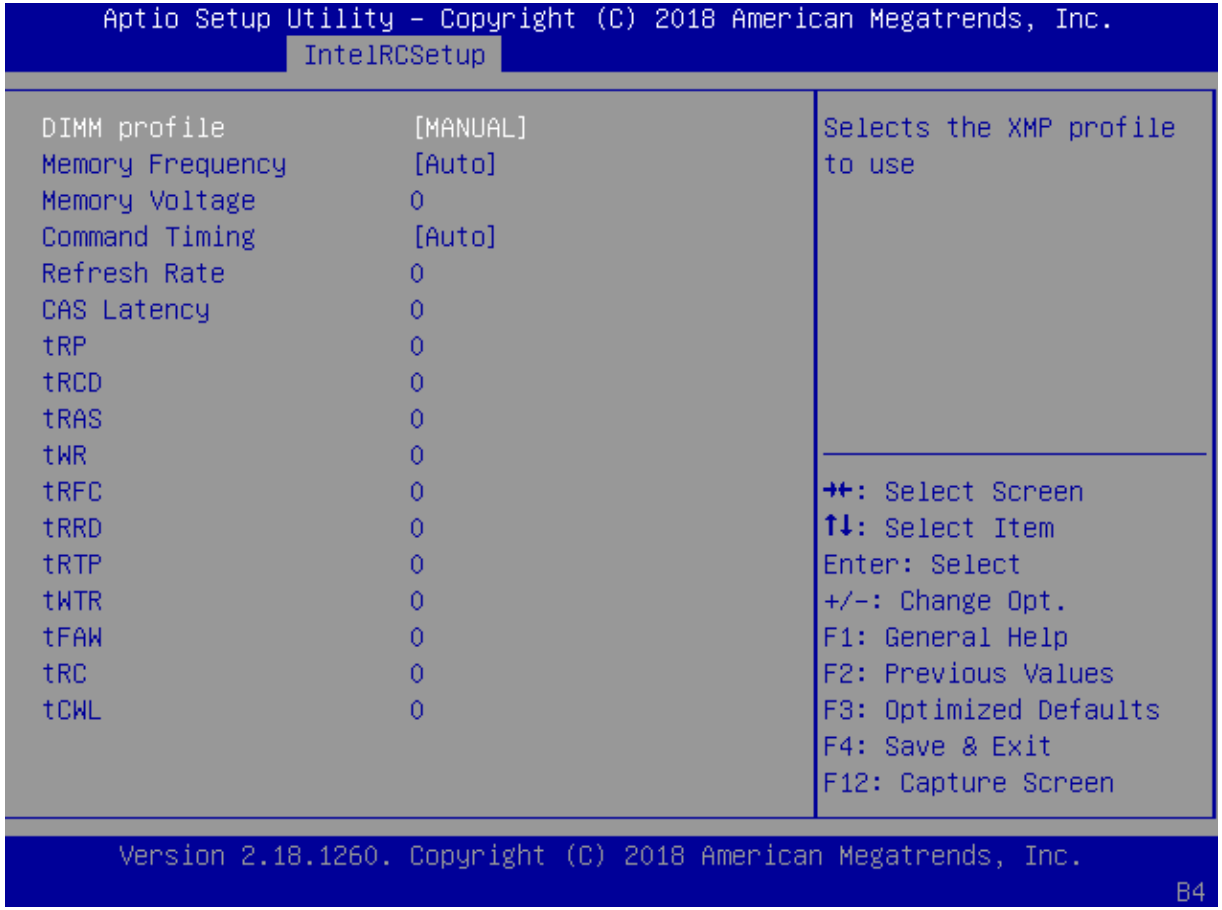
Memory Thermal



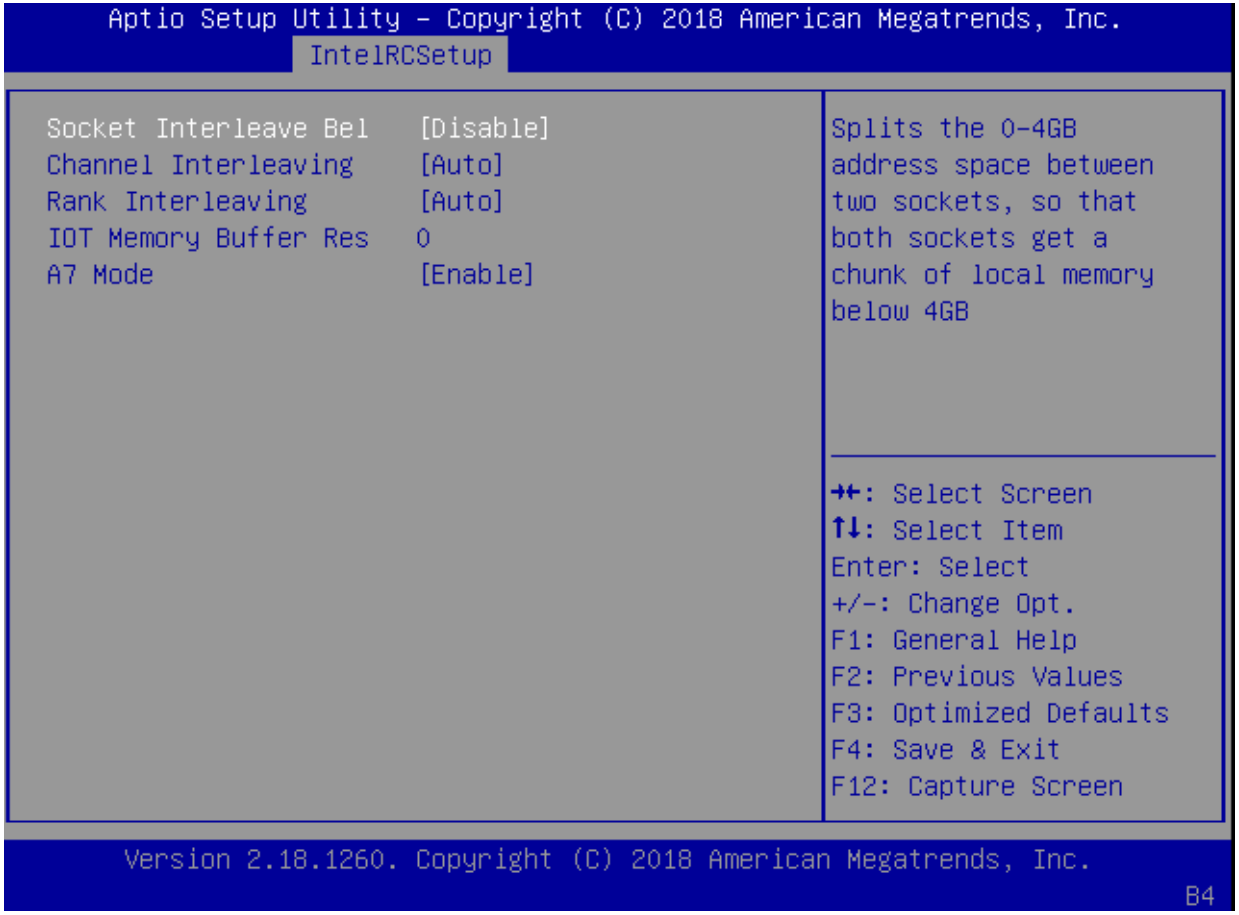
Memory Power Savings Advanced Options



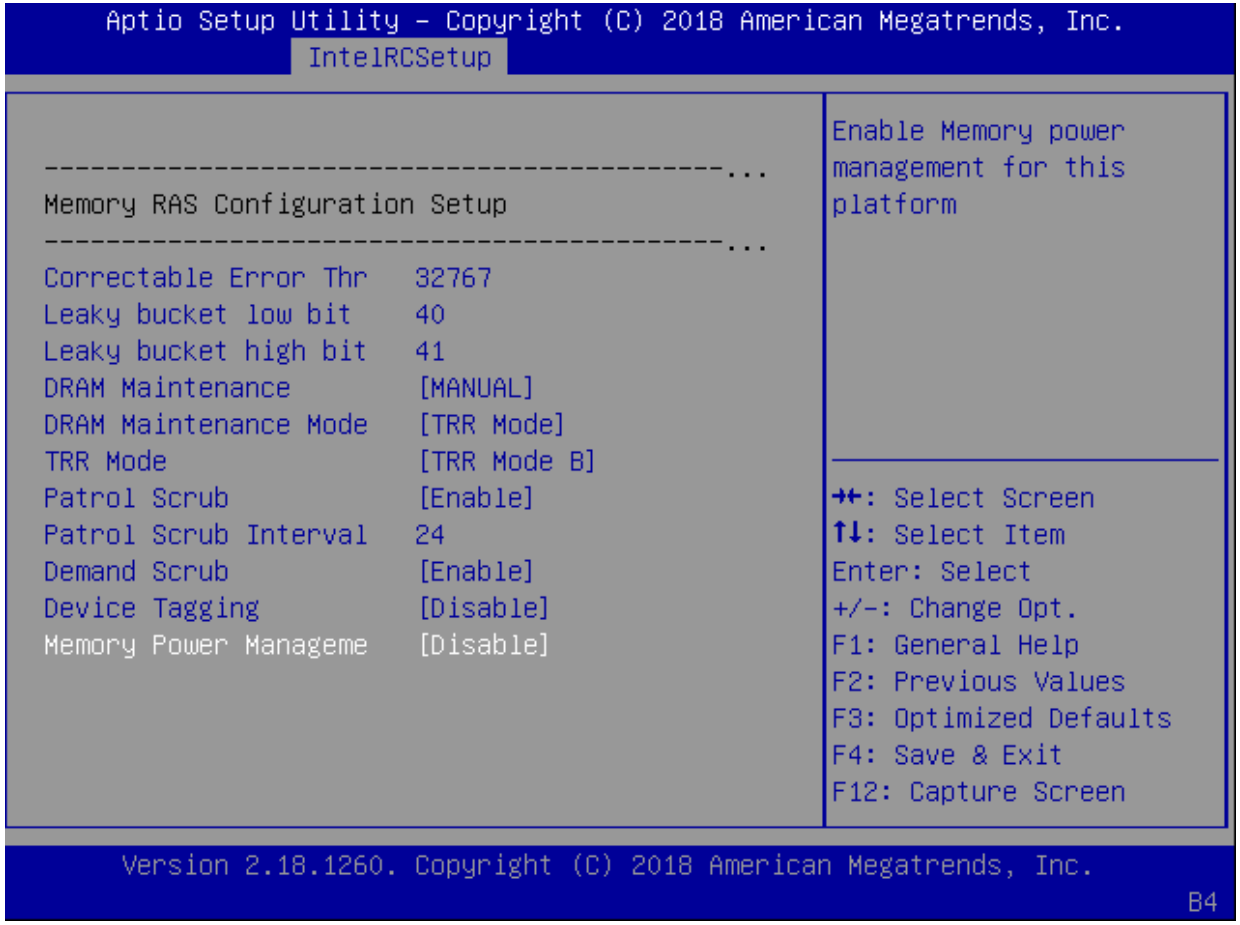
Memory Timings & Voltage Override



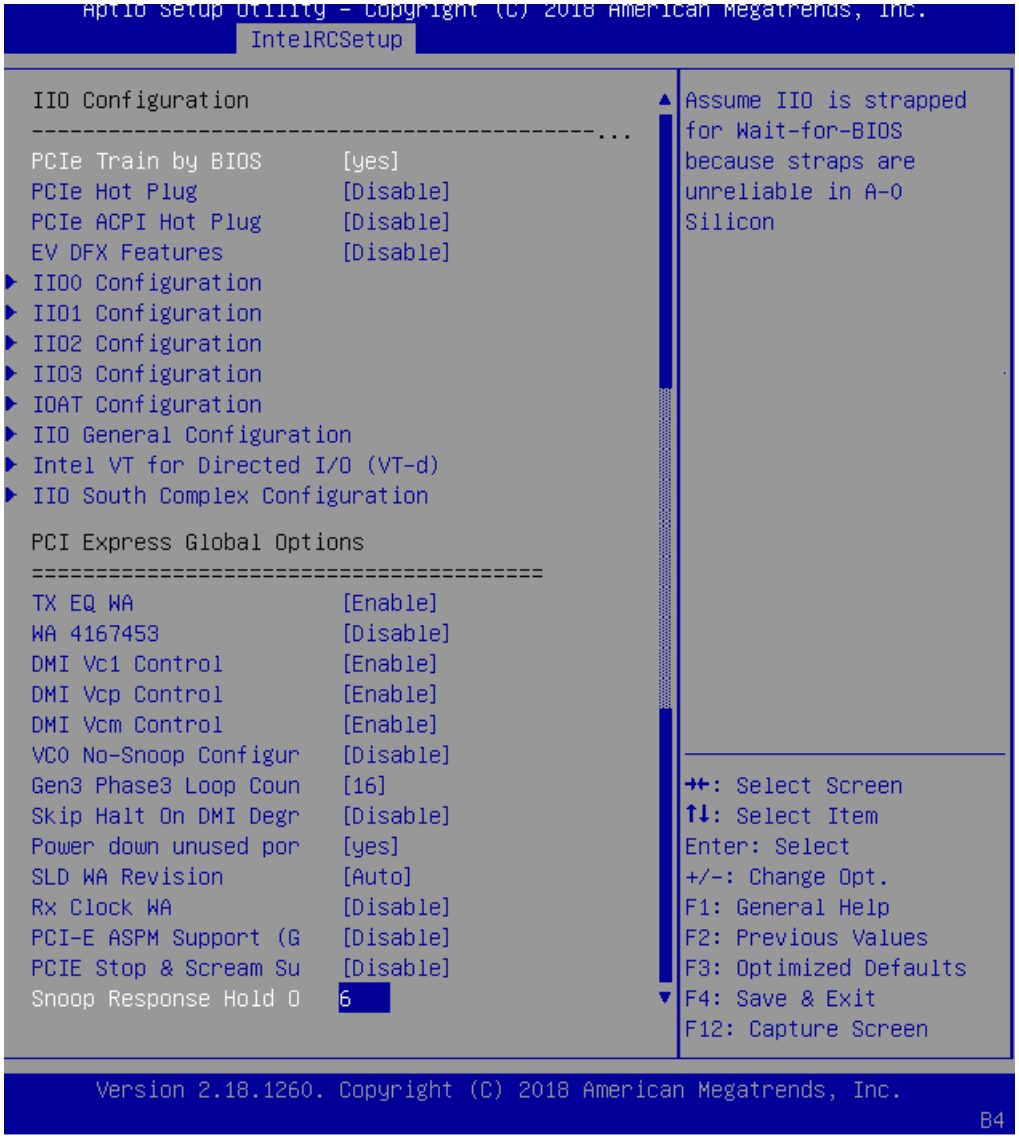
Memory Map


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
IntelRCSetup
Socket Interleave Bel [Disable]
Channel Interleaving [Auto]
Rank Interleaving [Auto]
IOT Memory Buffer Res 0
A7 Mode [Enable]
Splits the 0-4GB address space between two sockets, so that both sockets get a chunk of local memory below 4GB
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.
B4

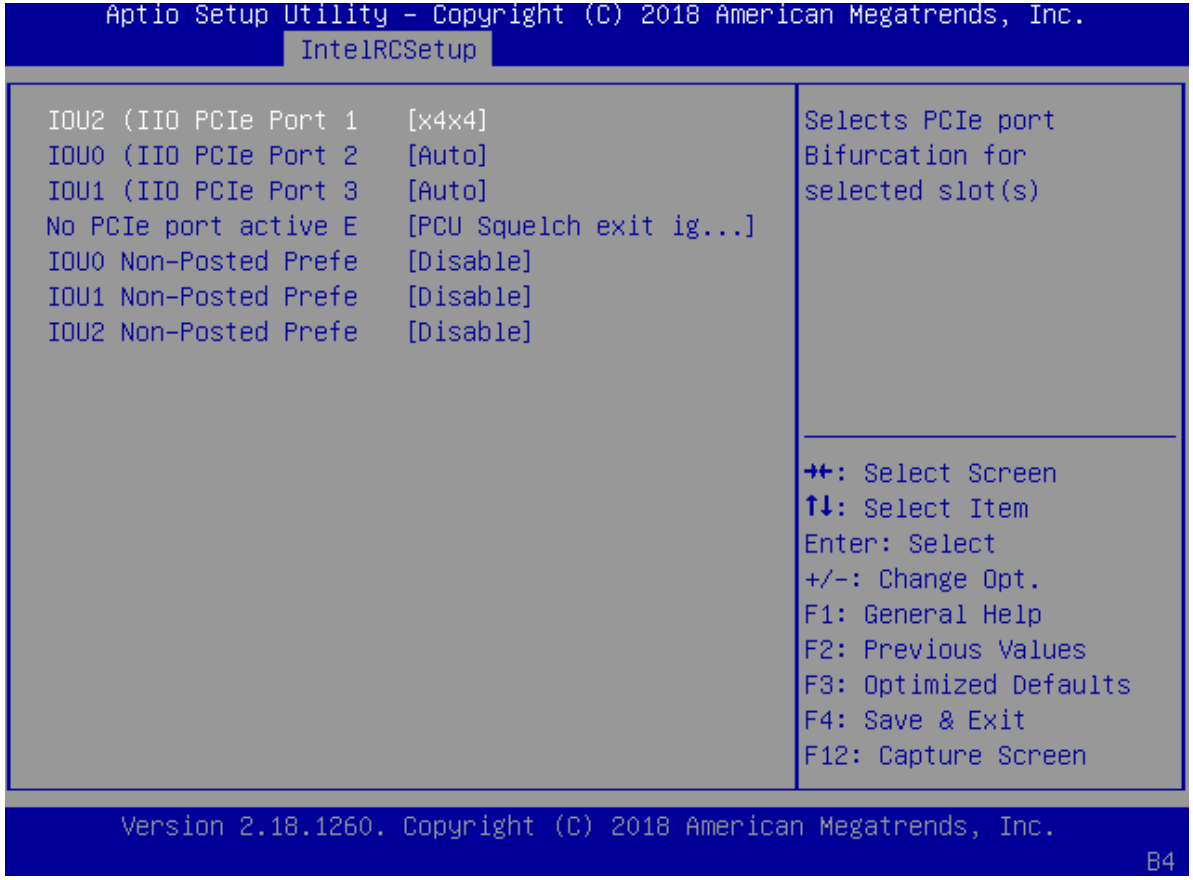
Memory RAS Configuration



IIO Configuration

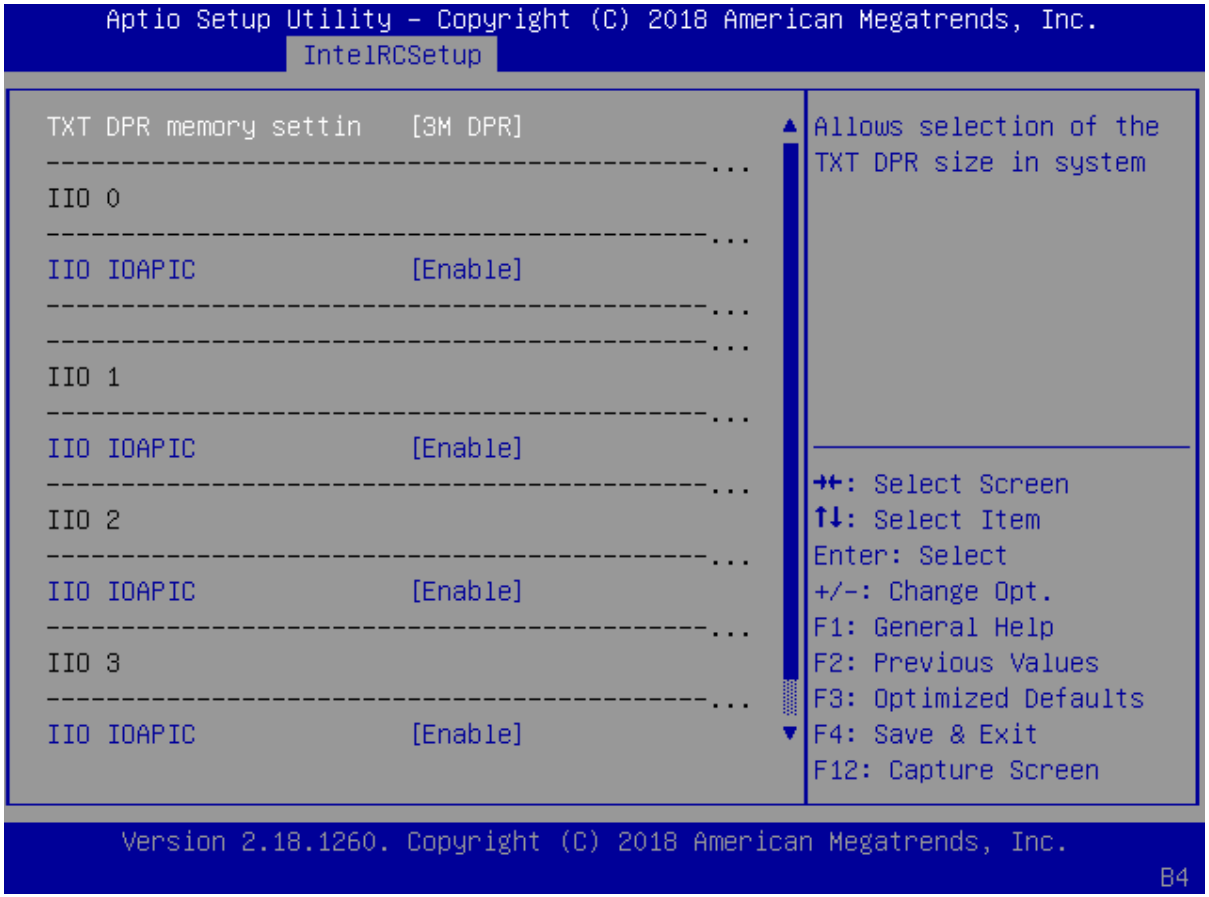


IIO (0~3) Configuration

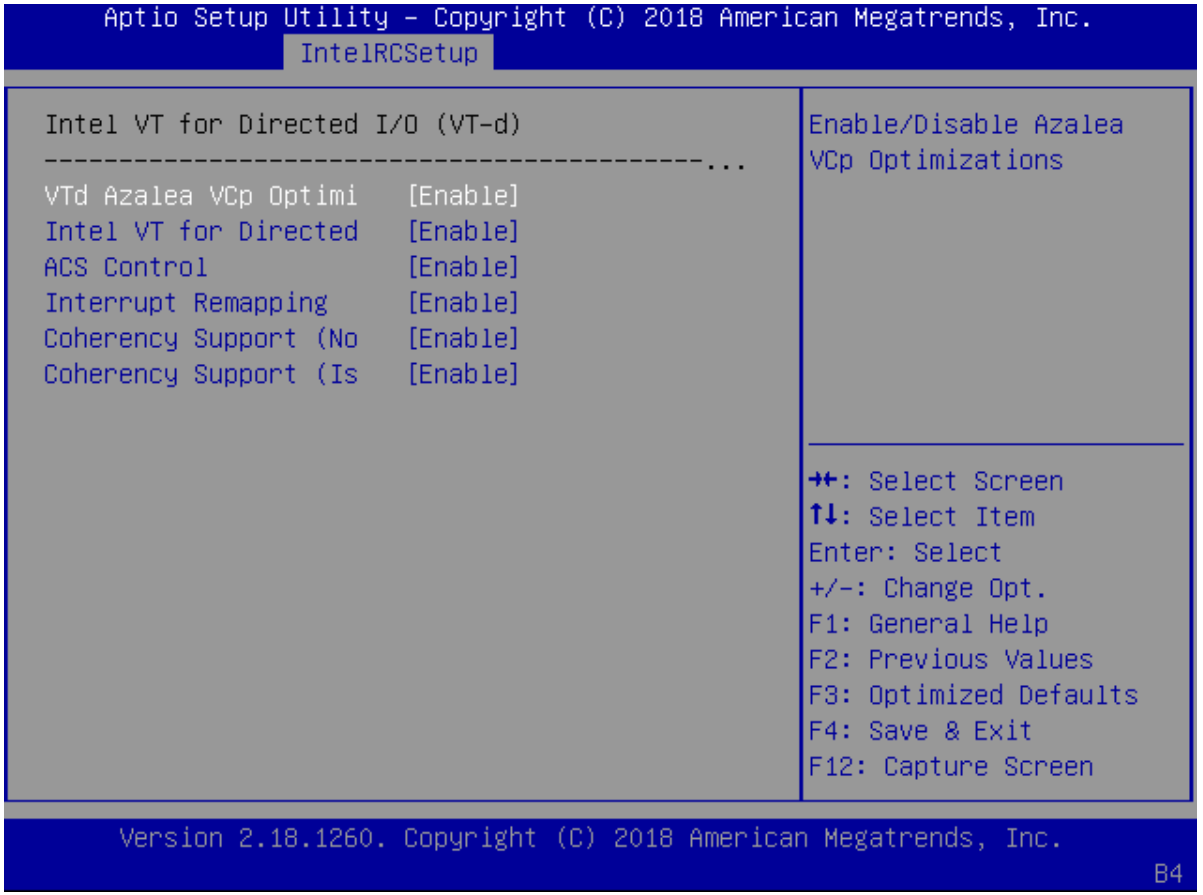


IOAT Configuration

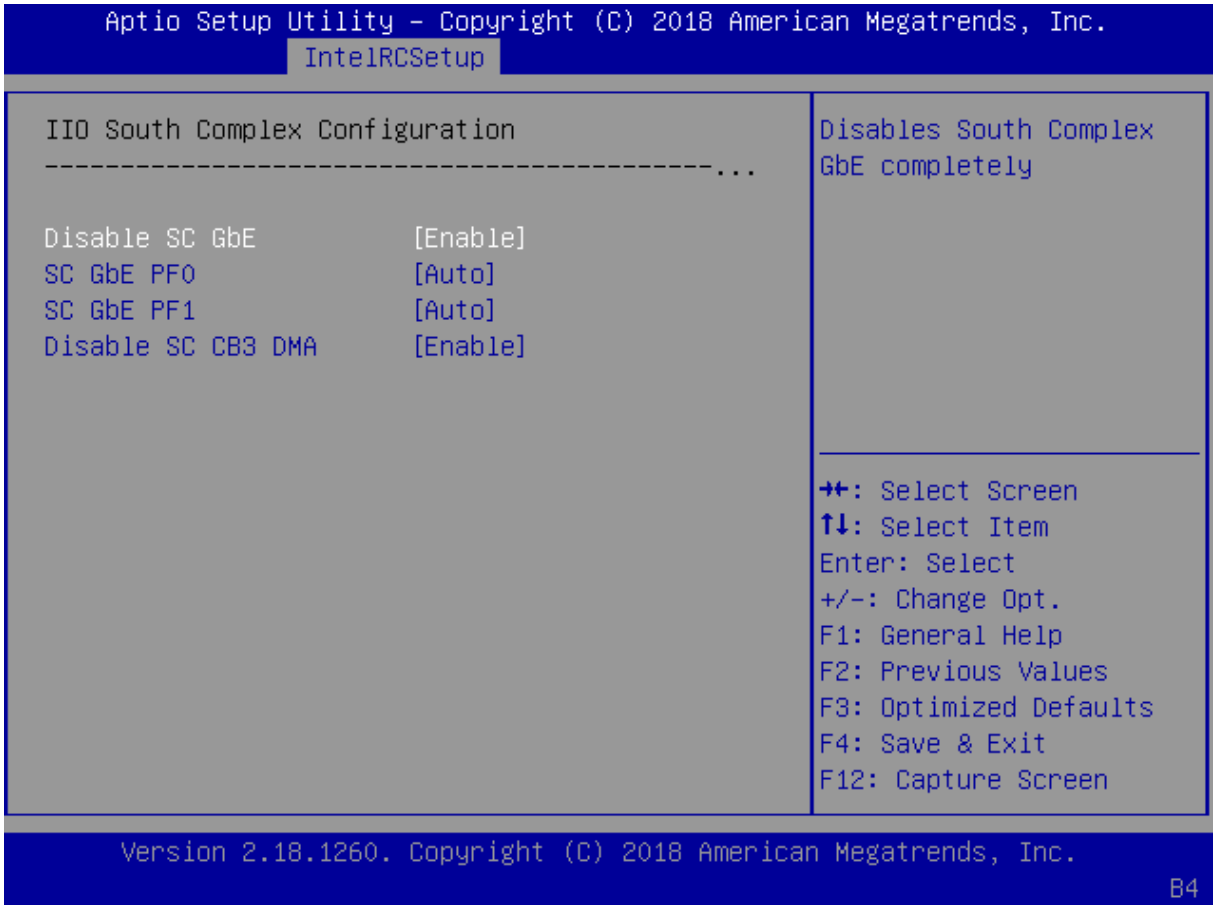
IIO General Configuration



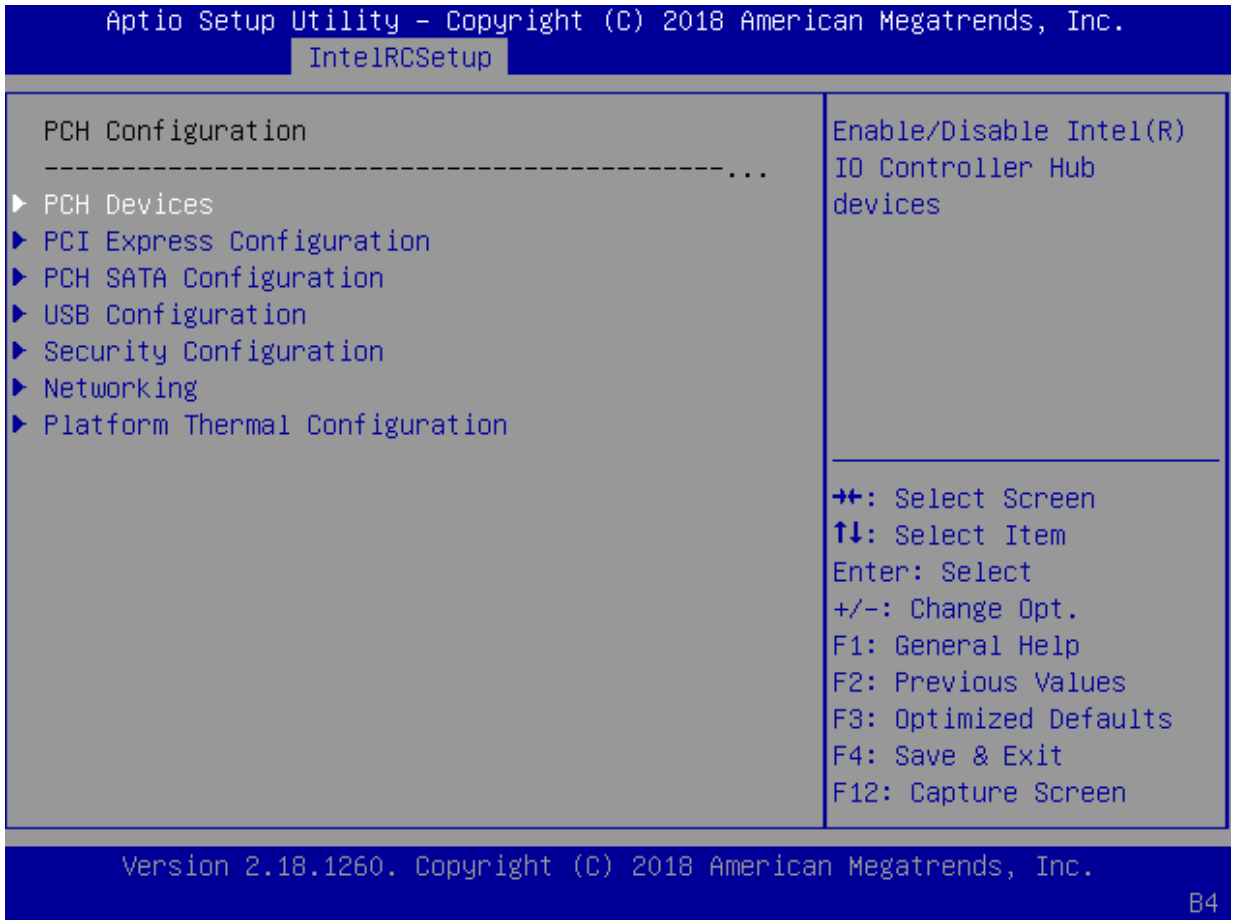
Intel VT for Directed I/O (VT-d)



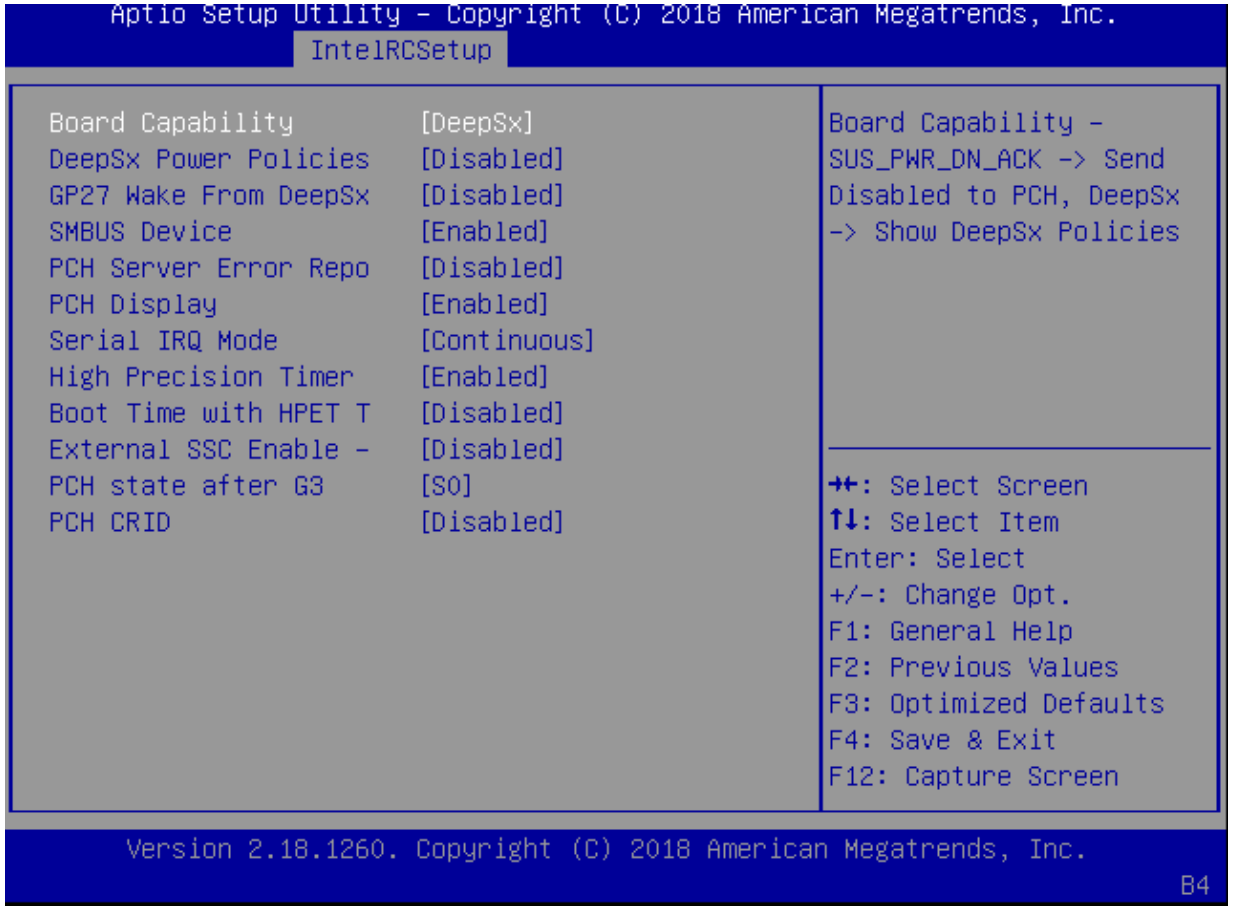
IIO South Complex Configuration



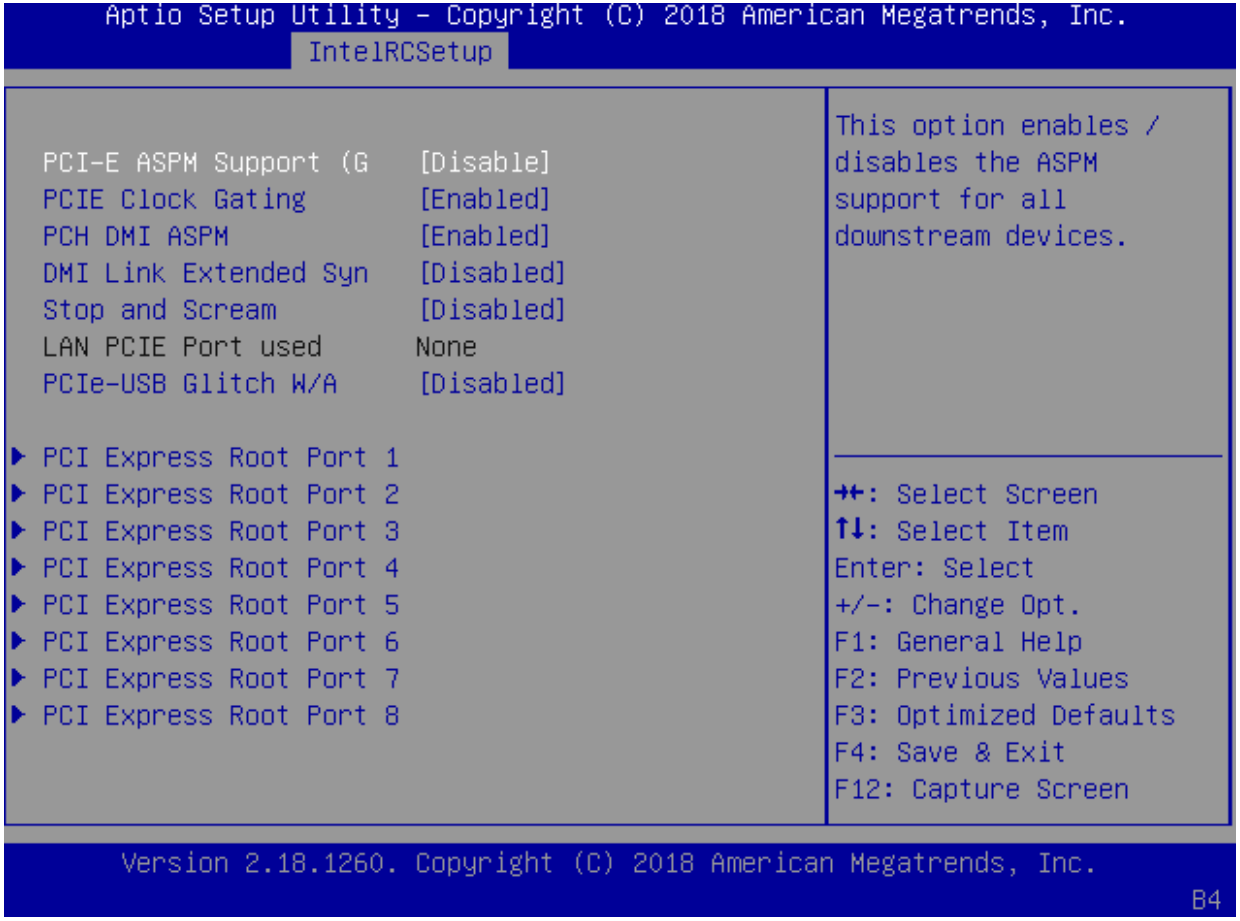
PCH Configuration



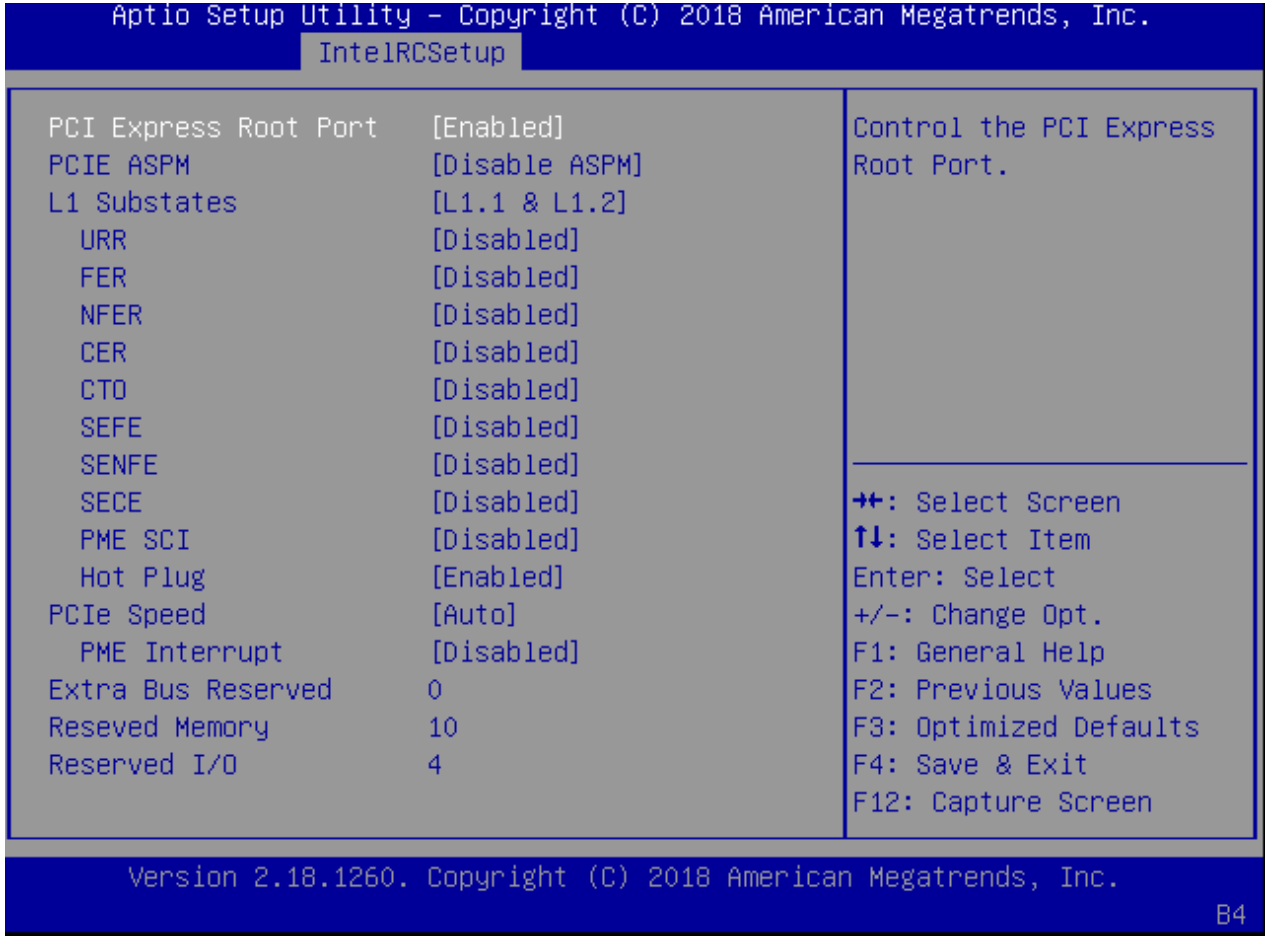
PCH Devices


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
IntelRCSetup
Board Capability [DeepSx]
DeepSx Power Policies [Disabled]
GP27 Wake From DeepSx [Disabled]
SMBUS Device [Enabled]
PCH Server Error Repo [Disabled]
PCH Display [Enabled]
Serial IRQ Mode [Continuous]
High Precision Timer [Enabled]
Boot Time with HPET T [Disabled]
External SSC Enable - [Disabled]
PCH state after G3 [S0]
PCH CRID [Disabled]
Board Capability - SUS_PWR_DN_ACK -> Send Disabled to PCH, DeepSx -> Show DeepSx Policies
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.
B4

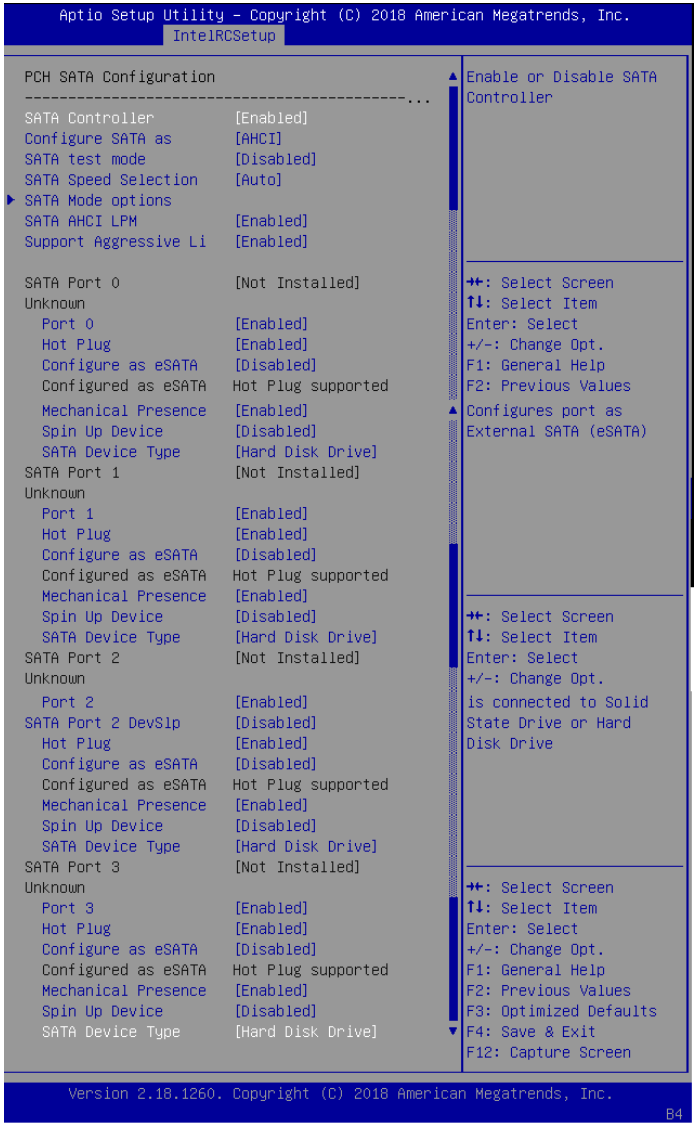
PCI Express Configuration



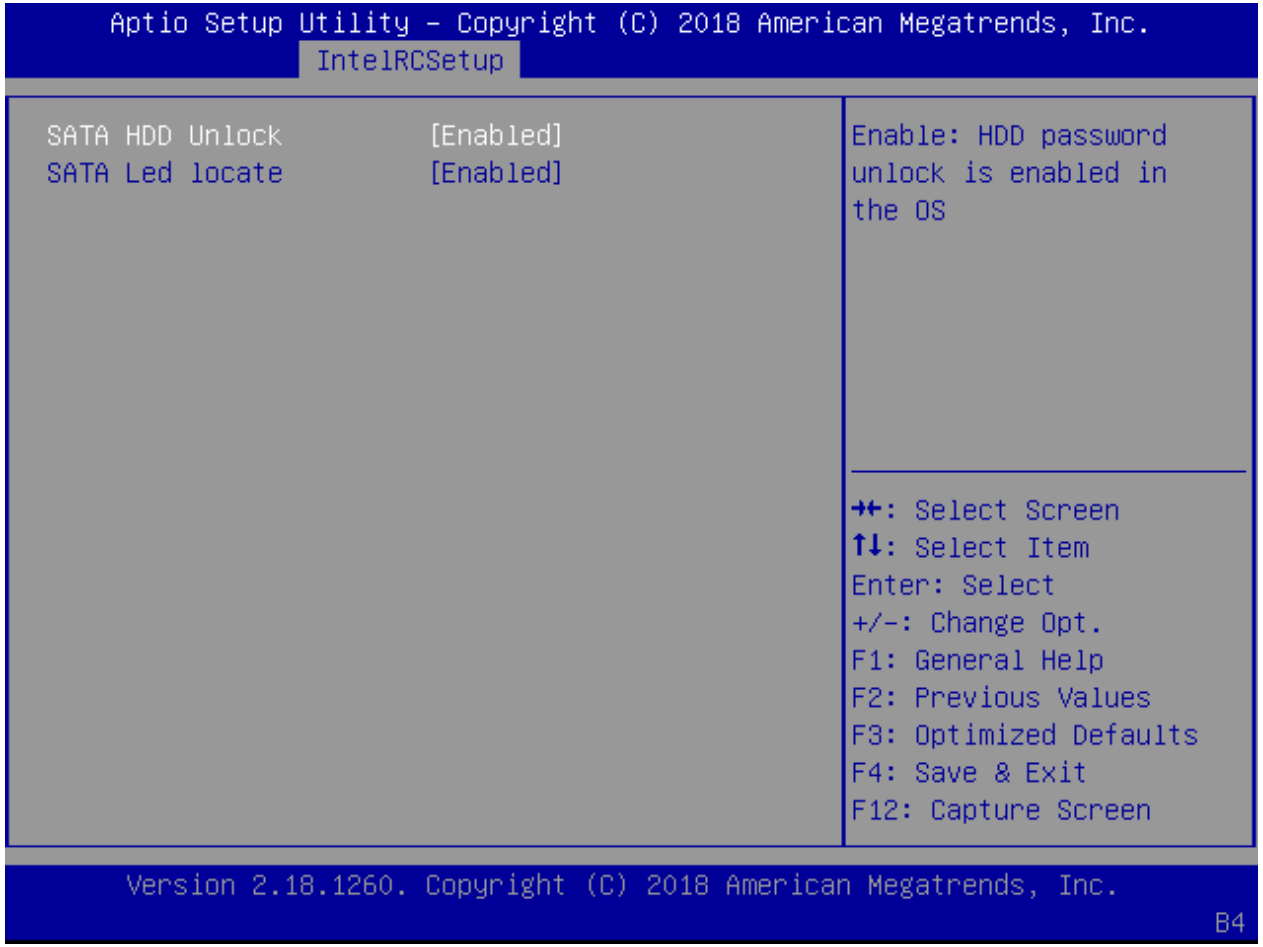
PCI Express Root Port 1~8



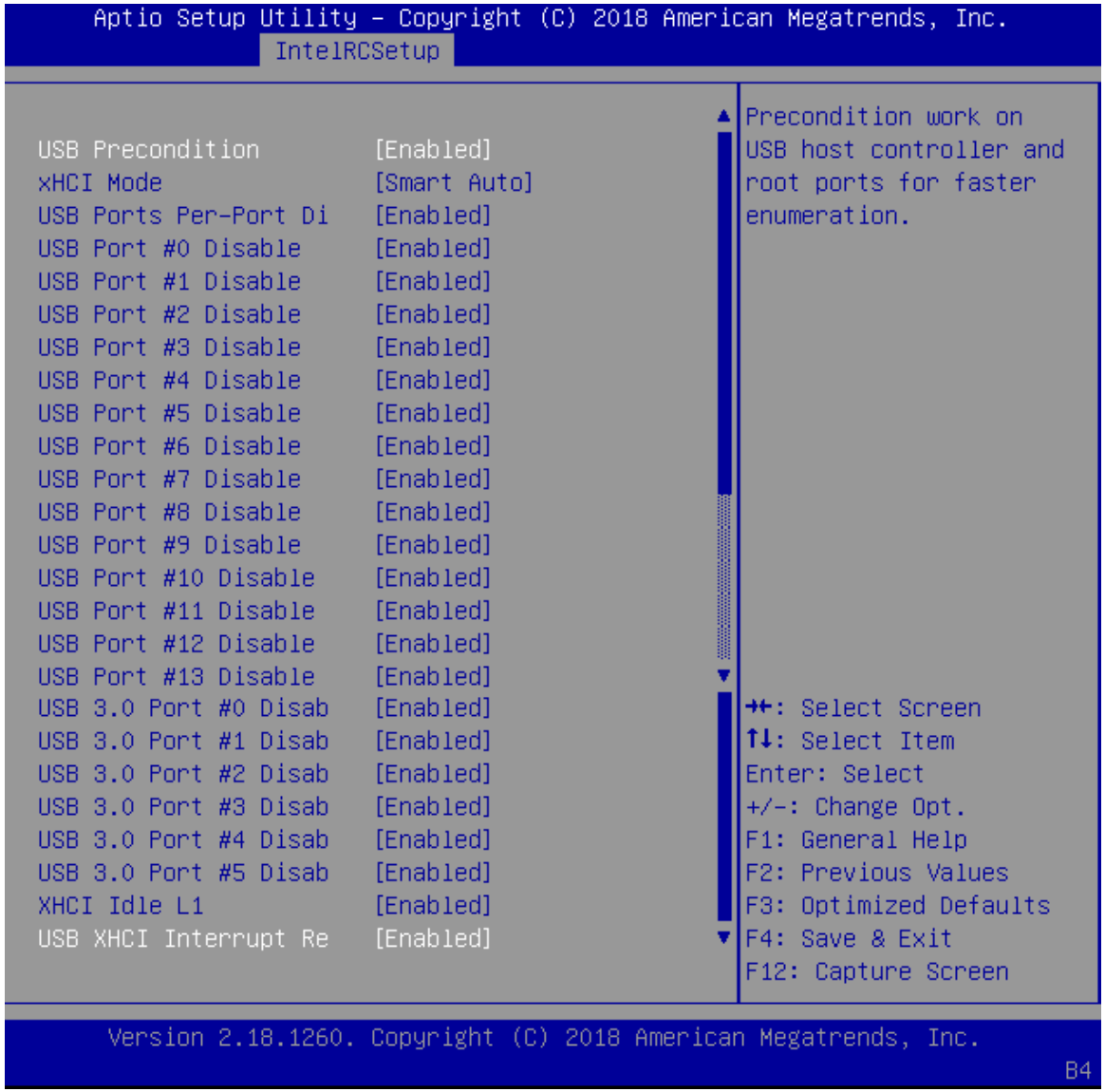
PCH SATA Configuration



SATA Mode options

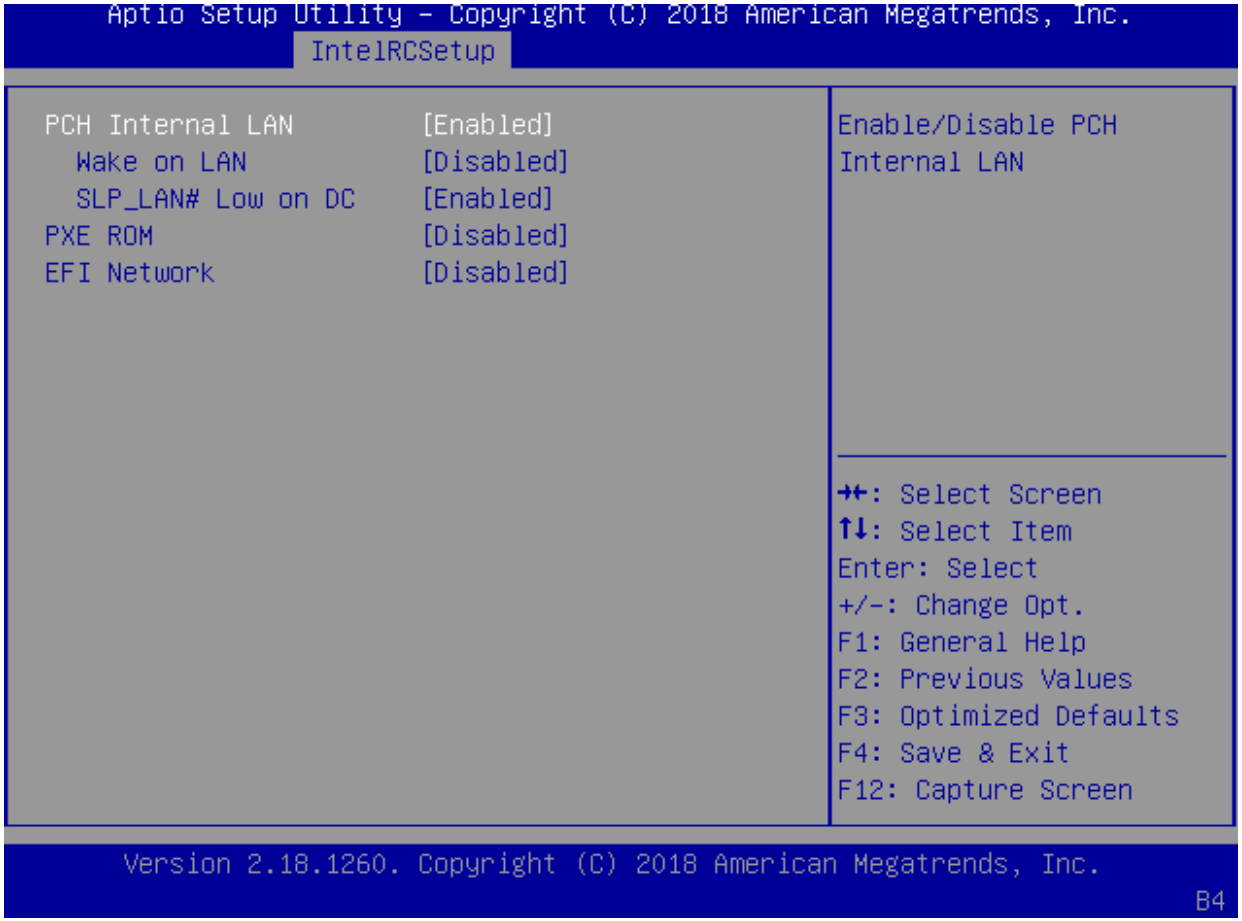


USB Configuration



Security Configuration

Networking


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
IntelRCSetup
PCH Internal LAN [Enabled]
Wake on LAN [Disabled]
SLP_LAN# Low on DC [Enabled]
PXE ROM [Disabled]
EFI Network [Disabled]
Enable/Disable PCH Internal LAN
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.
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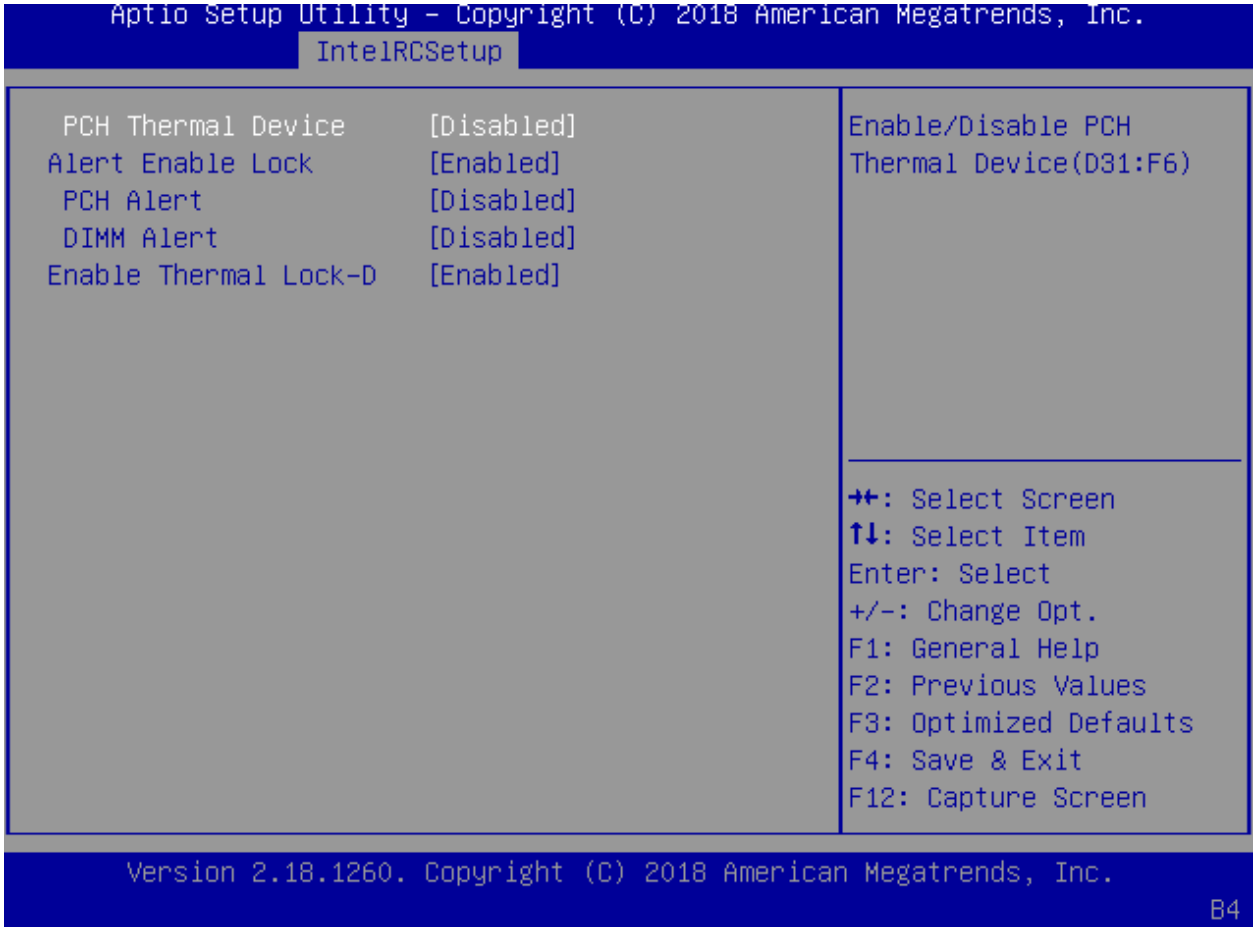
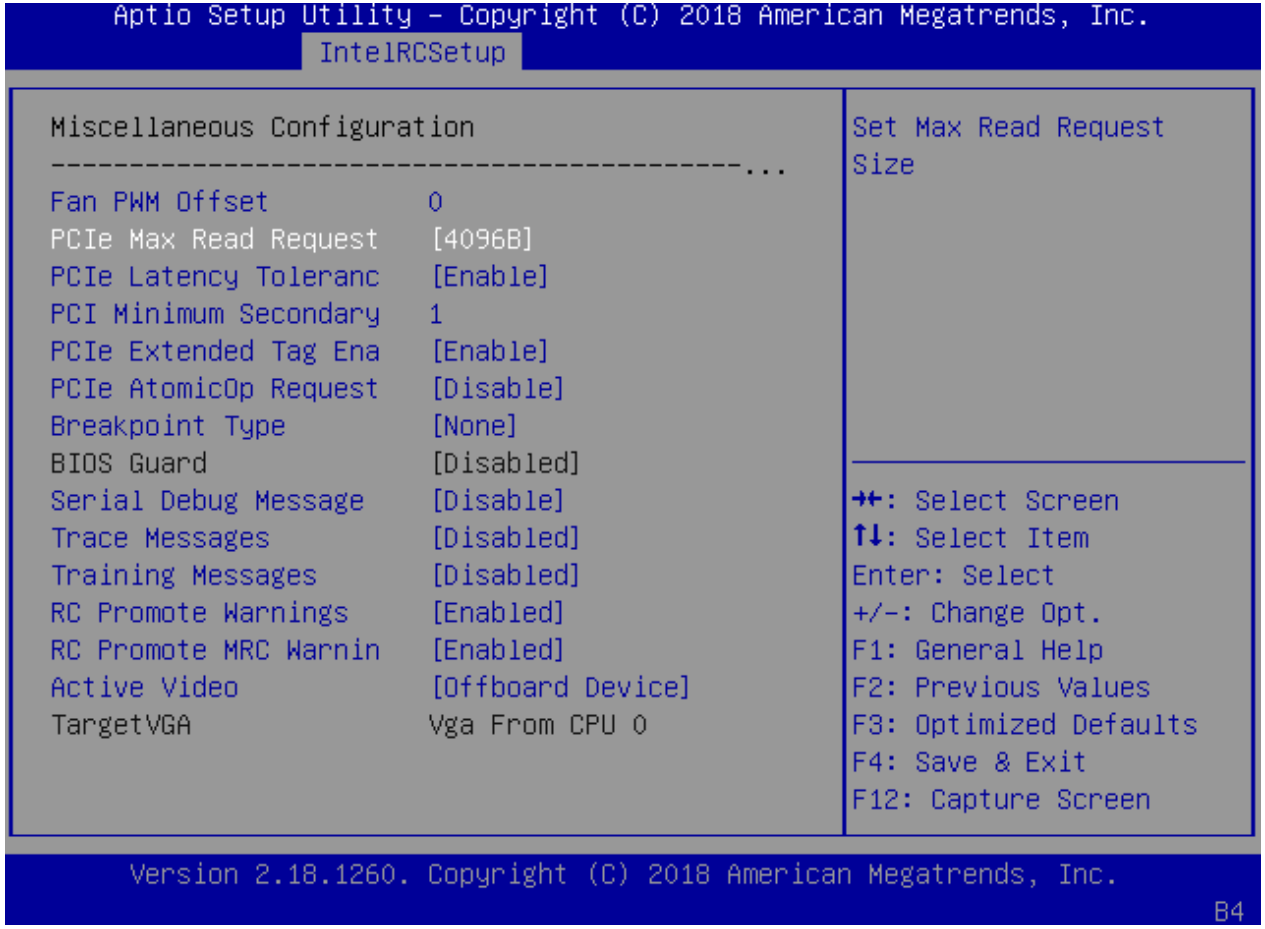
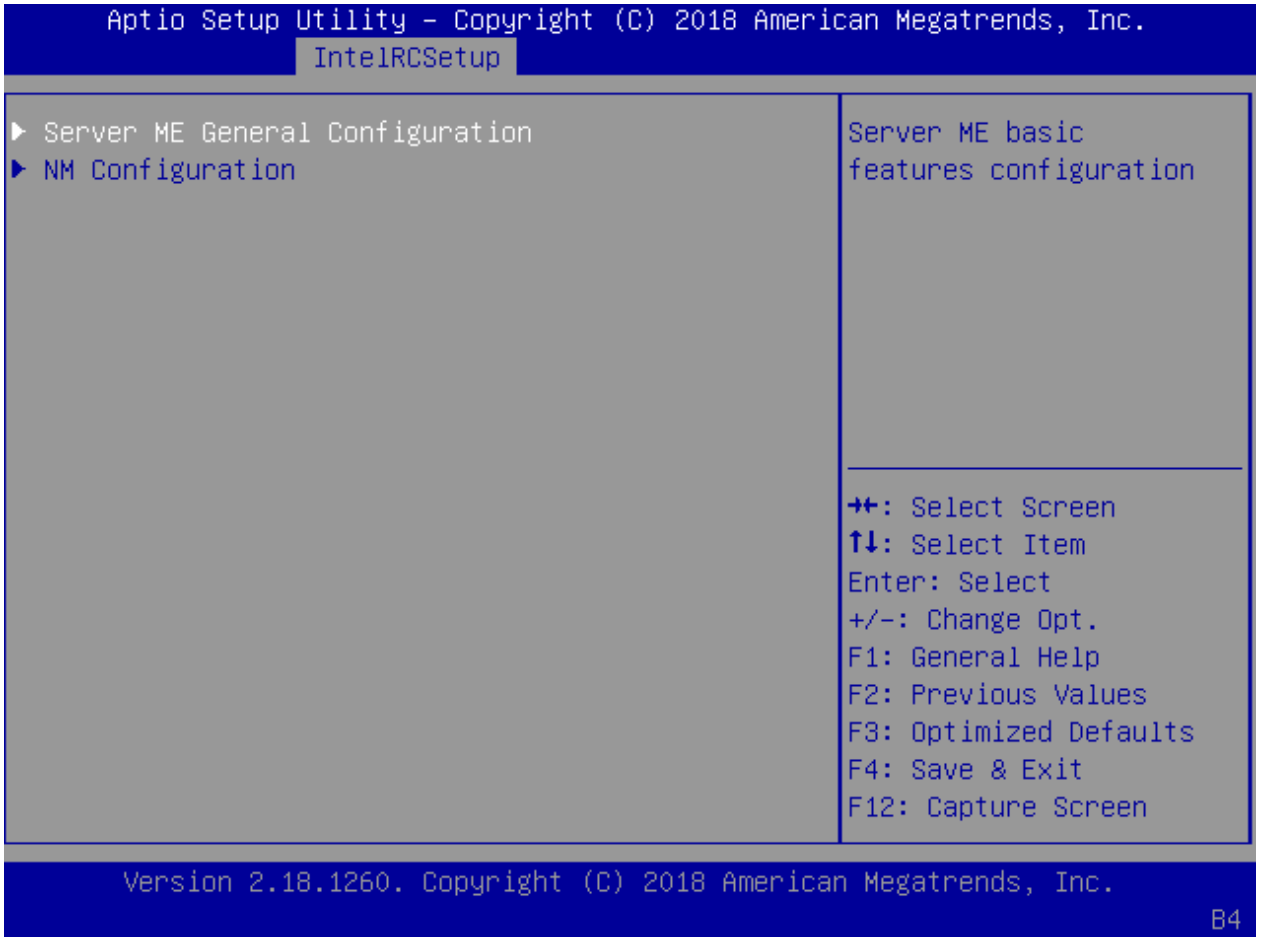
Platform Thermal Configuration



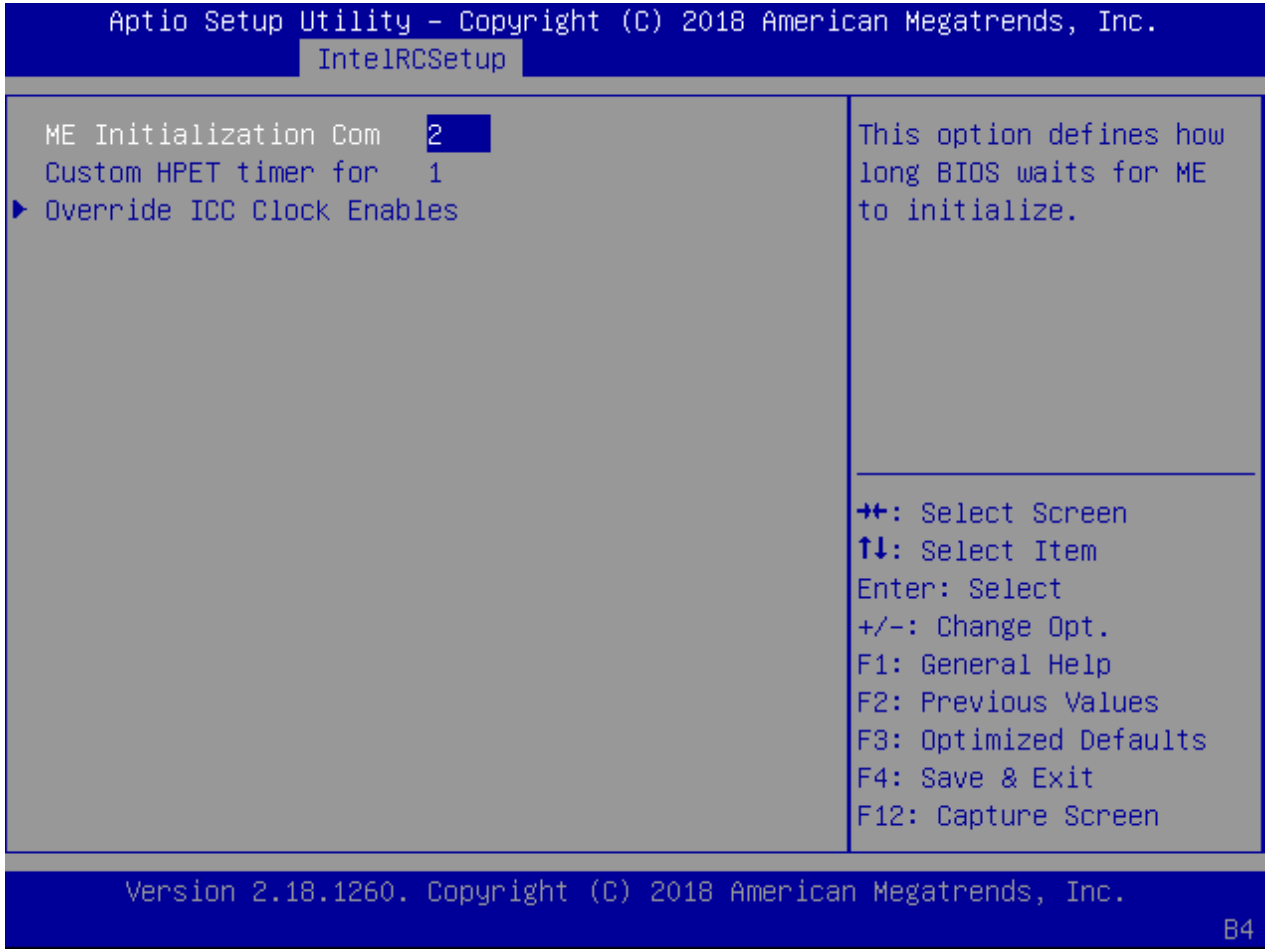
Miscellaneous Configuration



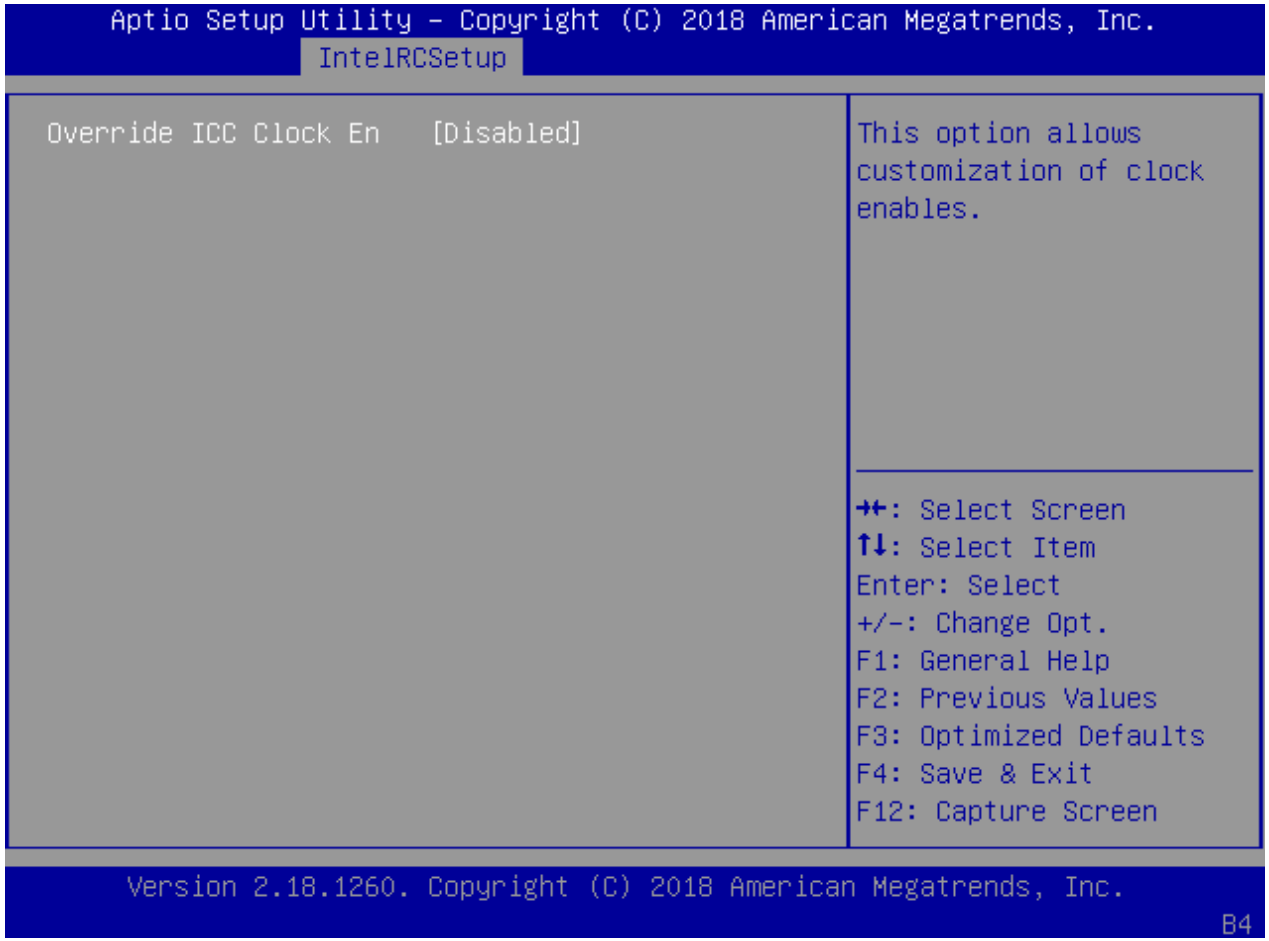
Server ME Debug Configuration



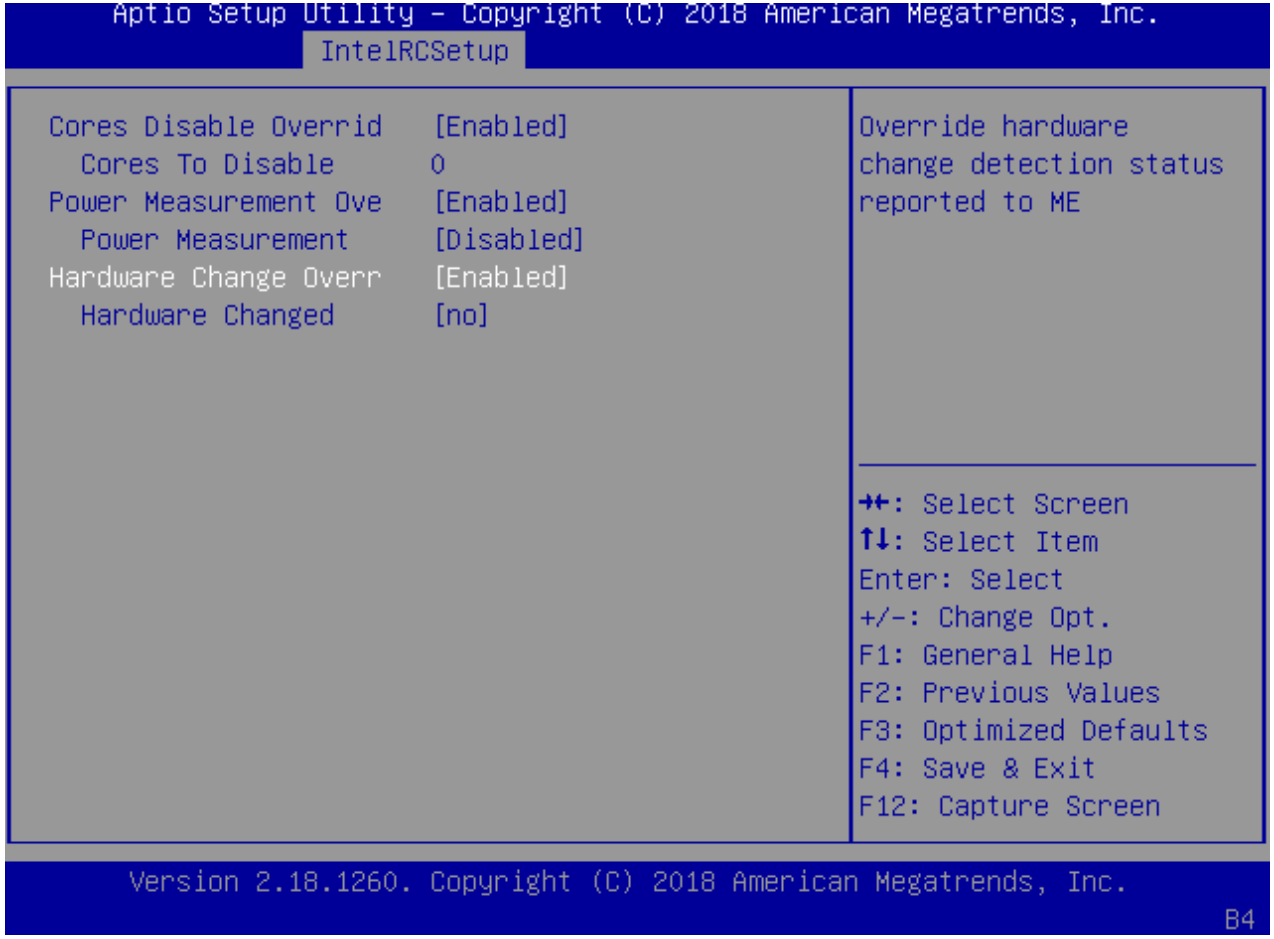
Server ME General Configuration



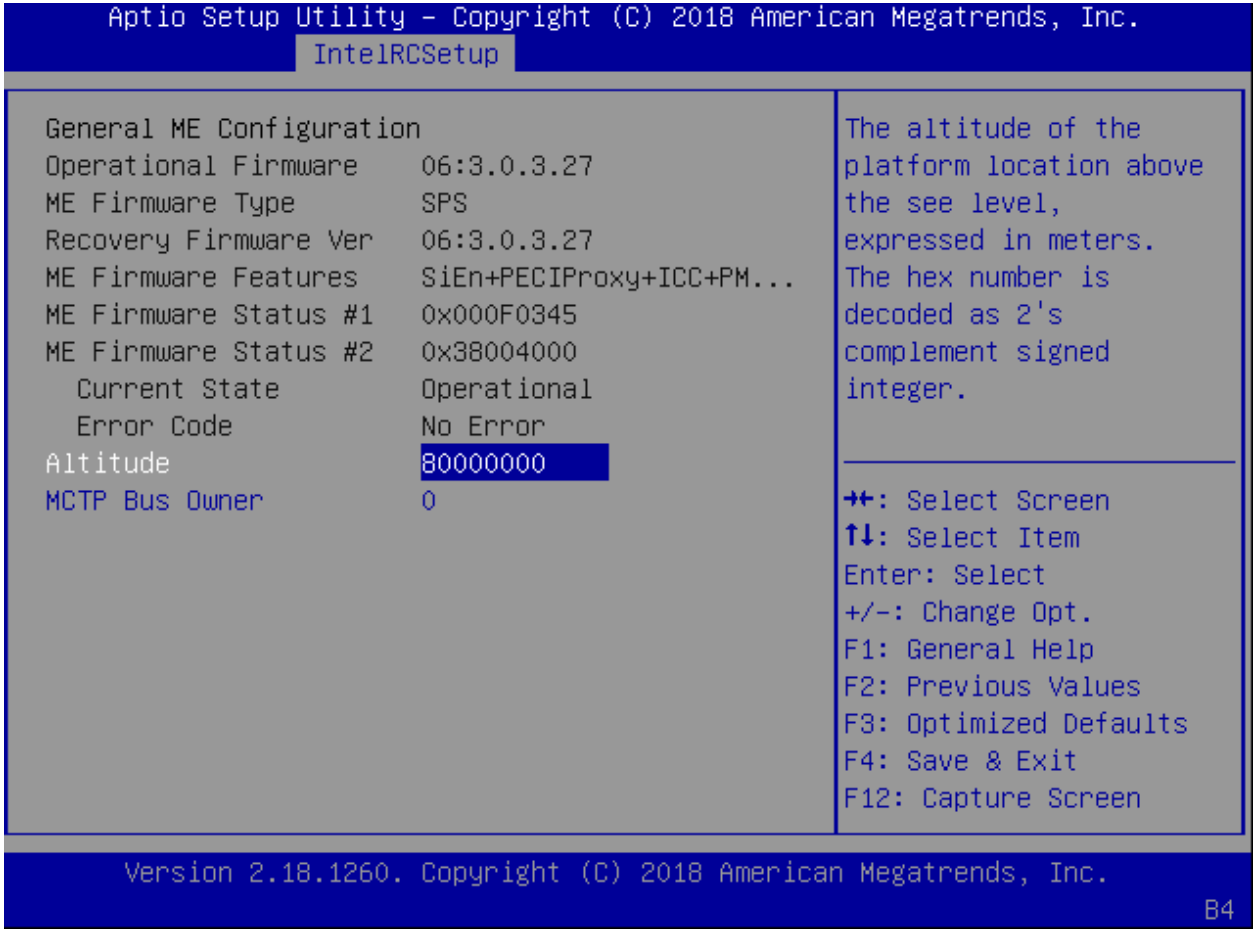
Override ICC Clock Enables



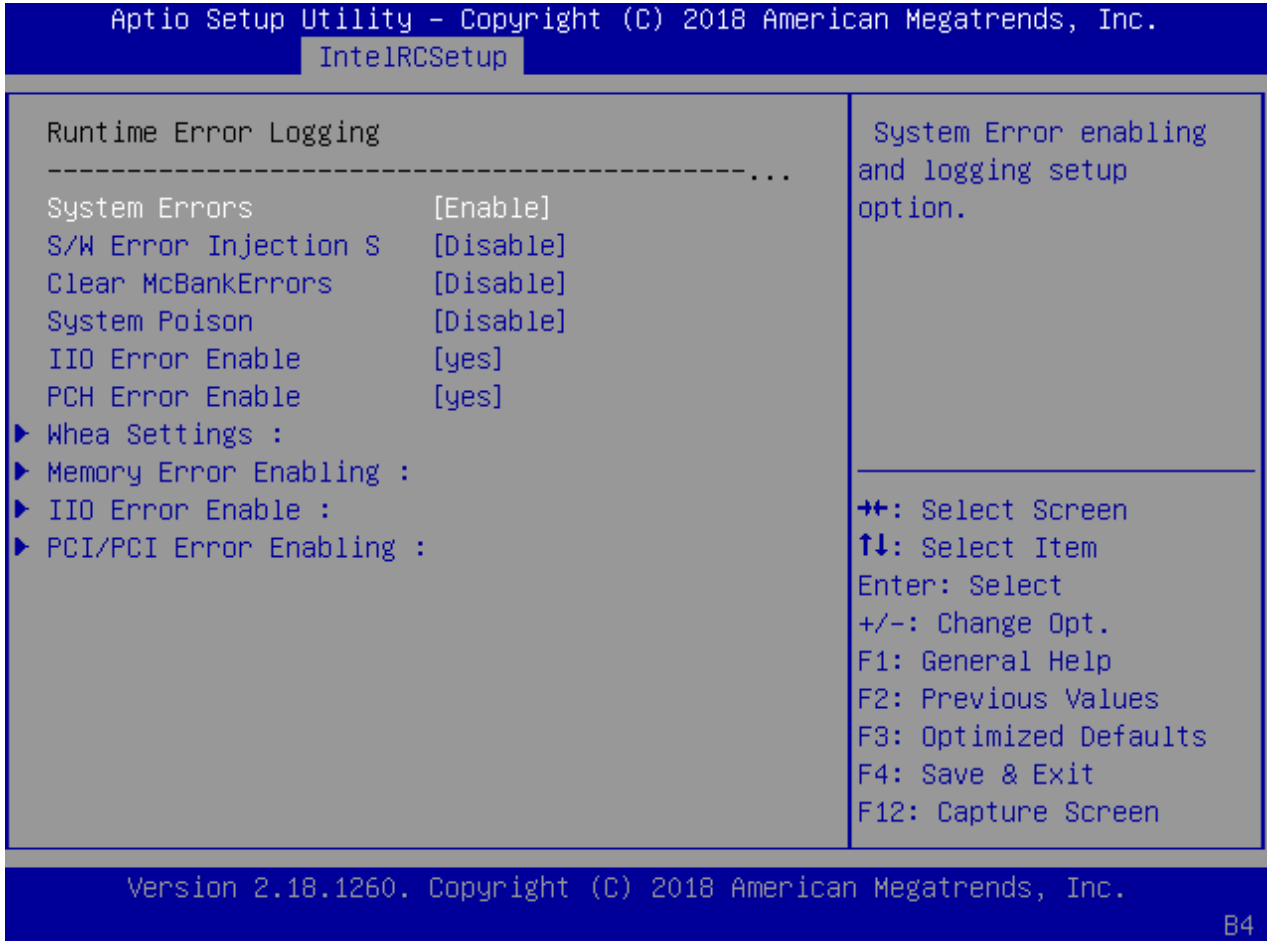
NM Configuration



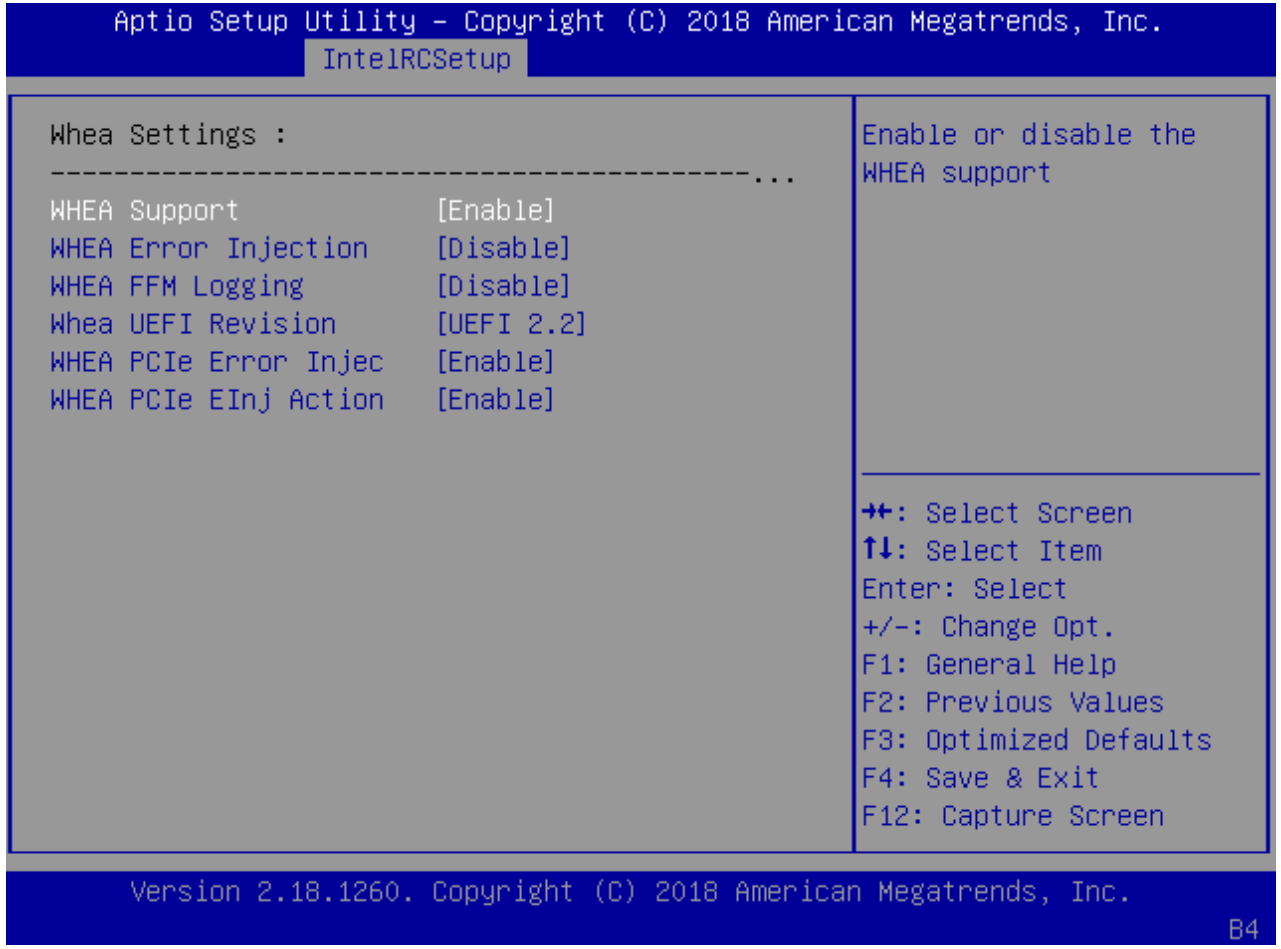
Server ME Configuration



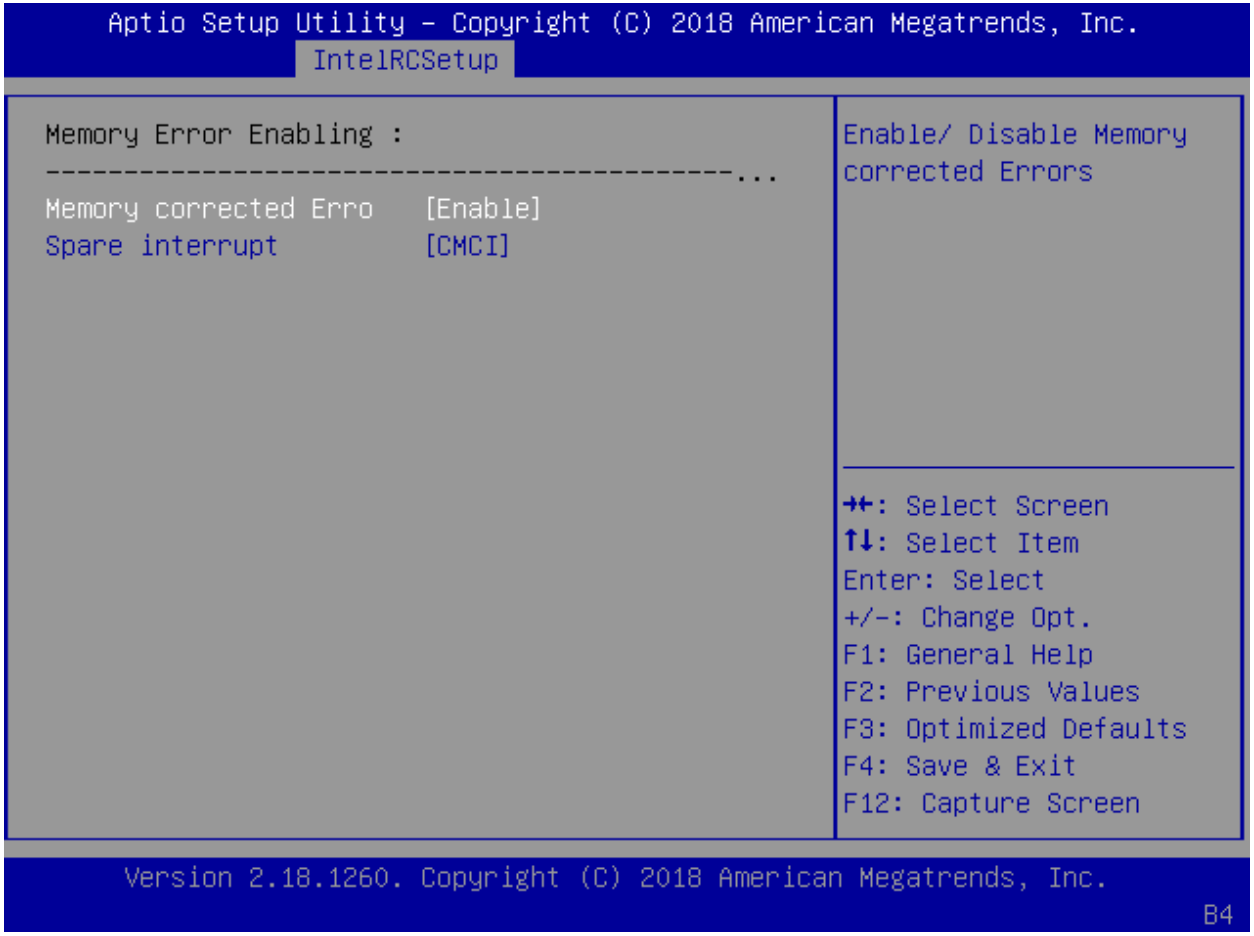
Runtime Error Logging



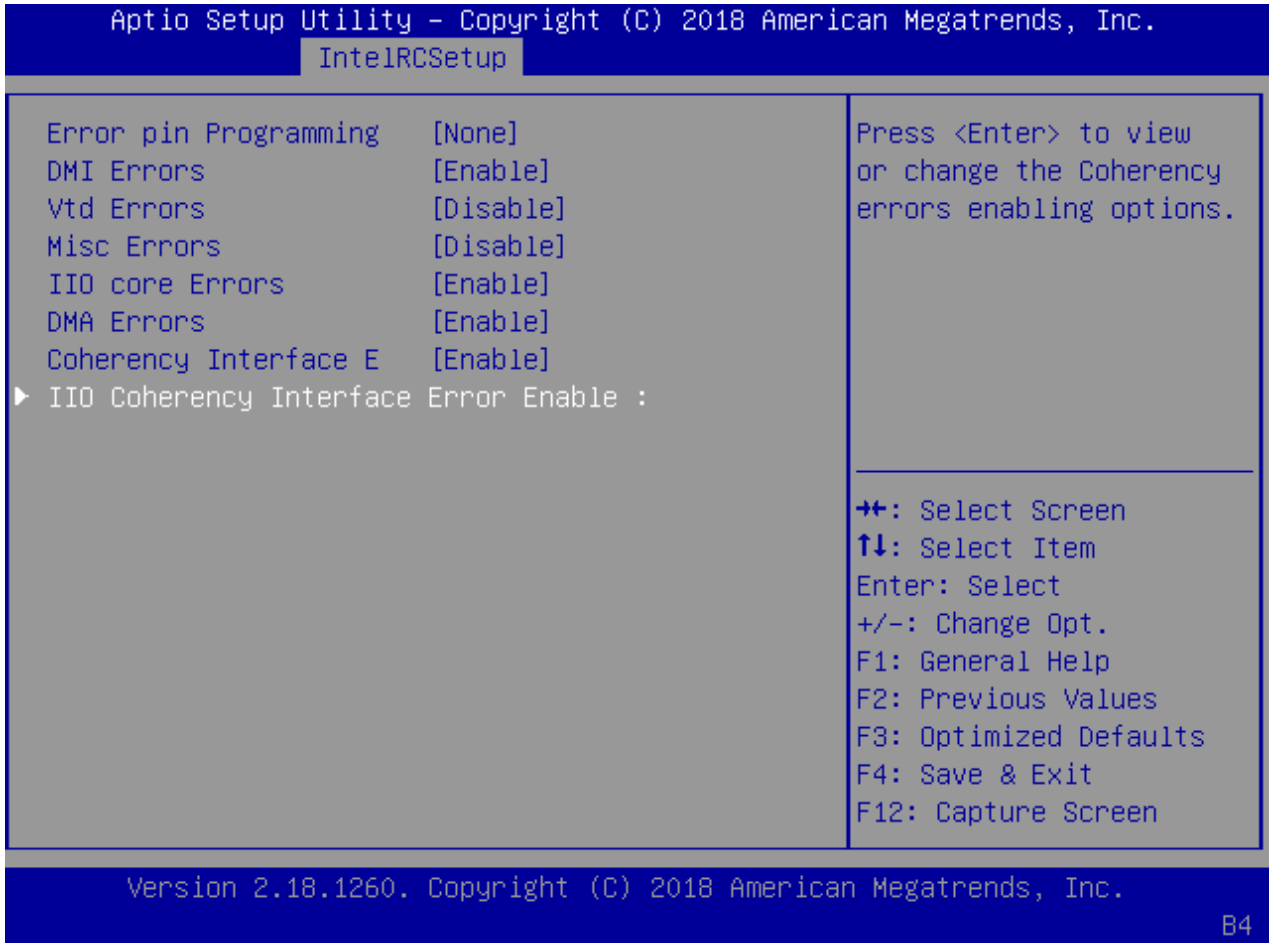
Whea Settings



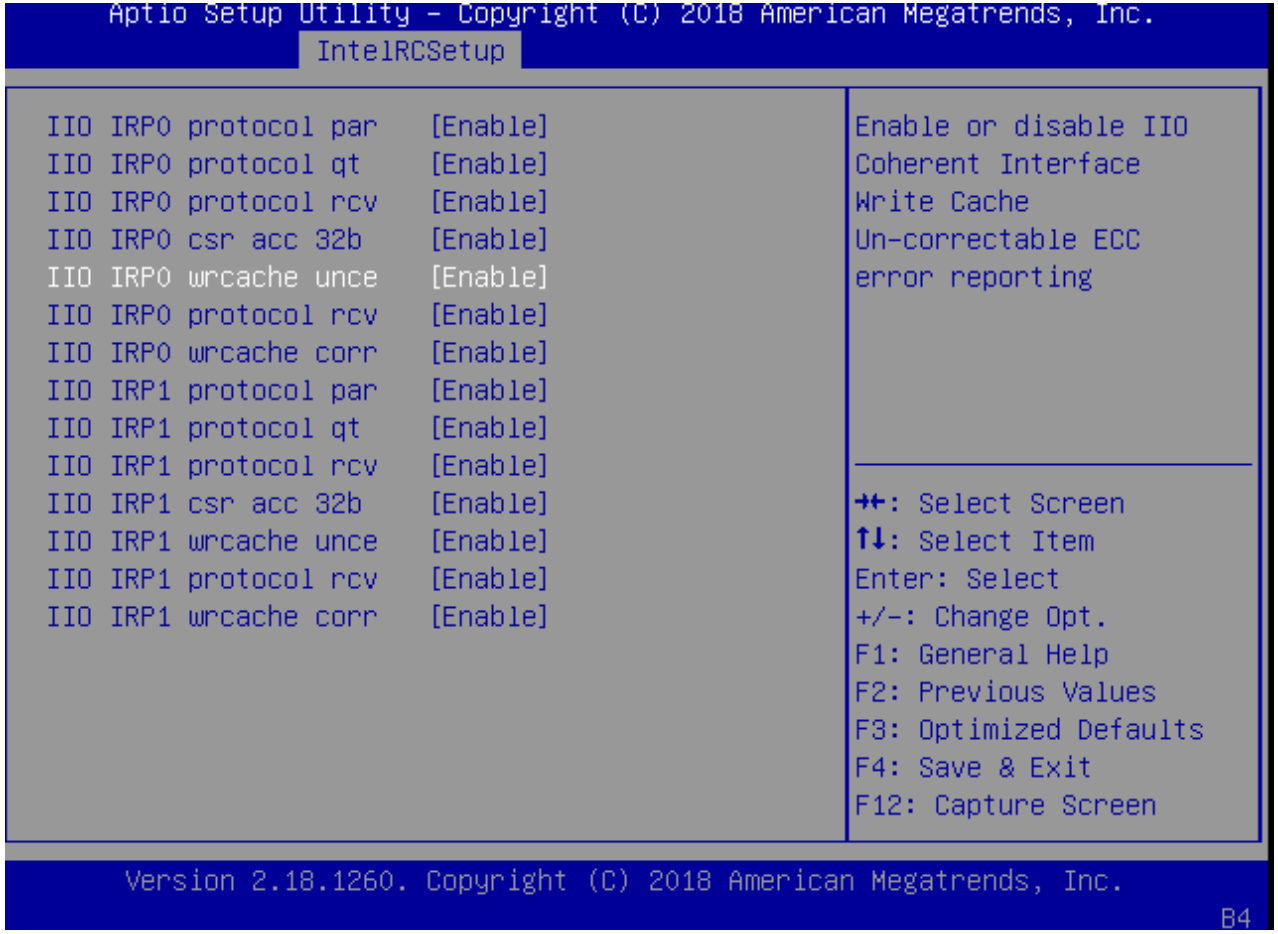
Memory Error Enabling



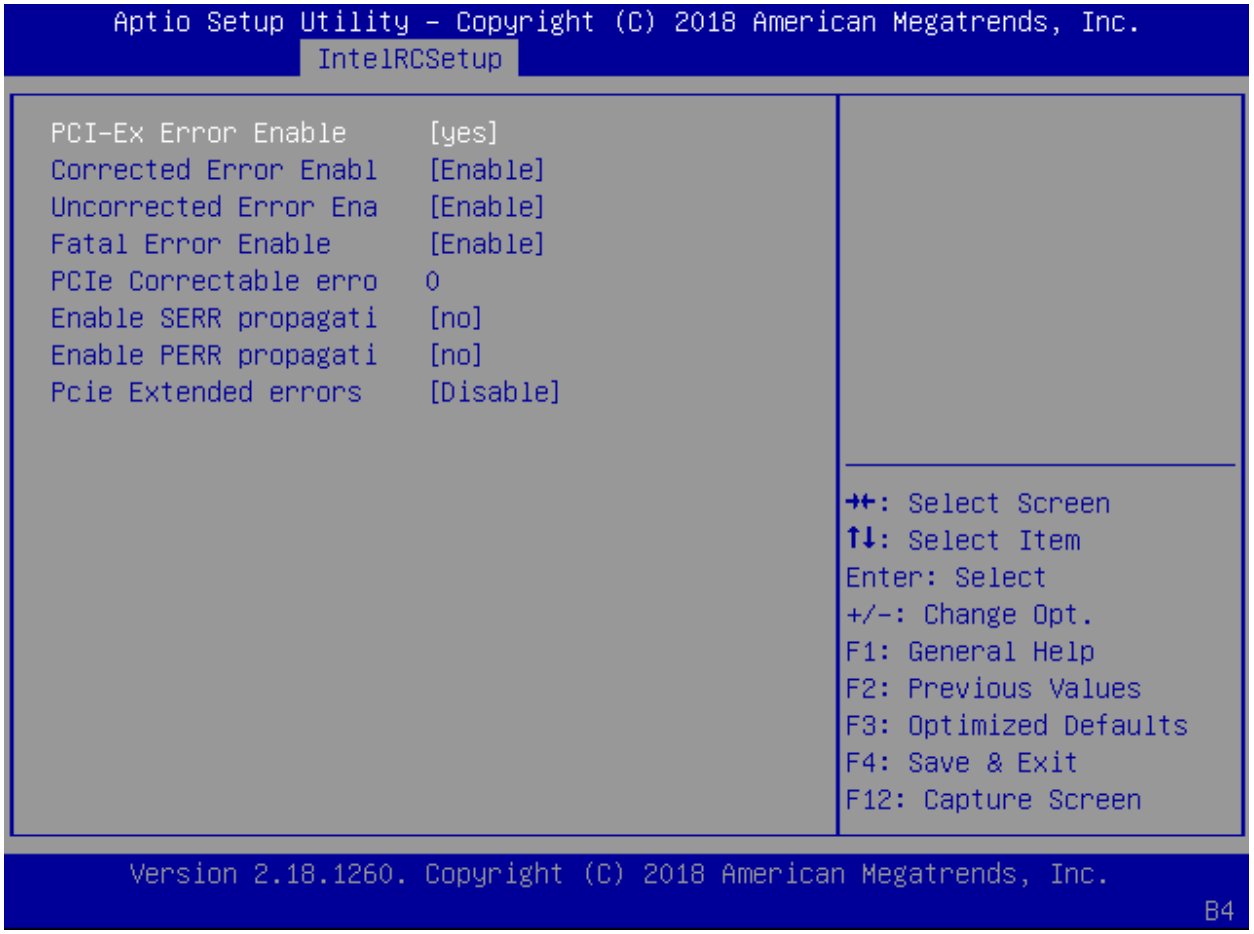
IIO Error Enable



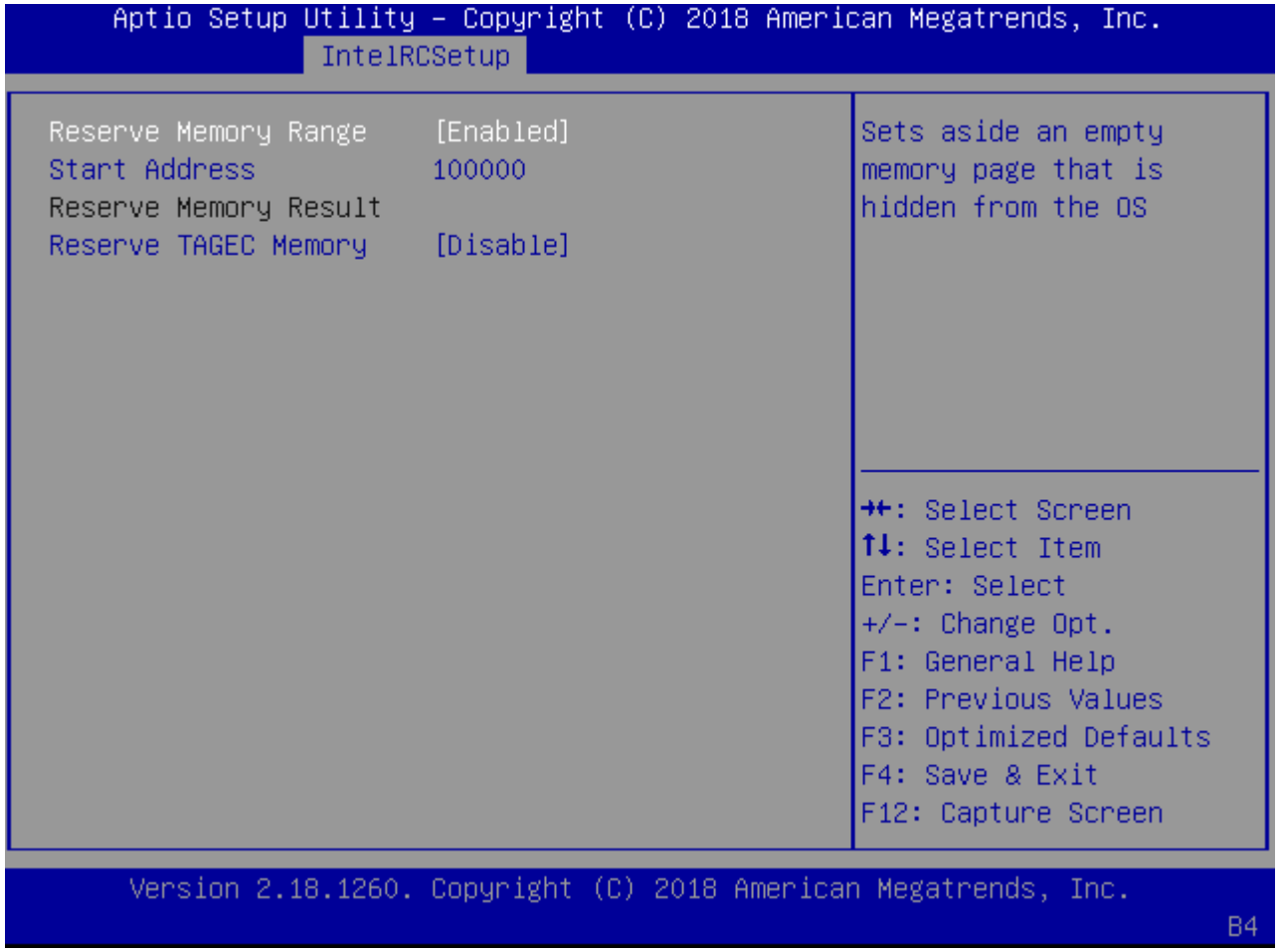
IIO Coherency Interface Error Enable



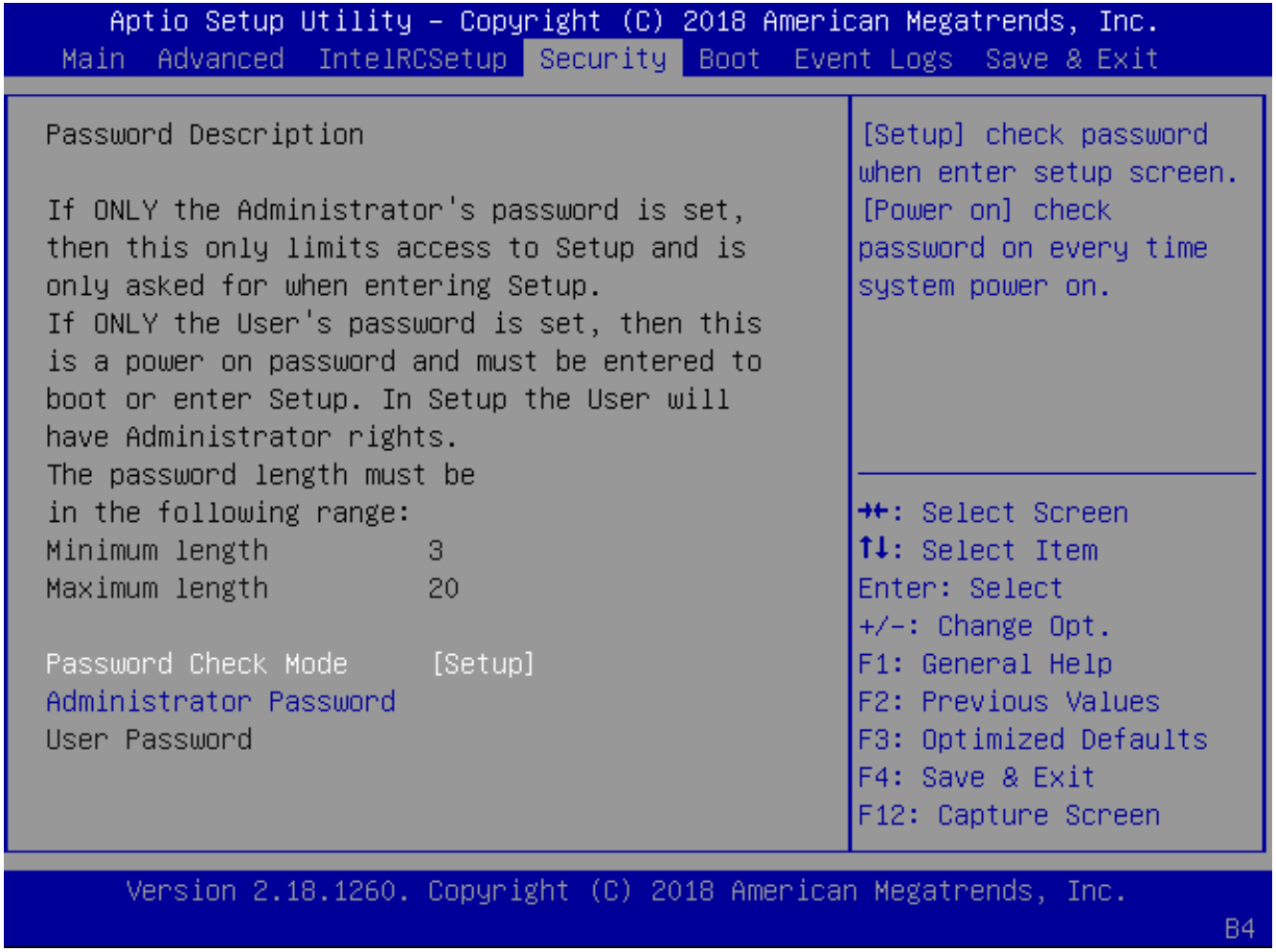
PCI/PCI Error Enabling



Reserve Memory



6.5 Security


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
Main Advanced IntelRCSetup Security Boot Event Logs Save & Exit
Password Description
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup.
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights.
The password length must be in the following range:
Minimum length 3
Maximum length 20
Password Check Mode [Setup]
Administrator Password
User Password
[Setup] check password when enter setup screen. [Power on] check password on every time system power on.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.
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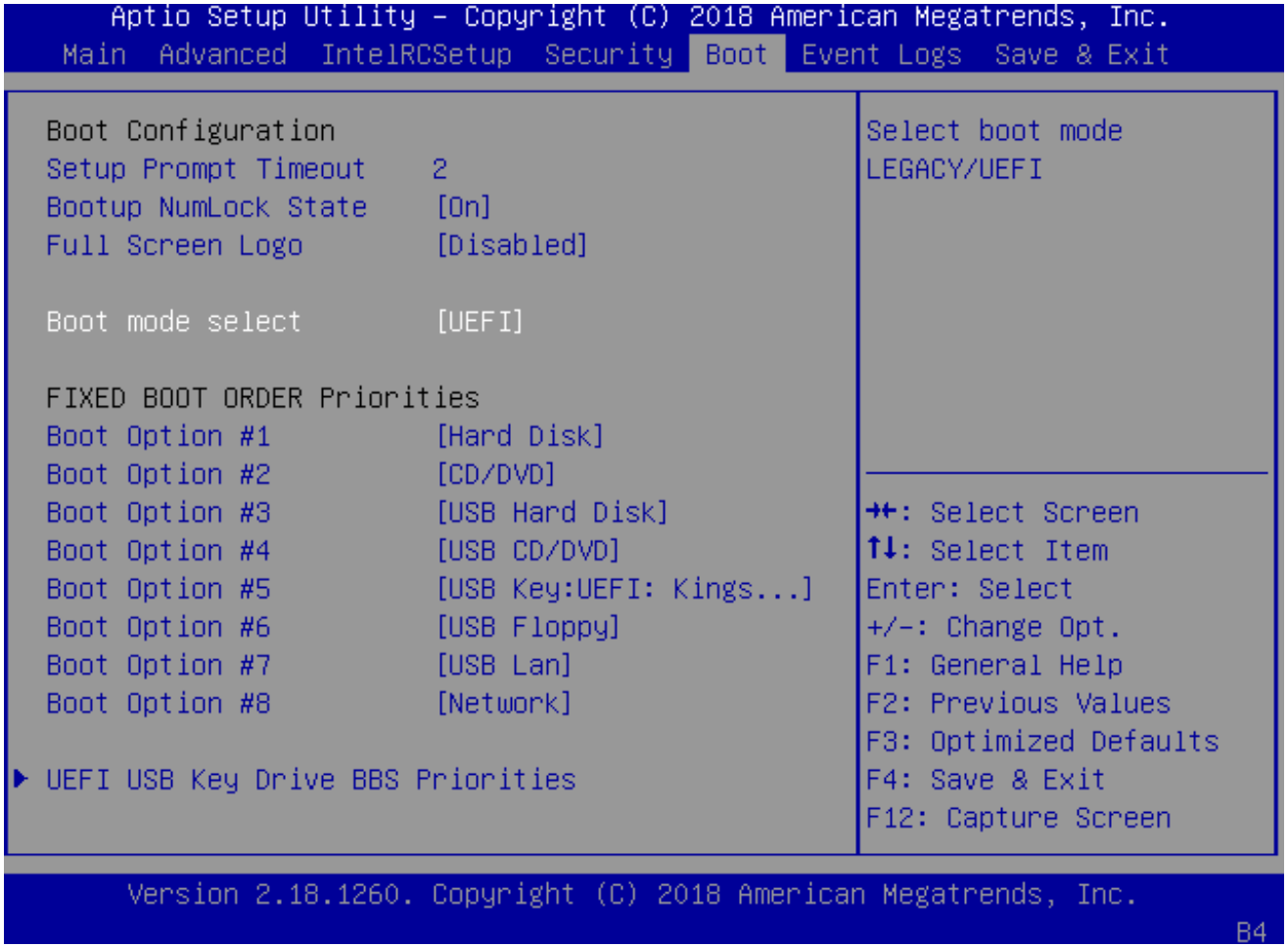
6.6 Boot


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
Main Advanced IntelRCSetup Security Boot Event Logs Save & Exit
Boot Configuration
Setup Prompt Timeout 2
Bootup NumLock State [On]
Full Screen Logo [Disabled]
Boot mode select [UEFI]
FIXED BOOT ORDER Priorities
Boot Option #1 [Hard Disk]
Boot Option #2 [CD/DVD]
Boot Option #3 [USB Hard Disk]
Boot Option #4 [USB CD/DVD]
Boot Option #5 [USB Key:UEFI: Kings...]
Boot Option #6 [USB Floppy]
Boot Option #7 [USB Lan]
Boot Option #8 [Network]
UEFI USB Key Drive BBS Priorities
Select boot mode
LEGACY/UEFI
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.
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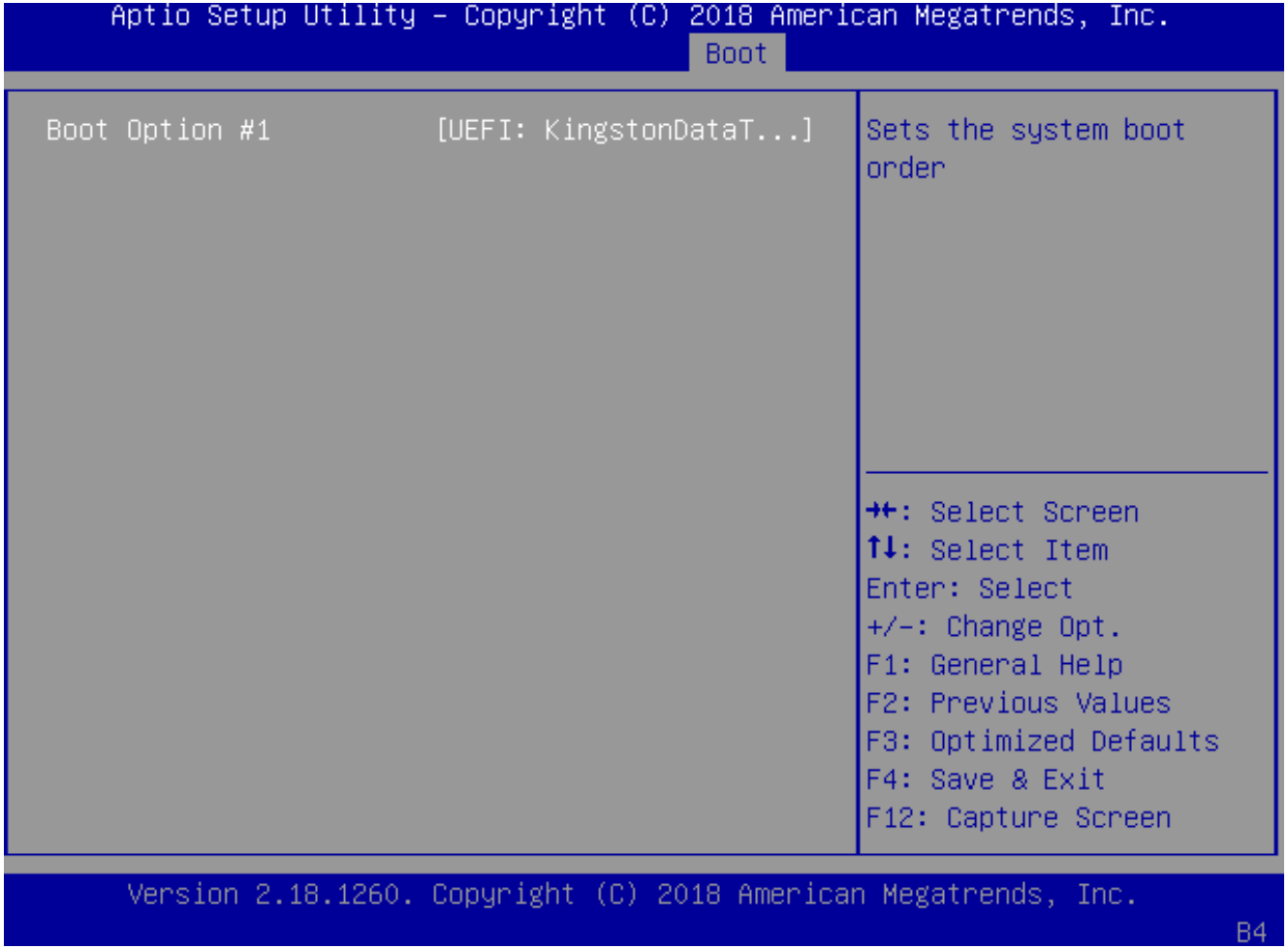
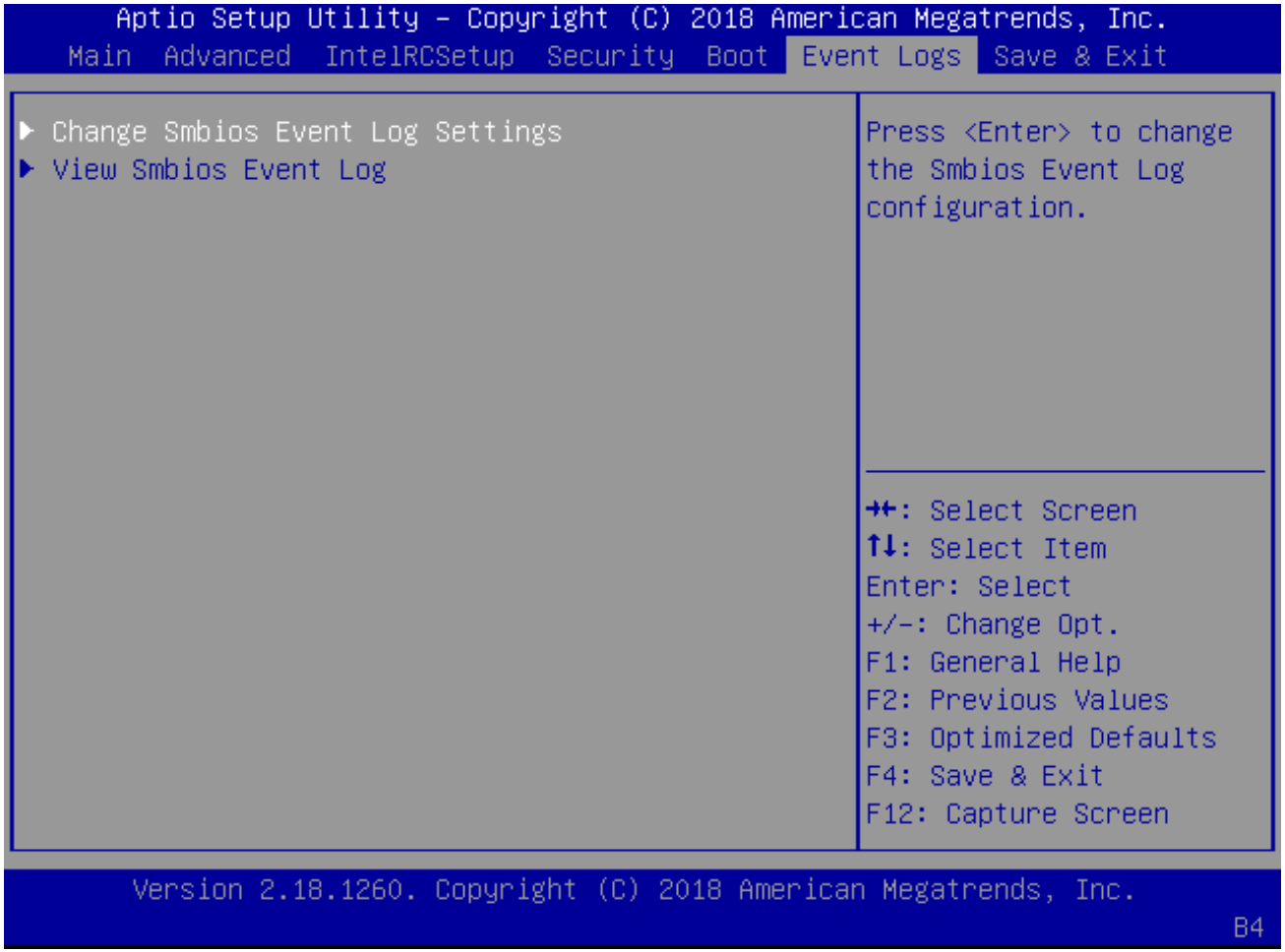
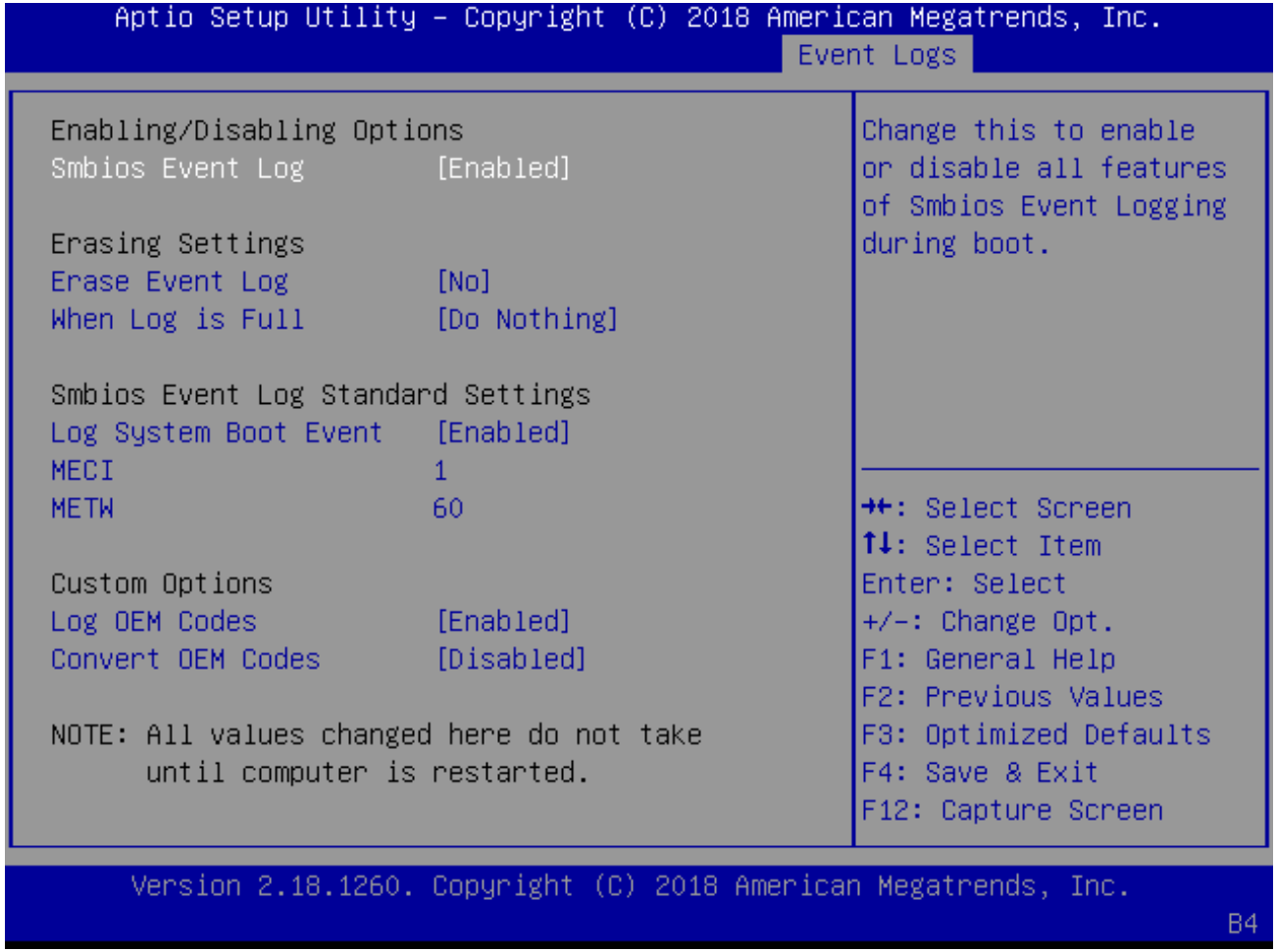
UEFI USB key Drive BBS Priorities



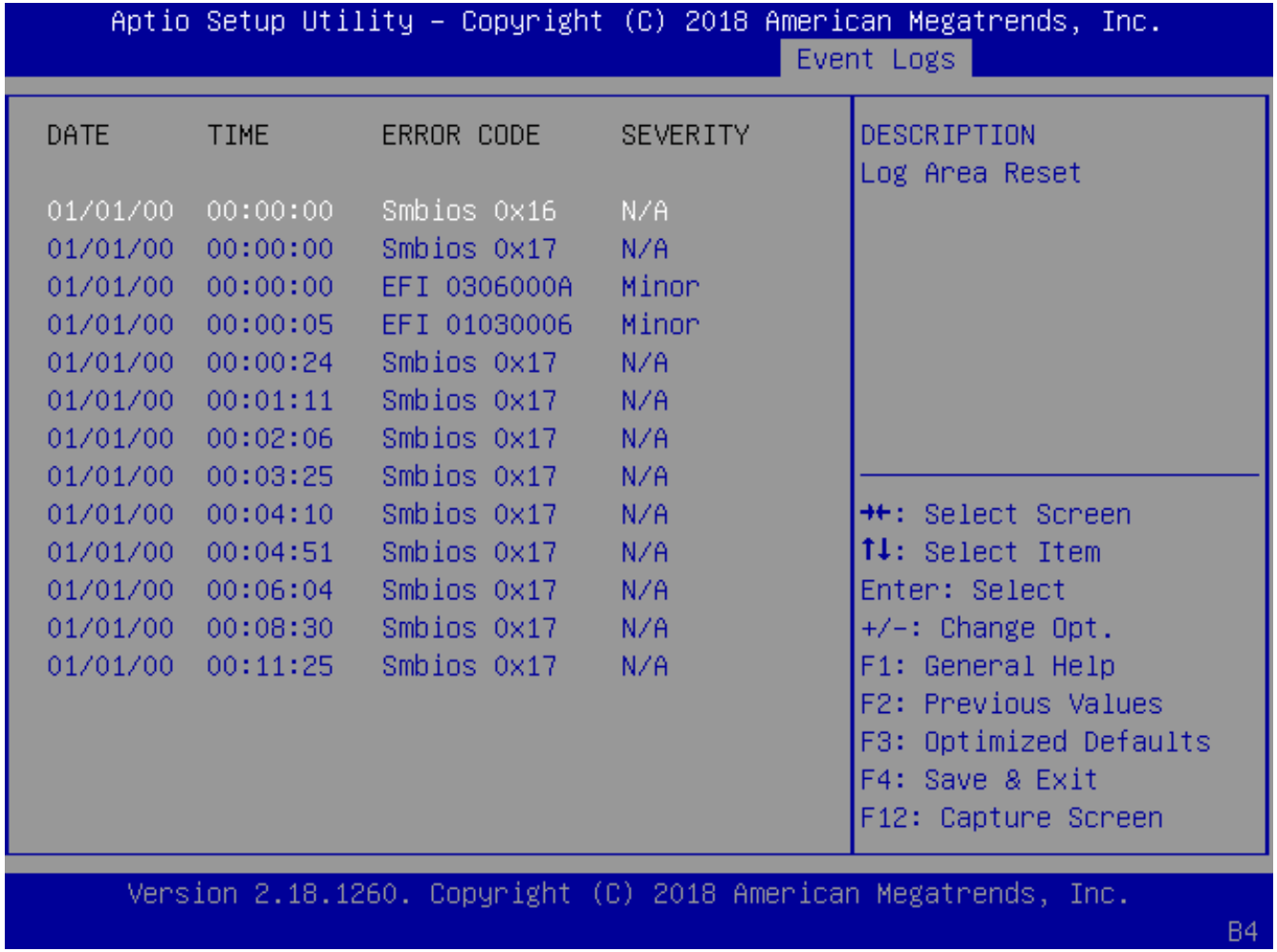
6.7 Event Logs



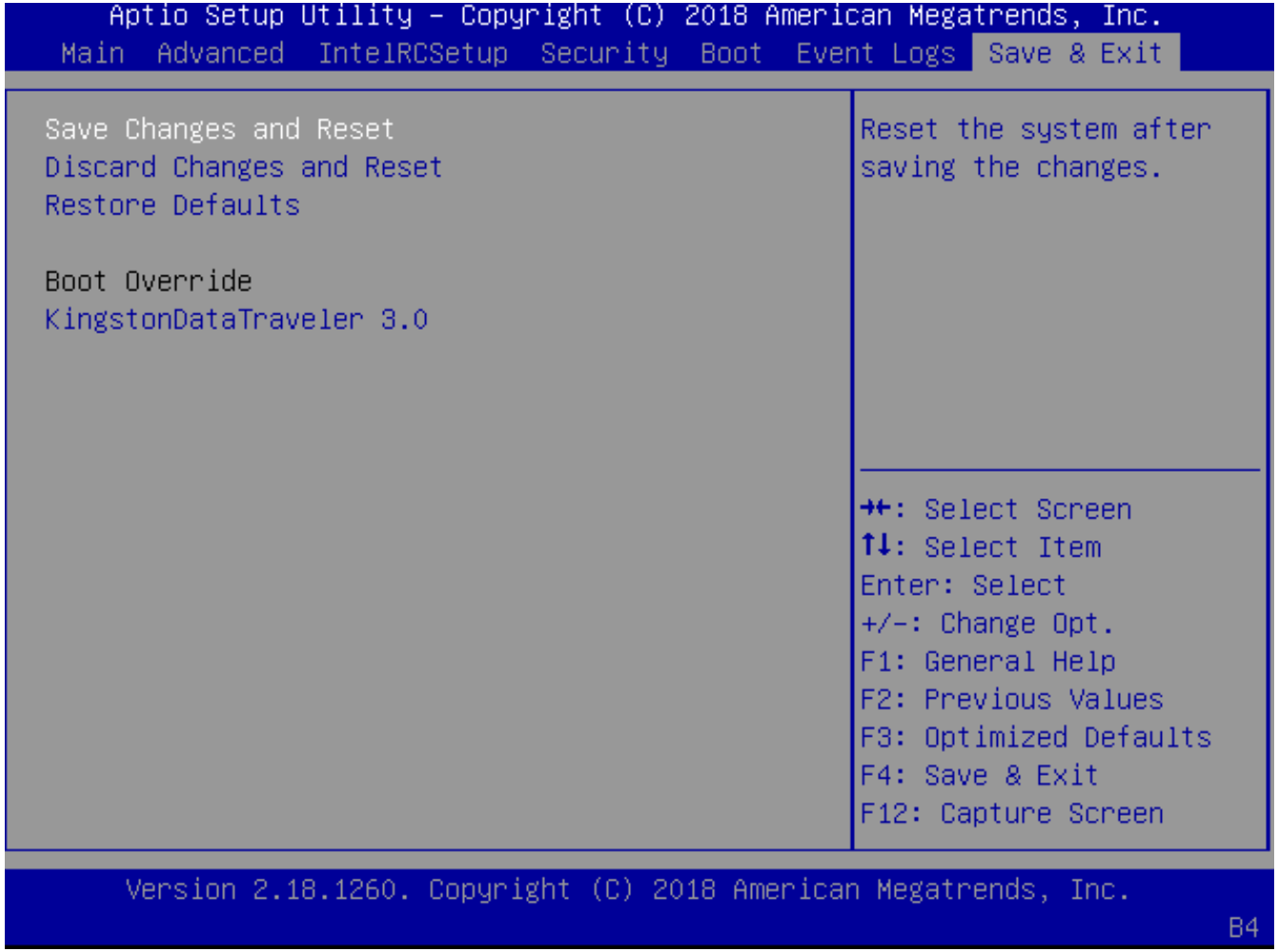
Change Smbios Event Log Settings



View Smbios Event Log



6.8 Save & Exit


Aptio Setup Utility – Copyright (C) 2018 American Megatrends, Inc.
Main Advanced IntelRCSetup Security Boot Event Logs Save & Exit
Save Changes and Reset
Discard Changes and Reset
Restore Defaults
Boot Override
KingstonDataTraveler 3.0
Reset the system after saving the changes.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
F12: Capture Screen
Version 2.18.1260. Copyright (C) 2018 American Megatrends, Inc.
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7 System Resources

LPC

Device	I/O Address	Note
Embedded Controller (ITE8528)	0x6E / 0x6F	EC Address
	0x62 / 0x66	EC ACPI CMD Port
	0x200 / 0x201	EC BRAM Port for I2C function
	0x1300~0x13FF	EC LPC IO Space
	0x3F8~0x3FF	EC UART1
	0x2F8~0x2FF	EC UART2
Carrier SIO	0x2E / 0x2F	W83627UGH Address
	0x3F0~0x3F8	SIO UART1
	0x2F0~0x2F8	SIO UART3

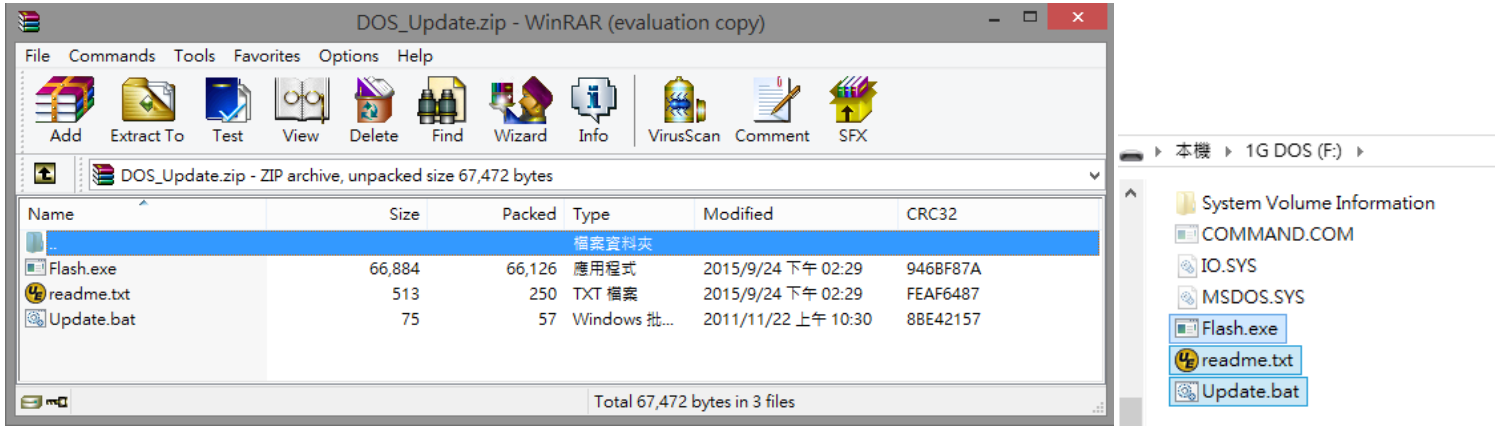
Table 12 System Resources

8 BIOS Update

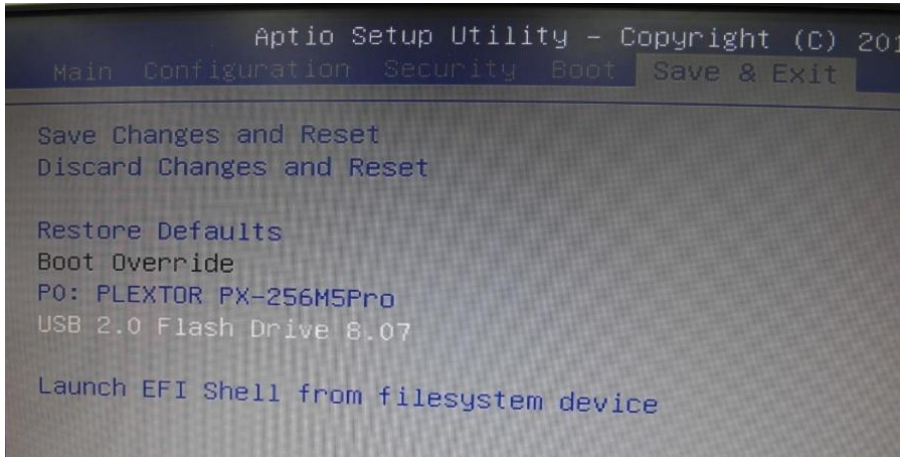
BIOS/EC DOS Update SOP process

Step 1. Create a DOS USB DOK. (Must be FAT or FAT32 format).

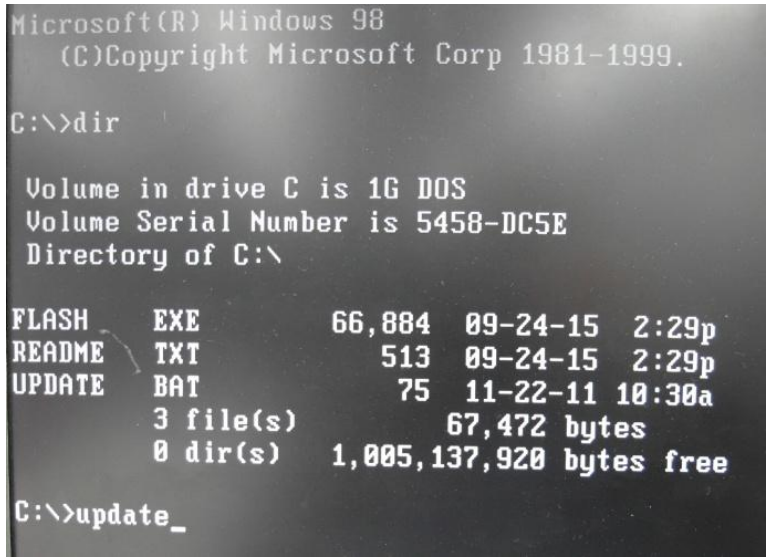
Step 2. Unzip update file to the DOS USB DOK.



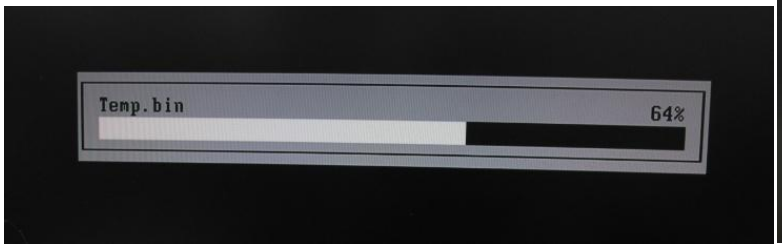
Step 3. Plug the DOS USB DOK into the target system and boot from the DOS USB DOK.

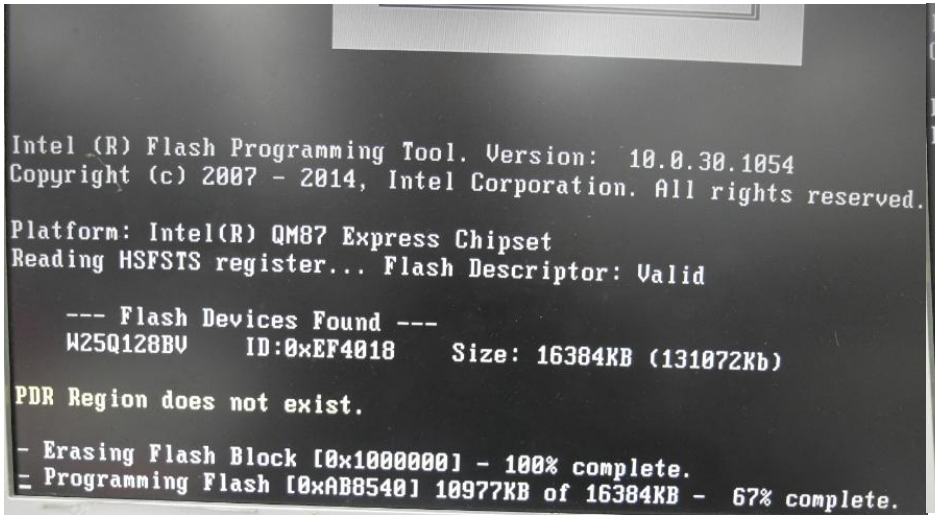


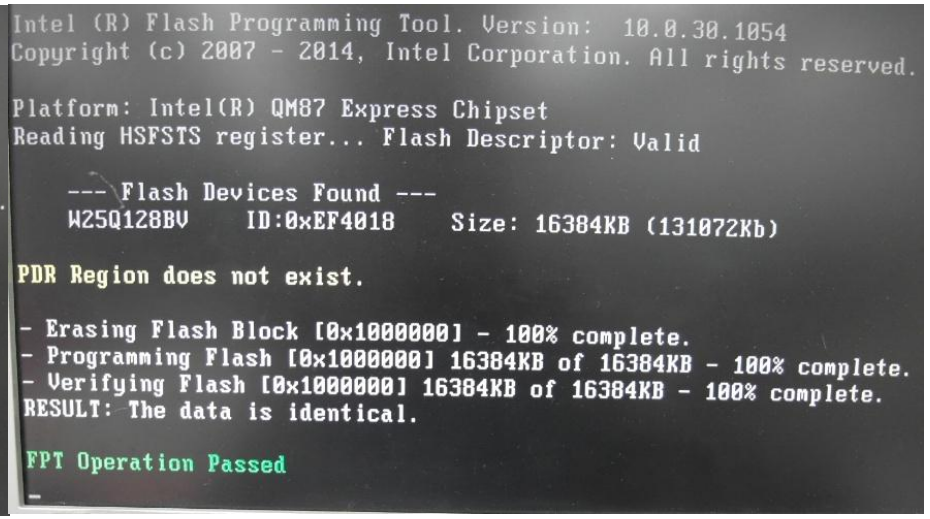
Step 4. Under the update file folder, type command : "update" and press enter.



Step 5. The update process will start and you can see the updating progress. Once finished, please power off and restart the system.





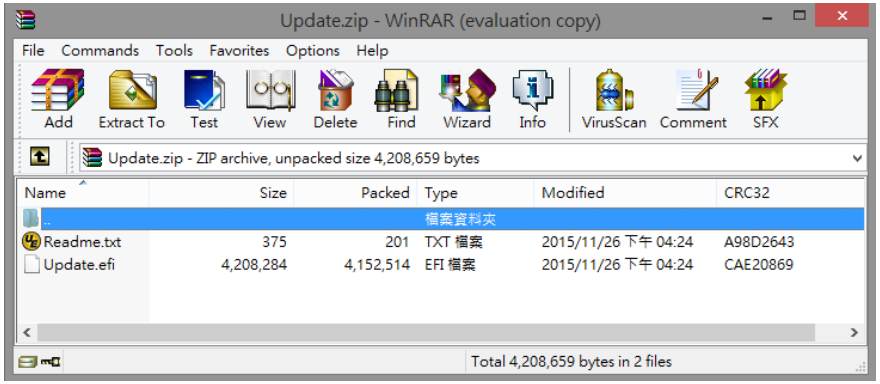


<End of BIOS/EC DOS update process>

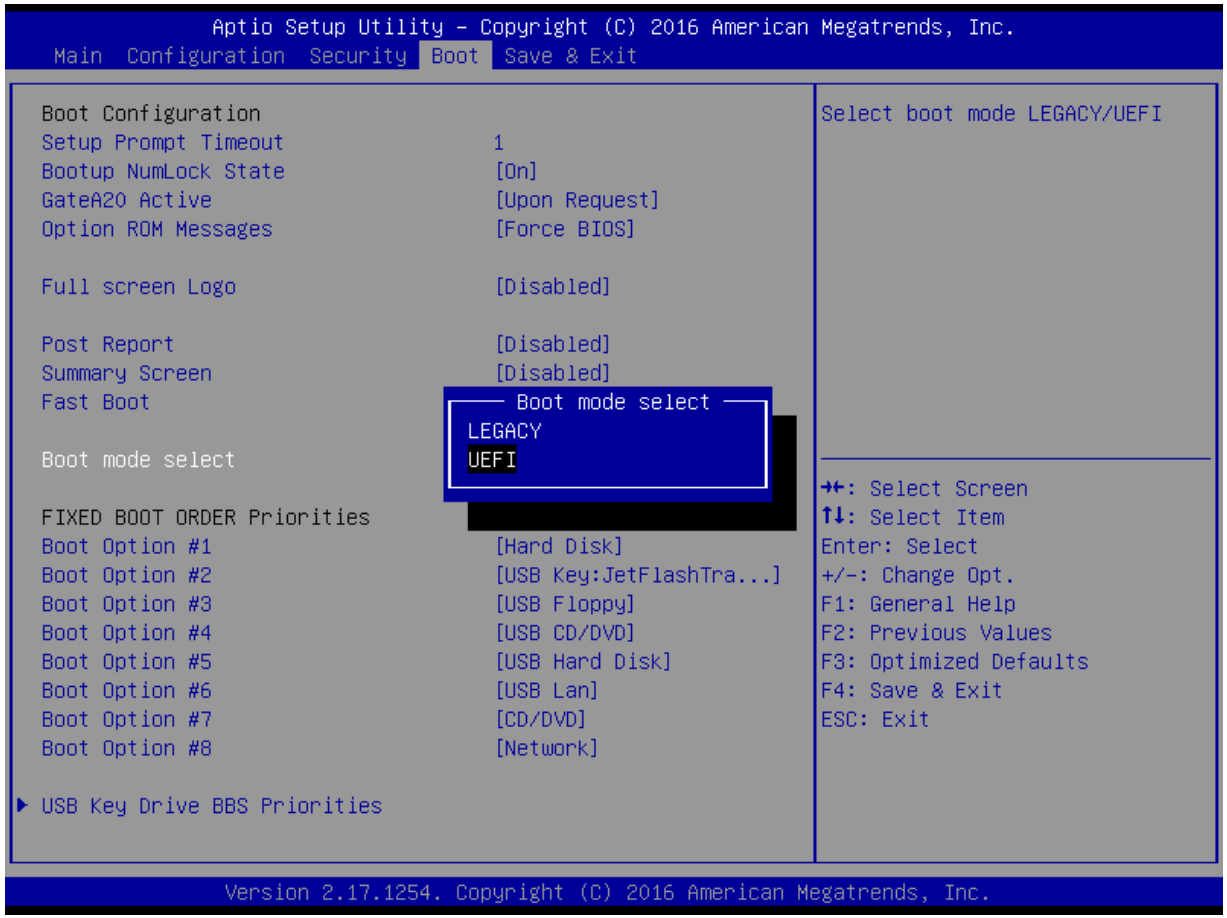
BIOS/EC UEFI Update SOP process

Step 1. Prepare a USB DOK. (Must be FAT or FAT32 format).

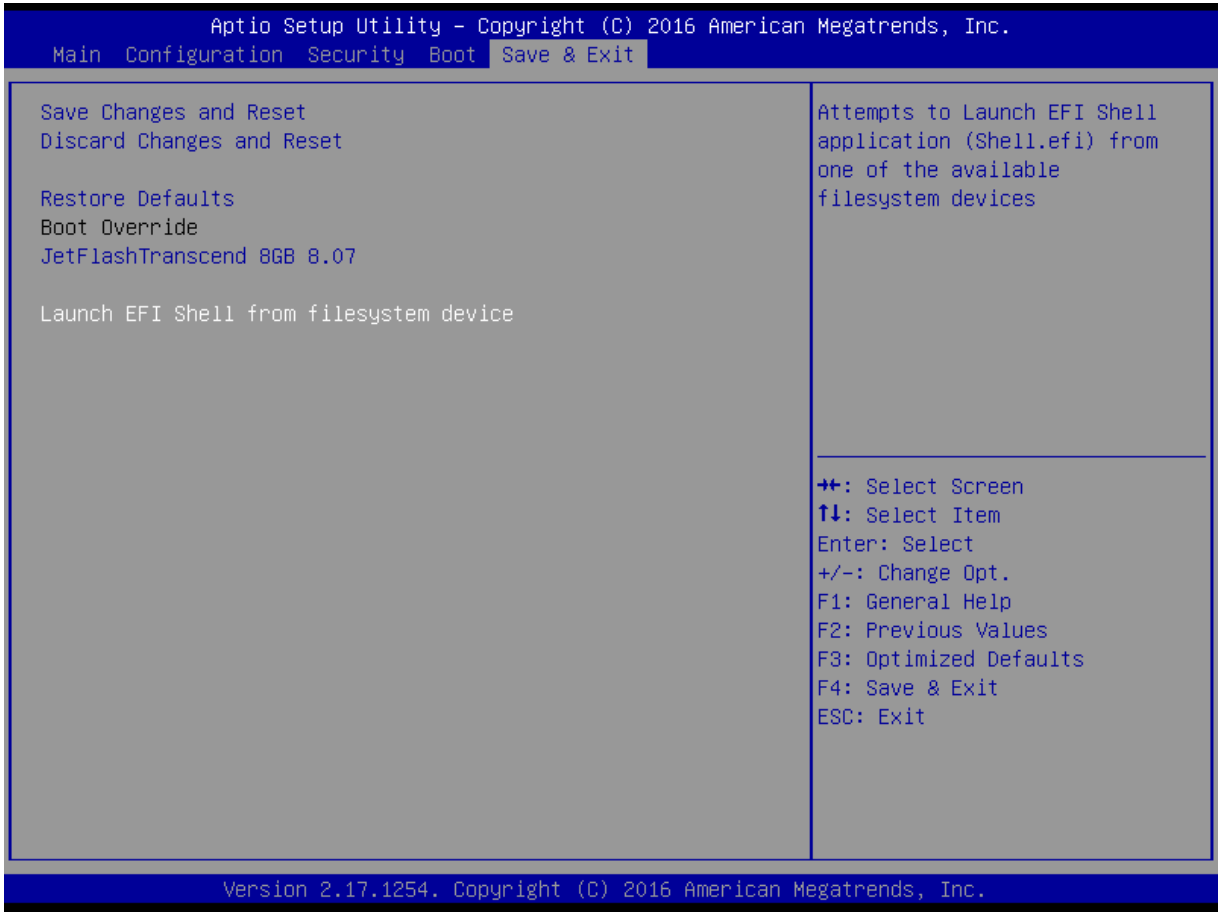
Step 2. Unzip update file to the USB DOK.



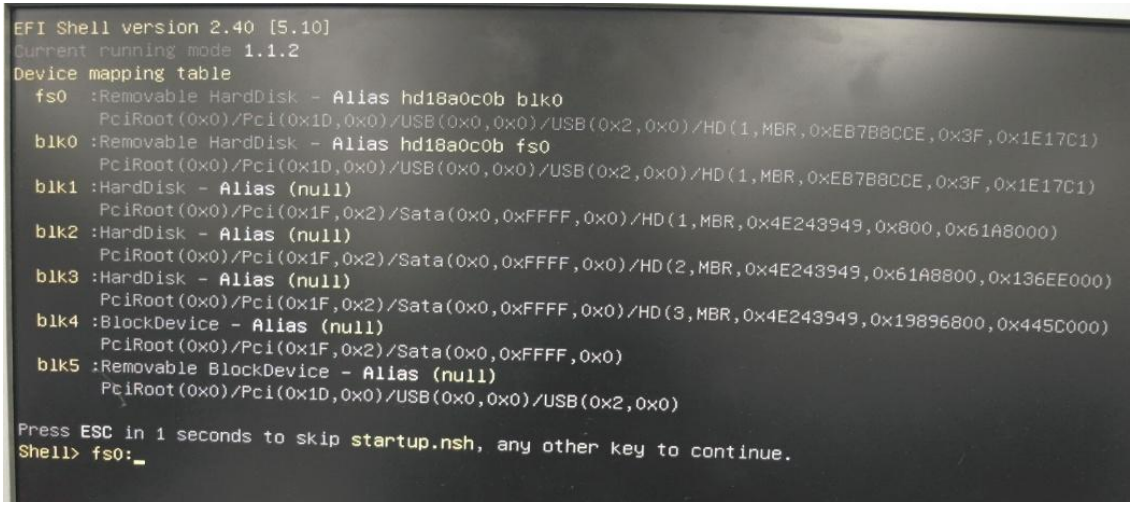
Step 3. Select UEFI boot mode in the BIOS boot menu and save, then restart the system.

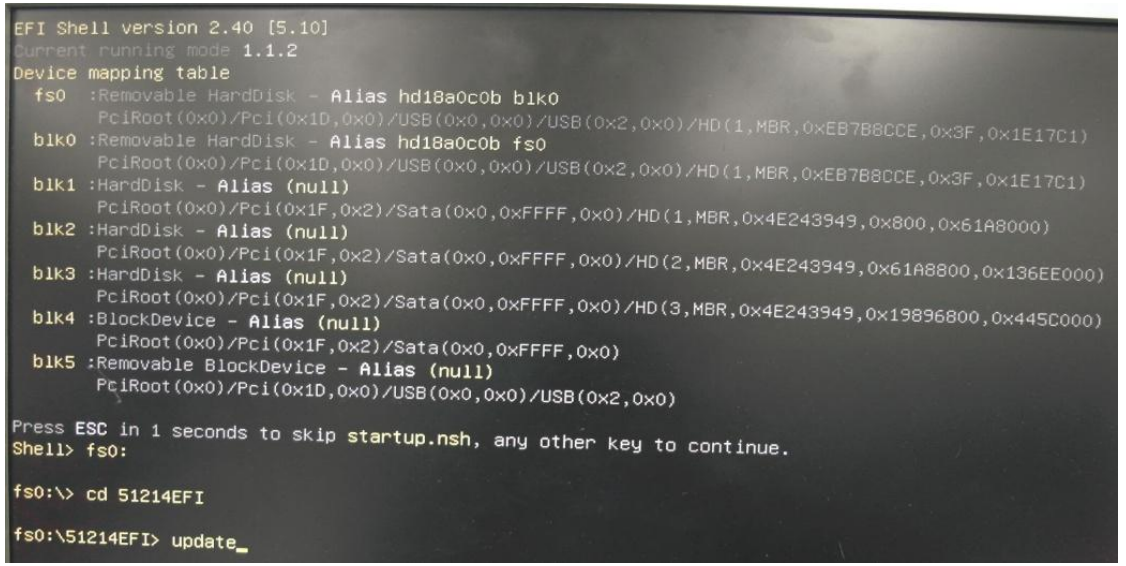


Step 4. Plug the USB DOK into the target system and boot from UEFI Shell.

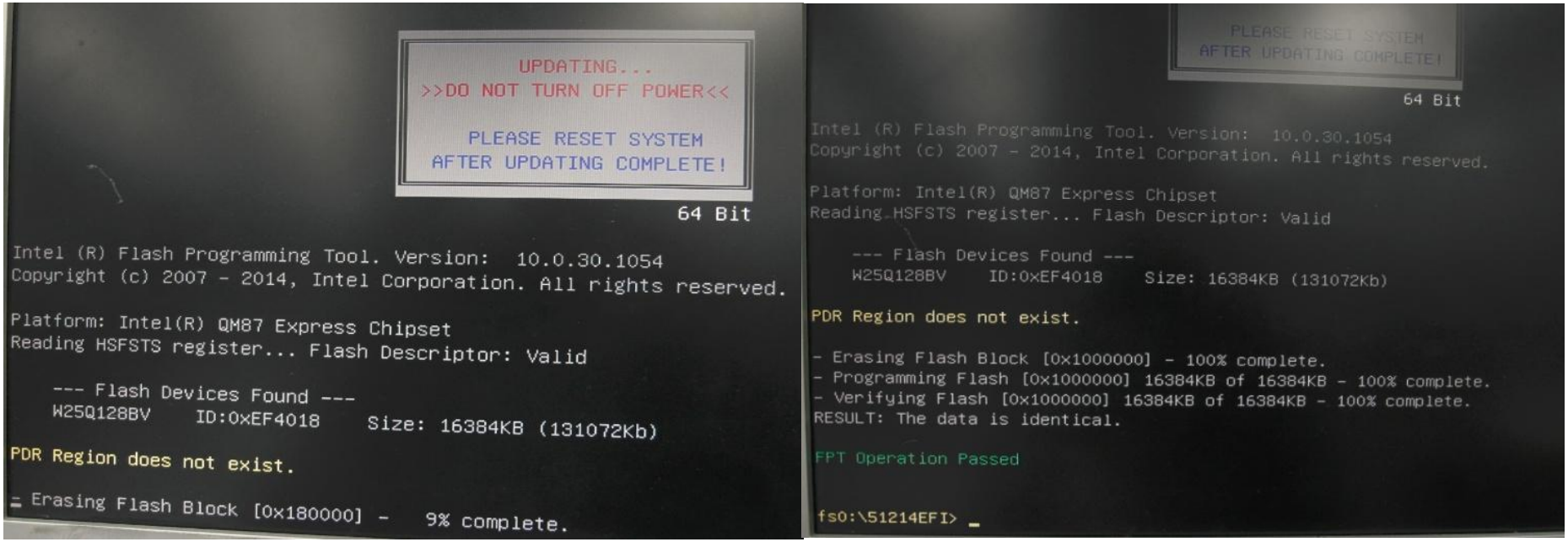


Step 5. Under the UEFI shell, direct to your USB DOK, below is an example uses fs0. Then direct to the folder with updated file and type command : "update" and press enter.





Step 6. The updating process will start and you can see the updating progress. Once finished, please power off and restart the system.



<End of BIOS/EC UEFI update process>

9 PORTWELL Software Tool

PORTWELL Evaluation Tool (PET)

The PORTWELL Evaluation Tool (PET) is an API which PORTWELL's customers can access the GPIO, I2C, SMBus, etc under Windows and Linux OS. For more information please contact PORTWELL.

PORTWELL BIOS web Tool (PBT)

The PORTWELL BIOS web Tool (PBT) is a brand new on-line utility innovated by PORTWELL. PBT now is available for PORTWELL's premiere customers who are able to add customized BIOS logo and change BIOS default settings on American Megatrends (AMI) BIOS. Please contact PORTWELL for more information.

PORTWELL EC Auto Test Tool (PECAT)

The PORTWELL EC Auto Test Tool (PECAT) is a brand new utility innovated by PORTWELL. PECAT now is available for PORTWELL's premiere customers, who are able to Test Embedded Controller Function in UEFI Mode. Please contact PORTWELL for more information.

10 Industry Specifications

The list below provides links to industry specifications that apply to PORTWELL modules.

Low Pin Count Interface Specification, Revision 1.0 (LPC) http://www.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0 http://www.usb.org/home
PCI Specification, Revision 2.3 https://www.pcisig.com/specifications
Serial ATA Specification, Revision 3.0 http://www.serialata.org/
PICMG® COM Express Module™ Base Specification http://www.picmg.org/
PCI Express Base Specification, Revision 2.0 https://www.pcisig.com/specifications