COM Express™ PCOM-B653VGL

User's Guide Rev 2.0

Revision History

R0.1	Preliminary
R0.2	Update BIOS and Tables information
R1.0	Initial release
R2.0	Update Display and Part number

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1 Introduction

This PCOM-B653VGL User's Guide contains detail information of the productspecifications, features, mechanical dimensions, heat sink/cooler and BIOS Setup.

PCOM-B653VGL is designed according to COM (Computer On Module) PICMG Open Modular Computing Standards COM Express™ Specification Rev3.0 Type 6 and Compact form factor (95x95cm).

PCOM-B653VGL, a COM Express Module with Intel 8th Generation processor code name Whiskey lake U. PCOM-B653VGL is the successor of PCOM-B644VG (Intel Kabylake U platform) targeted on Ultra low power processors 15W, 1-Chip processor includes a Platform Controller Hub (PCH) on the same die and suitable for wide working temperature from 0°C to +60°C. PCOM-B653VGL supports dual channel DDR4 memory. Display interfaces are VGA, LVDS, dual DDI and DP display with 4K x 2K high resolution display.

2 Block Diagram

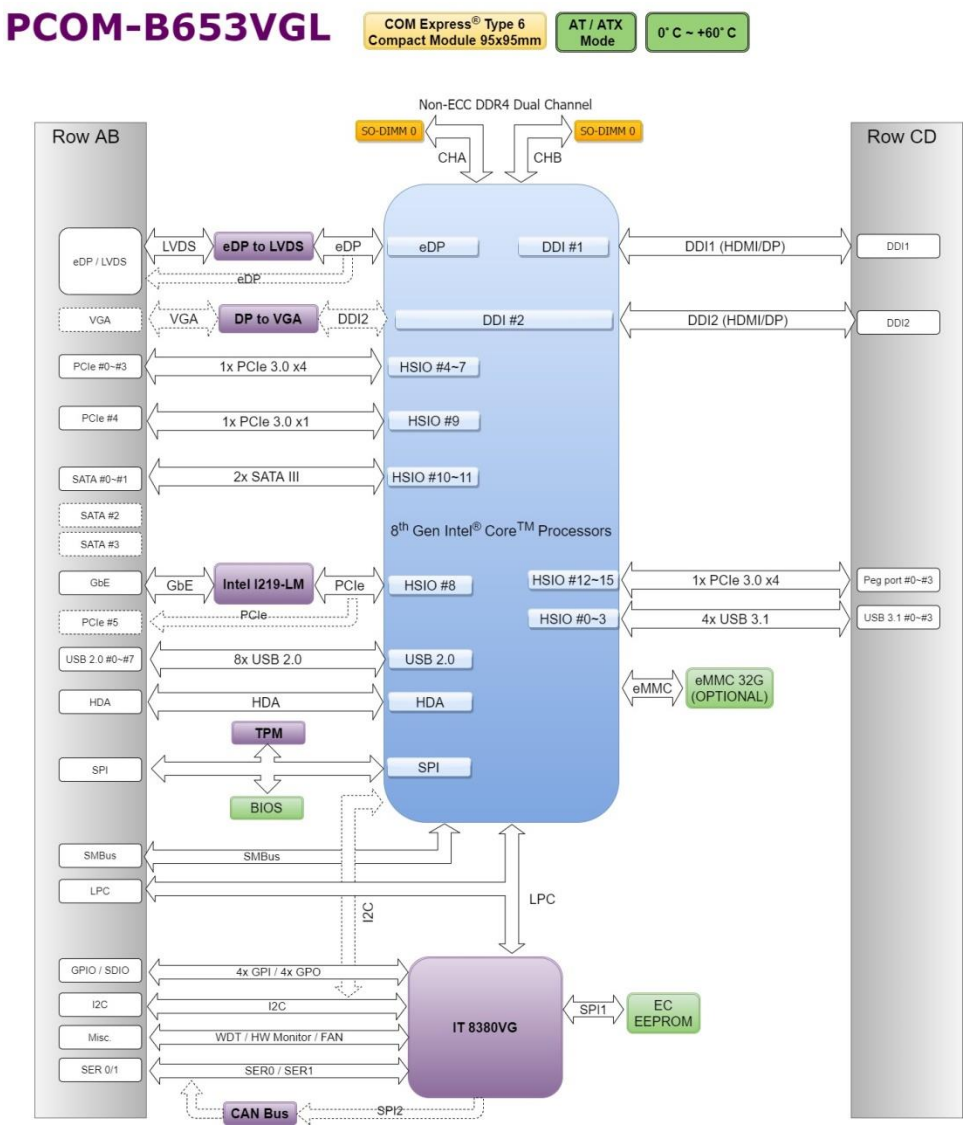


Figure 1 PCOM-B653VGL Block Diagram

3 Specifications

General				
Product	PCOM-B653VGL			
Form Factor	COM Express® Type 6 Compact Rev. 3.0			
Processor	Intel® Core™			Intel® Celeron®
	i7-8665UE	i5-8365UE	i3-8145UE	4305UE
Core	4	4	2	2
Freq.	1.70 GHz	1.60 GHZ	2.20 GHz	2.00 GHz
Turbo	4.40 GHz	4.10 GHz	3.90 GHz	2.00 GHz
Cache	8MB	6MB	4MB	2MB
Processor Graphics	Intel® UHD Graphics 620	Intel® UHD Graphics 620	Intel® UHD Graphics 620	Intel® UHD Graphics 610
Graphics Base Frequency	300.00 MHz	300.00 MHz	300.00 MHz	300.00 MHz
Graphics Max Dynamic Frequency	1.15 GHz	1.05 GHz	1.00 GHz	1.00 GHz
HW Encoding	H.264 AVC, MPEG2, HEVC, VP8/9, JPEG			
HW Decoding	H.264 AVC, VC1, MPEG2, VP8/9, JPEG			
HW Acceleration	DX 11.3/12, OpenGL 4.5, OpenCL 2.1			
Processor TDP	15 W	15 W	15 W	15 W
BIOS	AMI BIOS			
ECC Memory Supported	No			
Memory	2x DDR4 SODIMM sockets Dual channel Up to 64GB 2400 MT/s			

I/O Interface			
SATA	2x SATA III		
USB	4x USB 3.1 Gen2 (Port 0~3) 8x USB 2.0 (Port 0~7)		
Ethernet	1 GbE (I219-LM)		
Serial I/O	GPIO	8 GPIO (4 GPI and 4 GPO)	
	I2C	Baud Rate : 400KHz	
	SMBus	Baud Rate : 100KHz	
	UART	Only RX/TX signal	
PEG	1x PCIe Gen3 x4		
PCI Express	1x PCIe Gen3 x4 1x PCIe Gen3 x1 1x PCIe Gen3 x1 (Option)		
Display	Default	Options	Resolution
	DDI2	VGA	VGA Up to 1920x1200 @ 60Hz
		DDI2	HDMI up to 4096x2160 @ 60Hz
			DP Up to 4096x2304 @ 60Hz
	LVDS	eDP	eDP Up to 4096x2304 @ 60Hz
		LVDS	LVDS Up to 1920x1200 @ 60Hz
	DDI1	DDI1	HDMI up to 4096x2160 @ 60Hz
			DP Up to 4096x2304 @ 60Hz
Security	TPM 2.0 (Infineon SLB9670)		

Table 1 PCOM-B653VGL Specifications

3.1 Supported Operating Systems

The PCOM-B653VGL supports the following operating systems.

Vendor	Operating System	Supported
Microsoft	Windows 10 (64bit)	Yes
Linux	Ubuntu 18.04	Yes
	Fedora 31	Yes

Table 2 Supported Operating Systems

3.2 Windows OS driver

Please download the drivers from Portwell download center website http://www.portwell.tw/support/download_center.php

Item	Driver version	Windows OS
Chipset	10.1.18019.8144	Driver_PCOM-B653VGL_chipset-10.1.18019.8144-public-mup
Graphic	100.7158	Driver_PCOM-B653VGL_igfx_win10_100.7158
Ethernet(I219-LM)	12.18.8.9	Driver_PCOM-B653VGL_I219-LM
ME_Driver	1909.12.0.1236	Driver_PCOM-B653VGL_ME_Consumer_Win10_64_1909.12.0.1236

Table 3 PCOM-B653VGL Driver list

3.3 Electrical Characteristics

Input voltage	+12VDC (Nominal) +6VDC ~ +18VDC (Wide range)
RTC Battery power consumption	3.2uA
Power on mode	ATX / AT

Table 4 Electrical characteristics

3.4 Power sequence

PCOM-B653VGLPower sequence

Figure 2 Power on sequence

3.5 Circuit protection design

PCOM-B653VGL has designed Schottkydiode protection on the module for Serial Port,FAN(PWMOUT & TACHIN), LID and SLEEP. Considerations must be taken while designing carrier board.

*Note : Pull up voltage VCC is 5V.

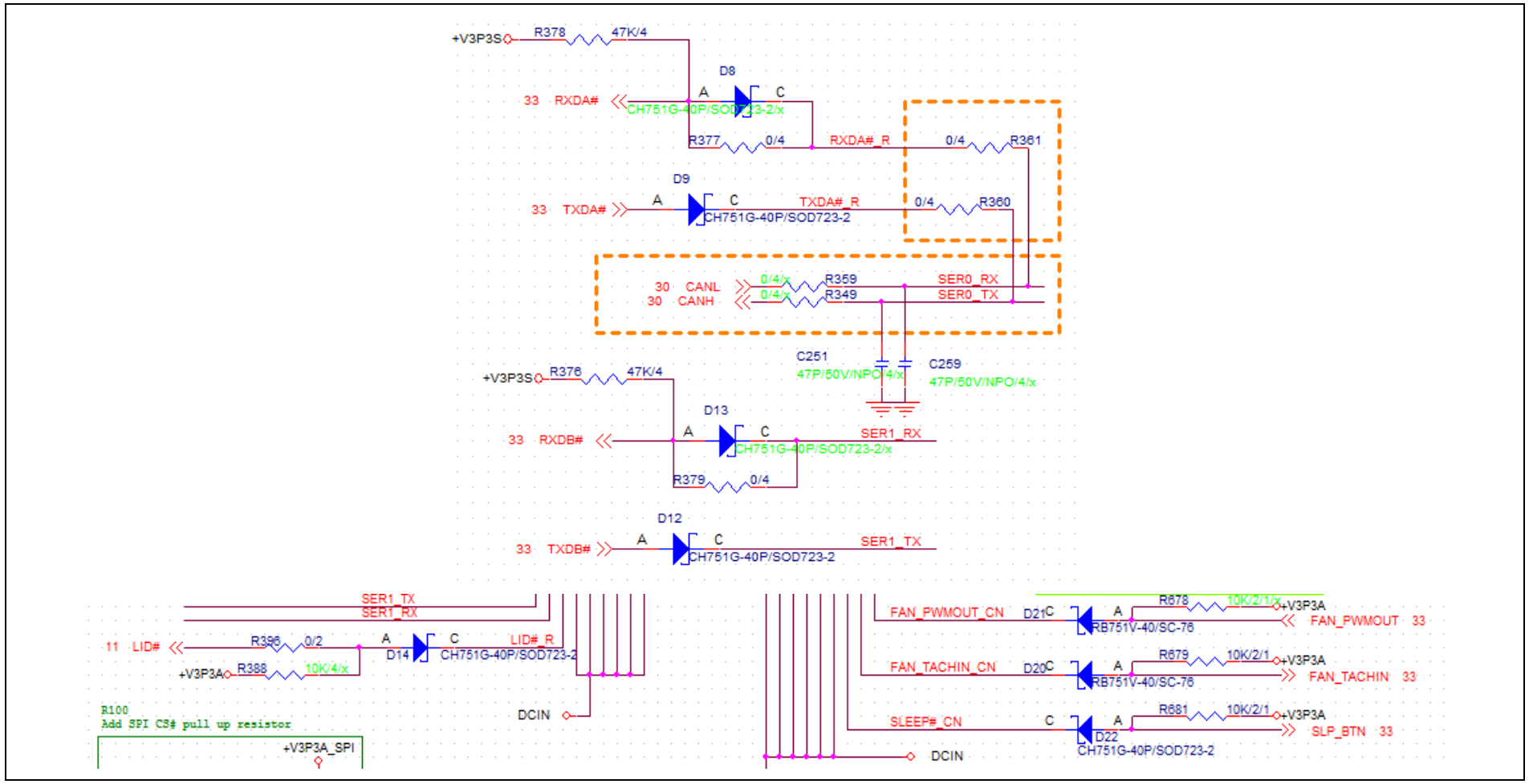


Figure 3 Circuit protection design

3.6 Mechanical Dimensions

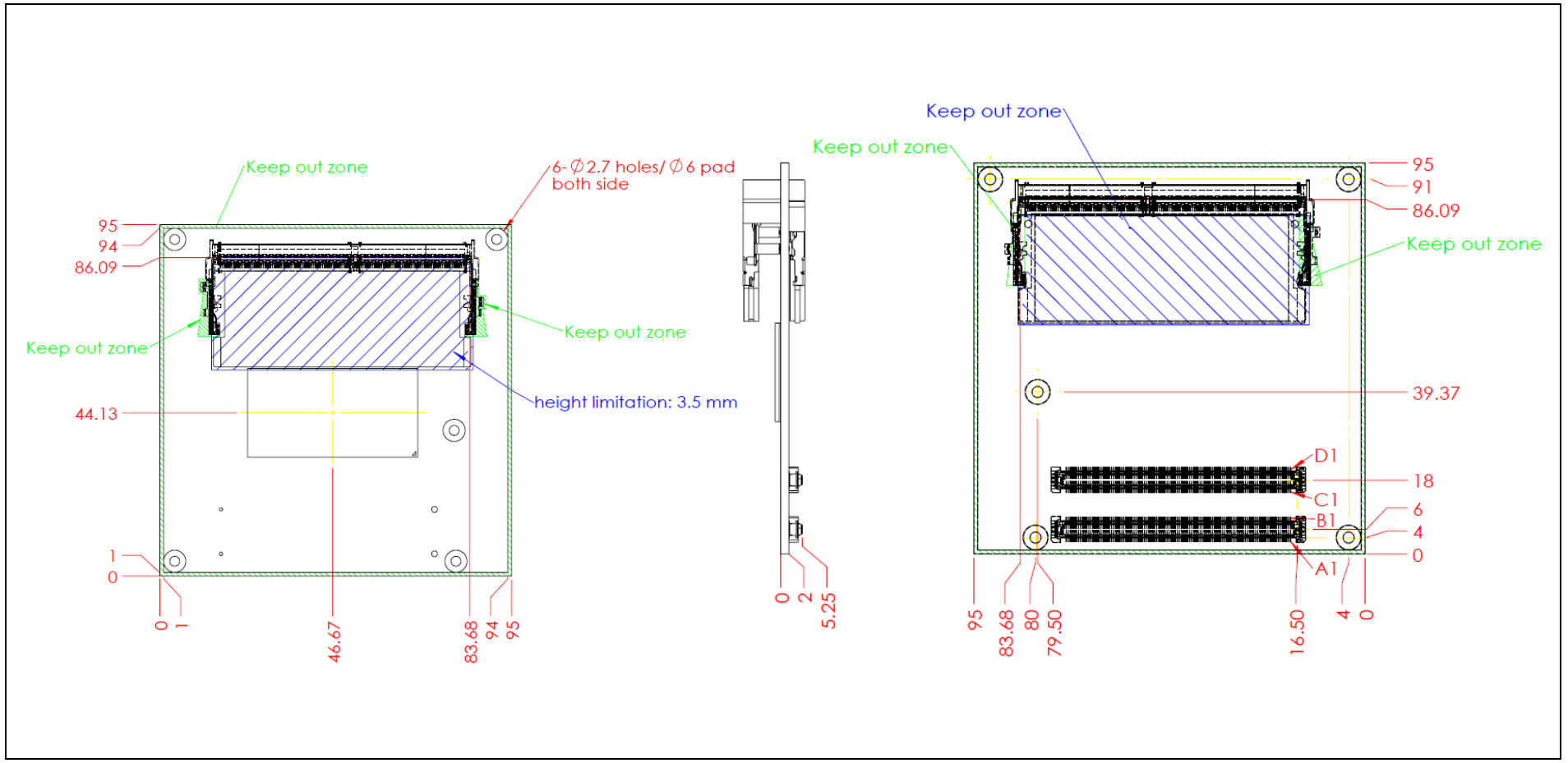


Figure 4 Mechanical Dimensions - Top & BOT & Assembly

3.7 Module and HS weight

Weight

Module	80.0g
Cooler (H/S+FAN)	165g
Accessory (Screws & Stand-off)	17g

Table 5 Module and AccessoryWeight

3.8 Environmental Specifications

Storage Temperature	0~60°C
Operation Temperature	0~60°C
Storage Humidity	0%~95%
Operation Humidity	0%~95%

Table 6 Environmental Specifications

3.9 Optional function rework SOP

1. Optional function rework SOP : eDP

PCOM-B653VGL Default display is LVDS, rework following SOP for eDP display interface.

- Step 1

Remove below resistors and caps :
C329,C333,C142,C143,C144,C145,R258,R726

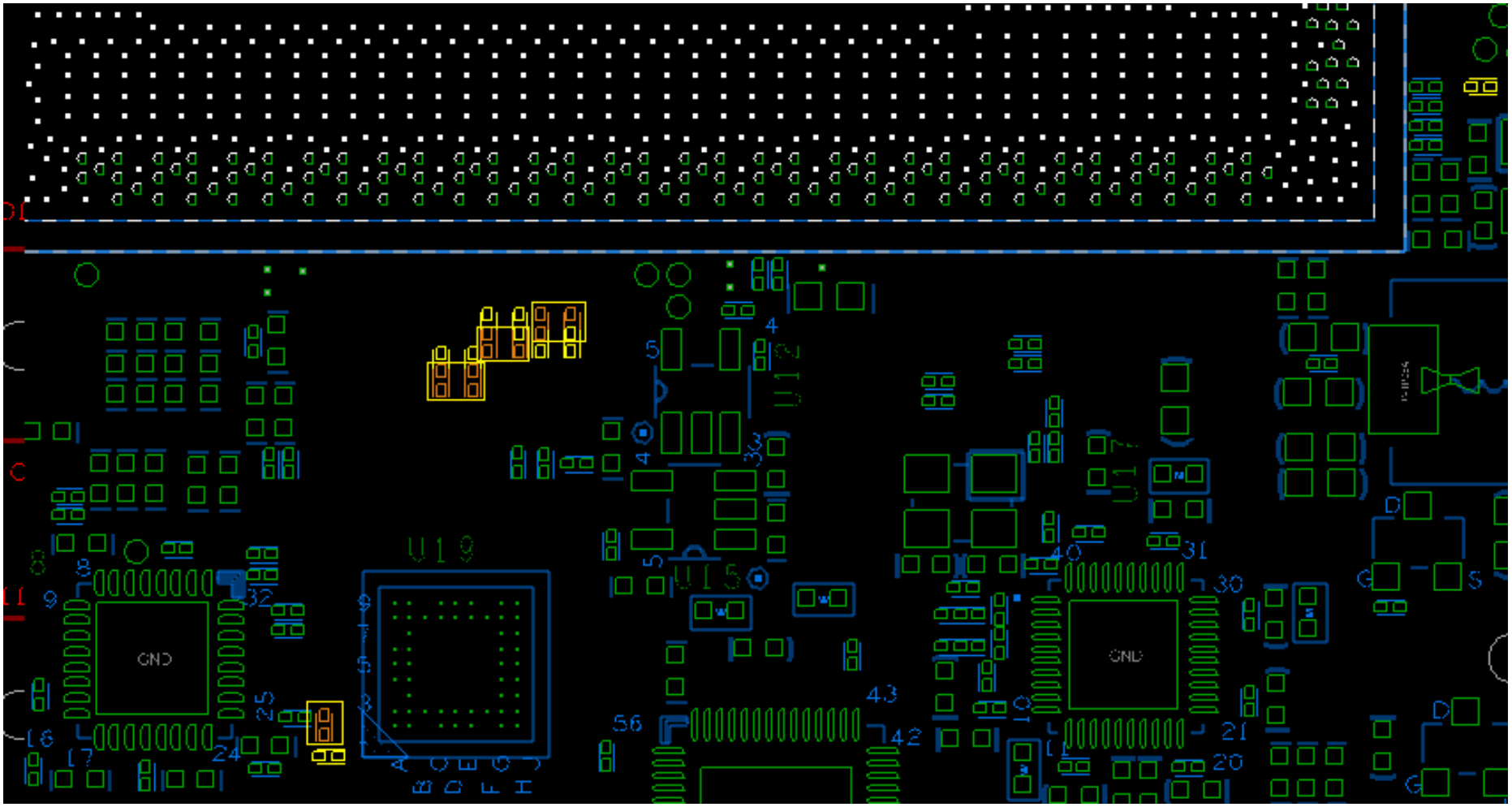
- Step 2

Add below resistors and caps :
C148,C149,R716,R717,R718,R715,R225,R727

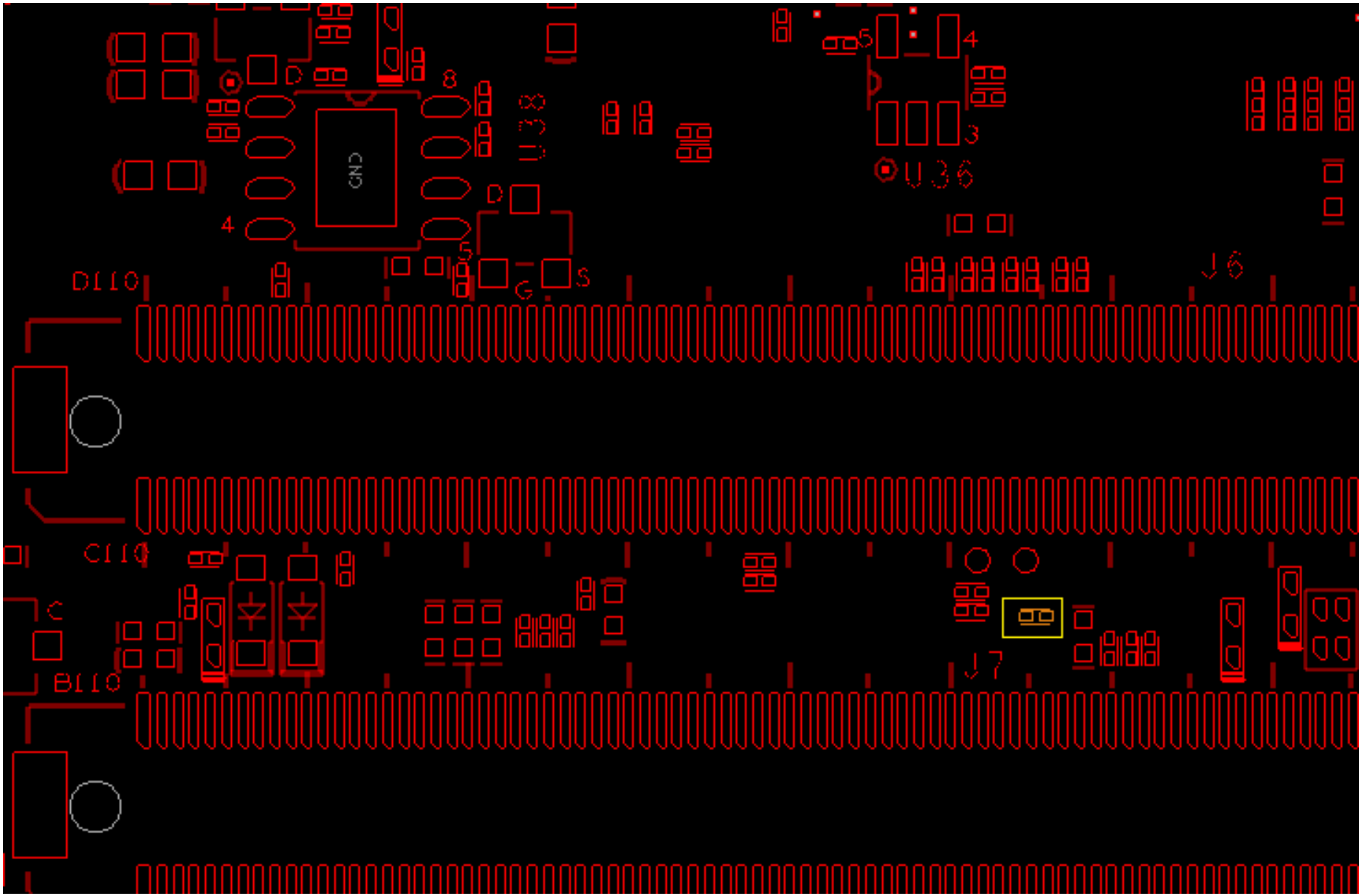
- Quick Tips

Remove 8 parts (yellow color rectangle)
Add 8 parts (Red color rectangle)

Remove (top side)



Remove (bottom side)



Add (top side)

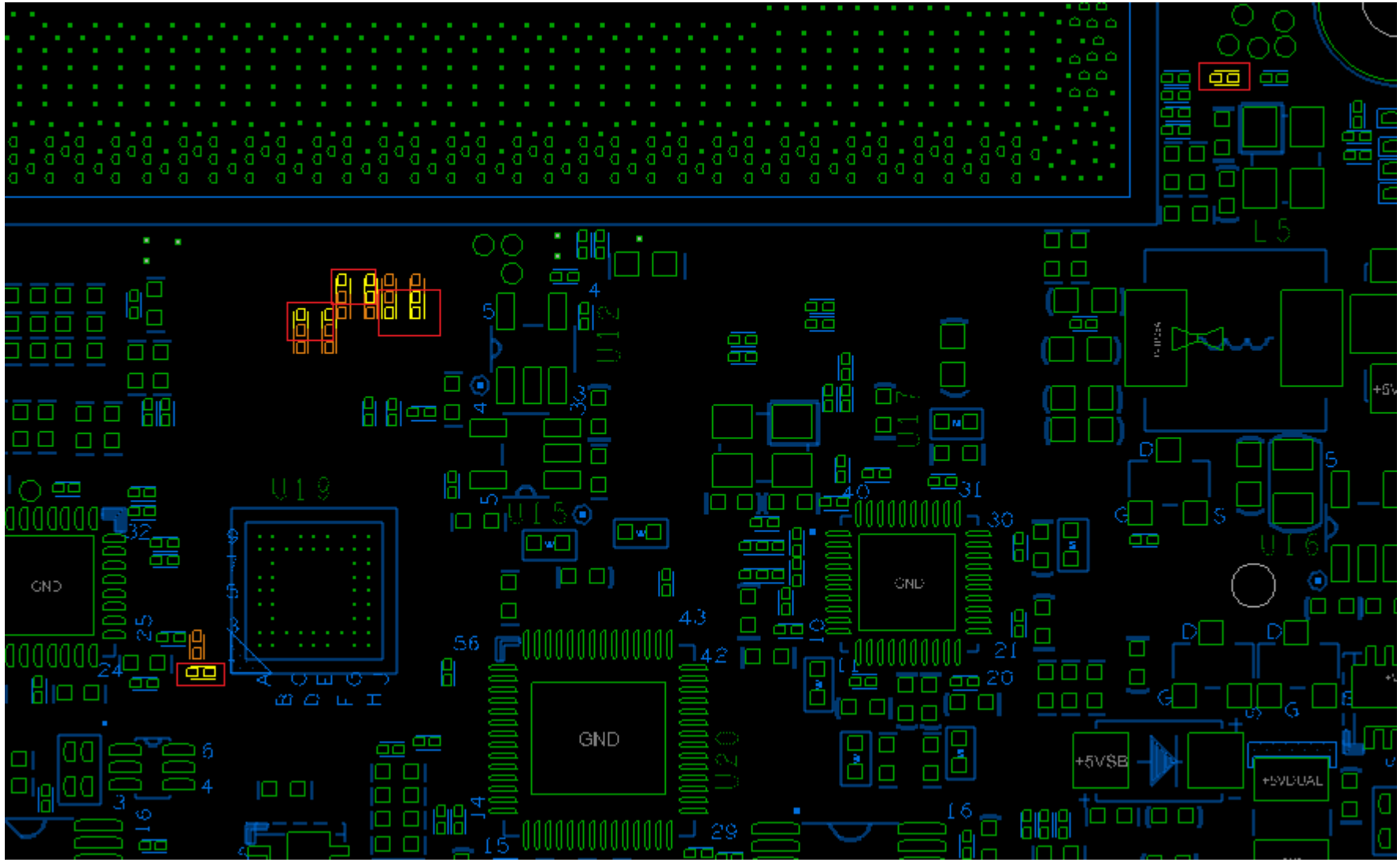


Figure 5 Optional function rework SOP : eDP

2. Optional function rework SOP : DDI2 (HDMI)

PCOM-B653VGL Default display is DDI2(HDMI/DP), rework following SOP for VGA display interface

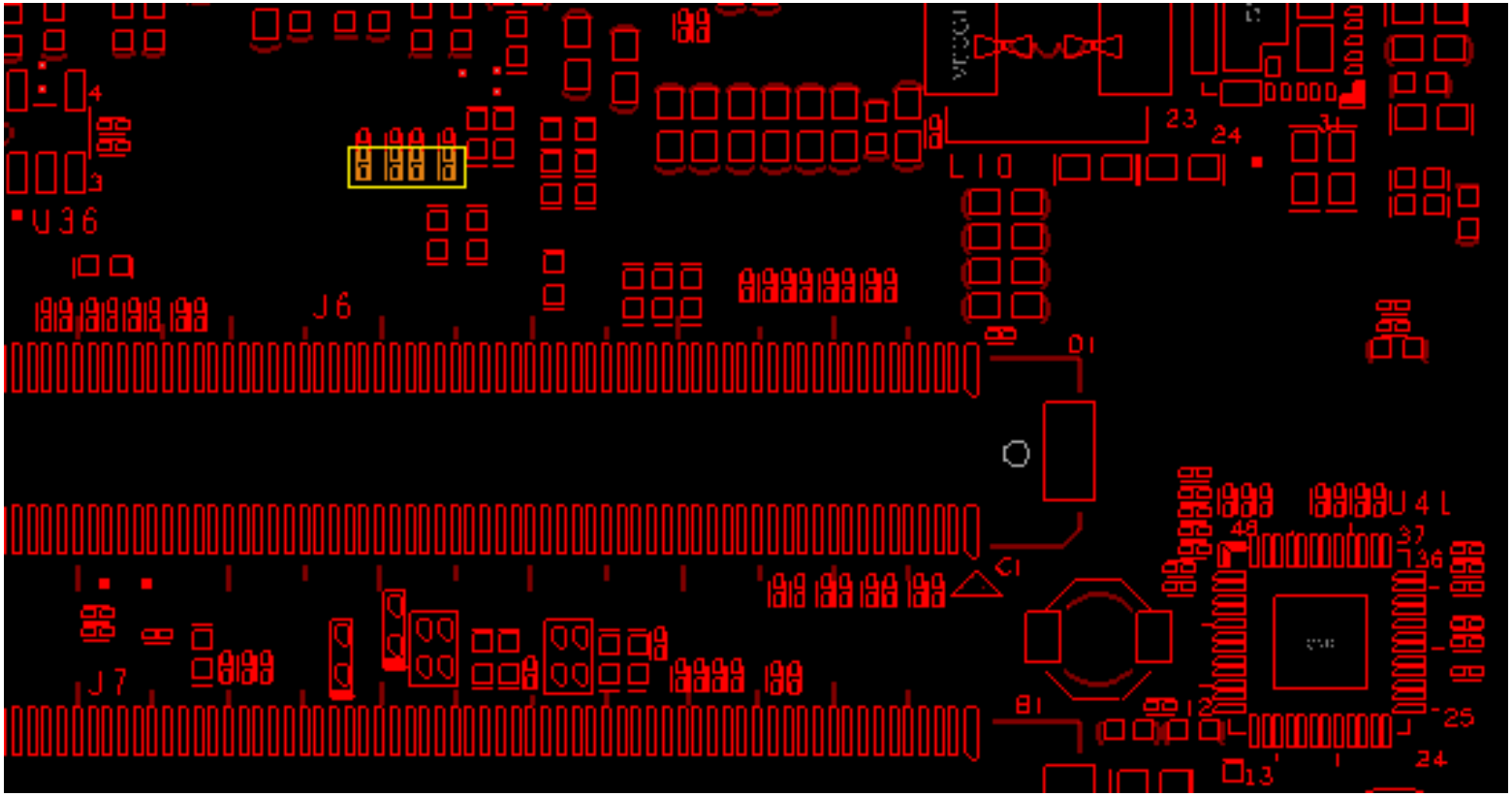
- Step 1

Remove R598,R599,R614,R615,R611,Q3,R731,R730.

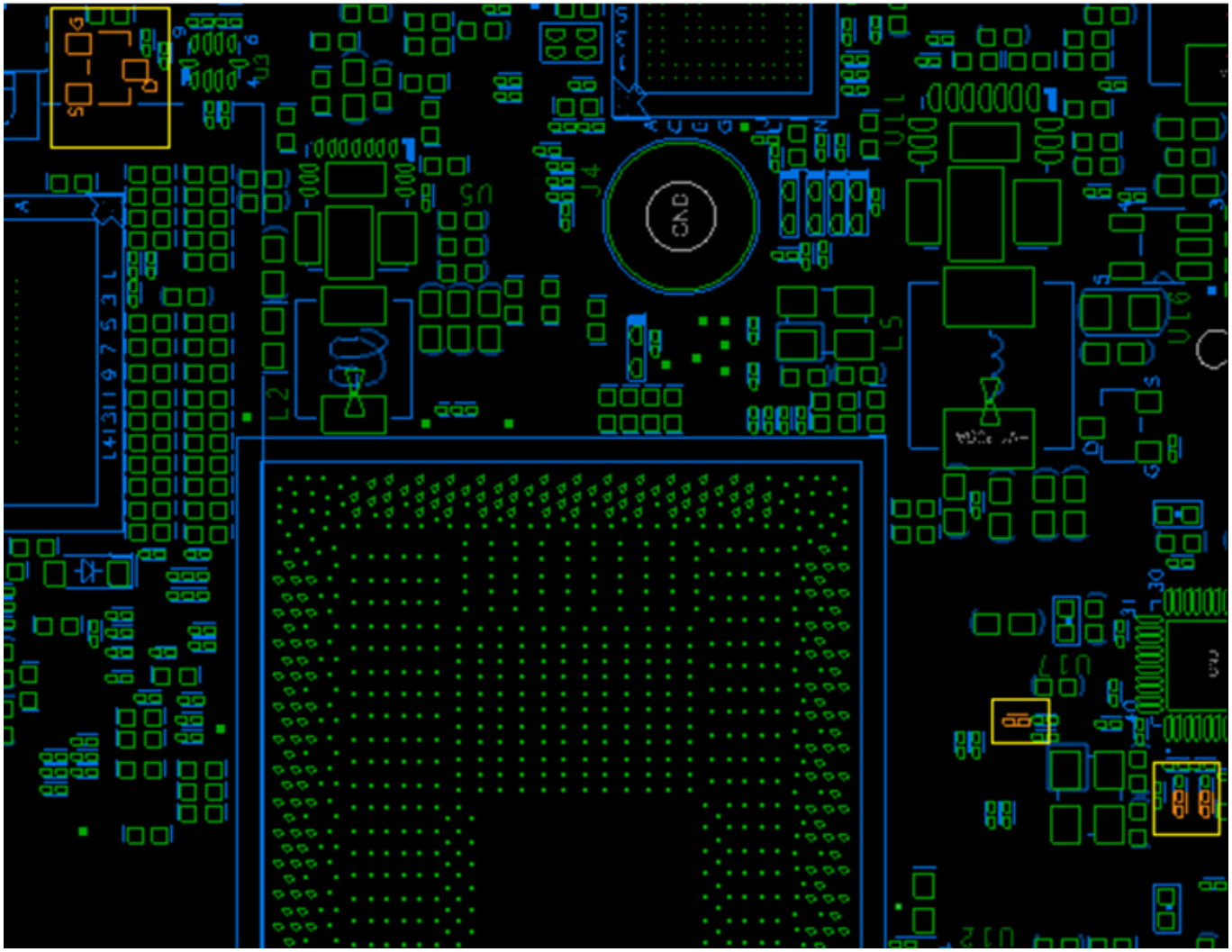
- Step 2

Add C172,C173,C180,C181,C195,C203,C290

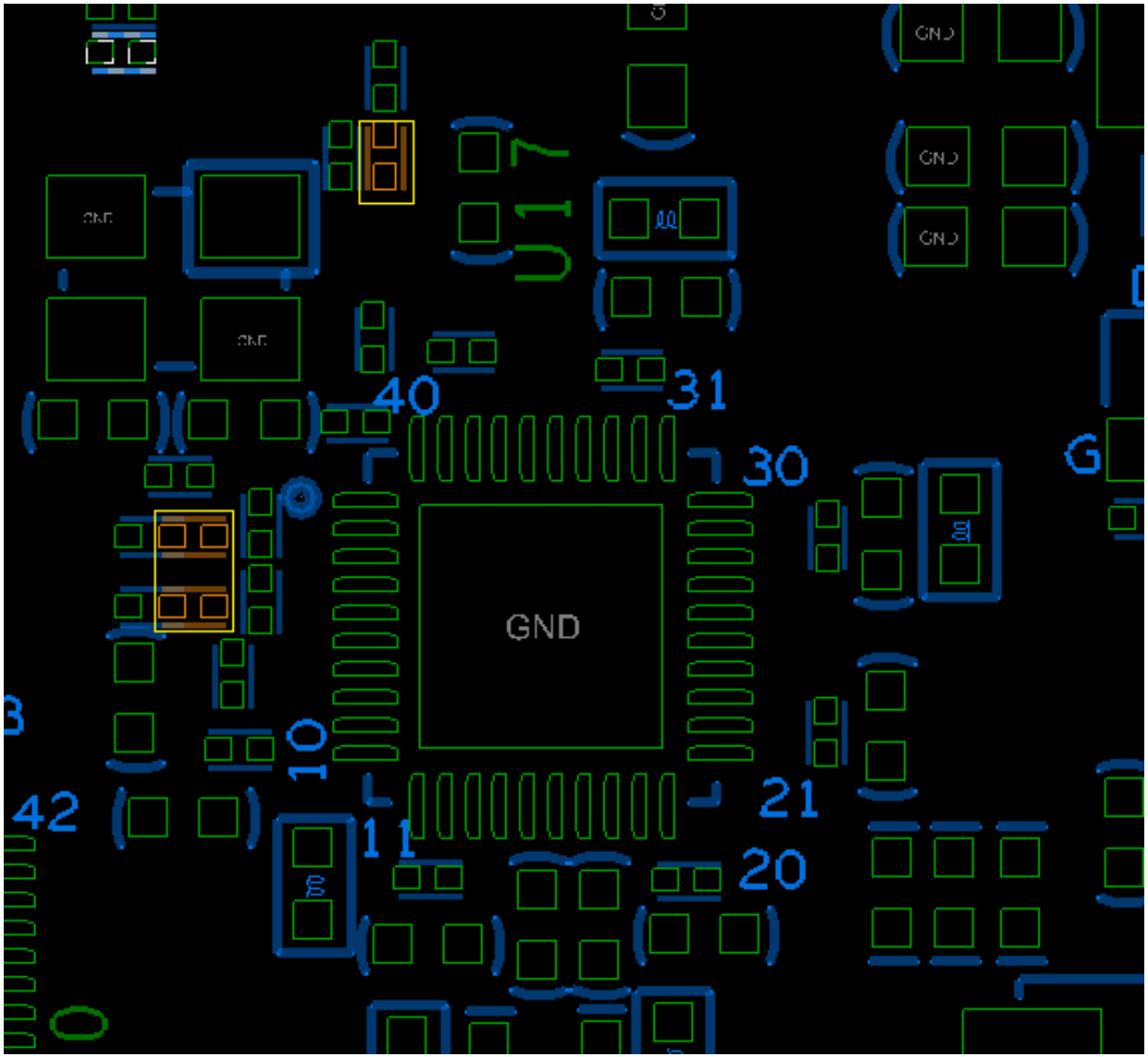
Remove (Top side)



Remove (Bottom side)



Add (Top side)



Add (Bottom side)

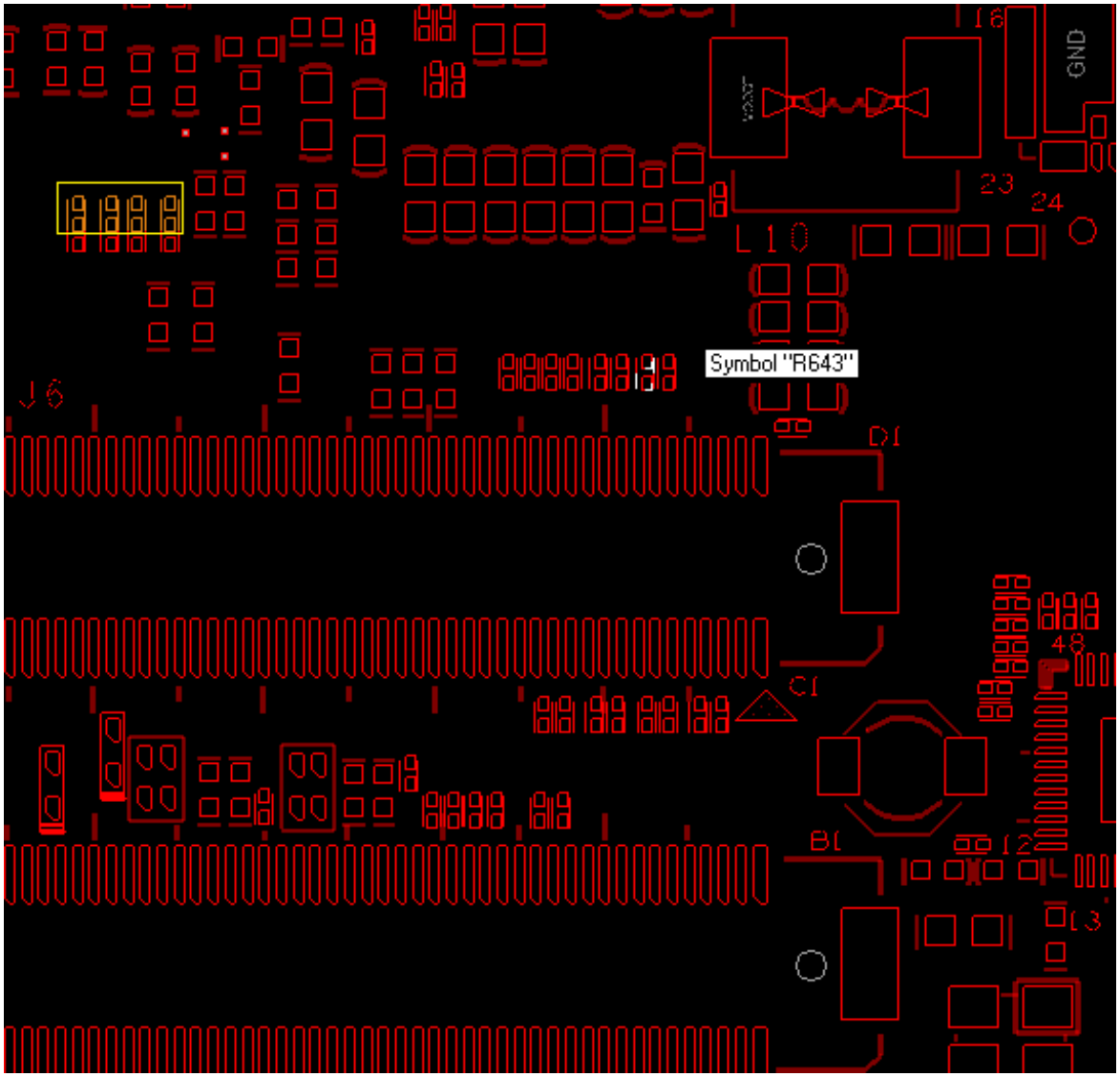


Figure 6 Optional function rework SOP : DDI2 (HDMI)

4 Heatsink / Cooler dimensions

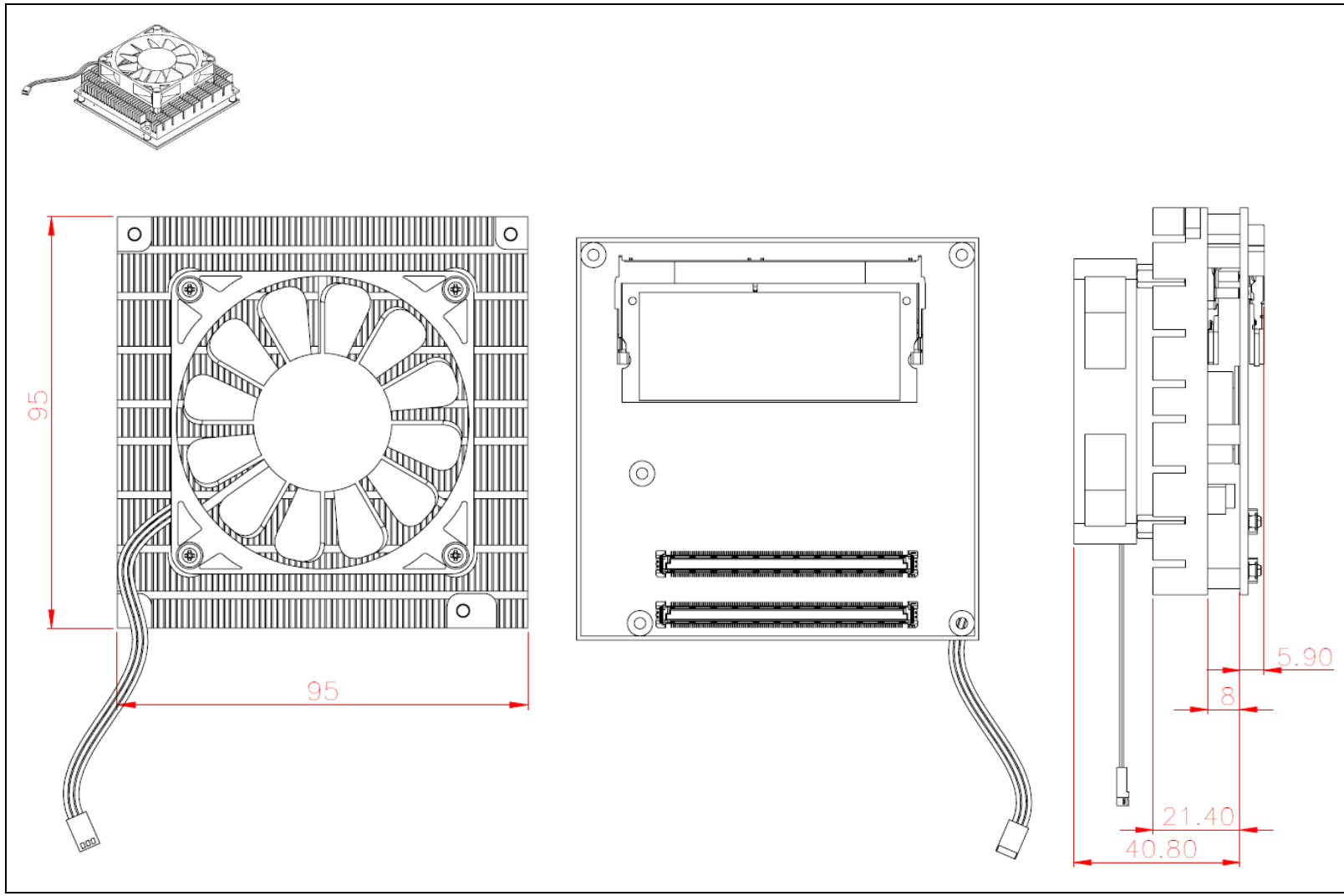


Figure 7 Heat sink / cooler mechanical dimensions

4.1 H/S Assembly

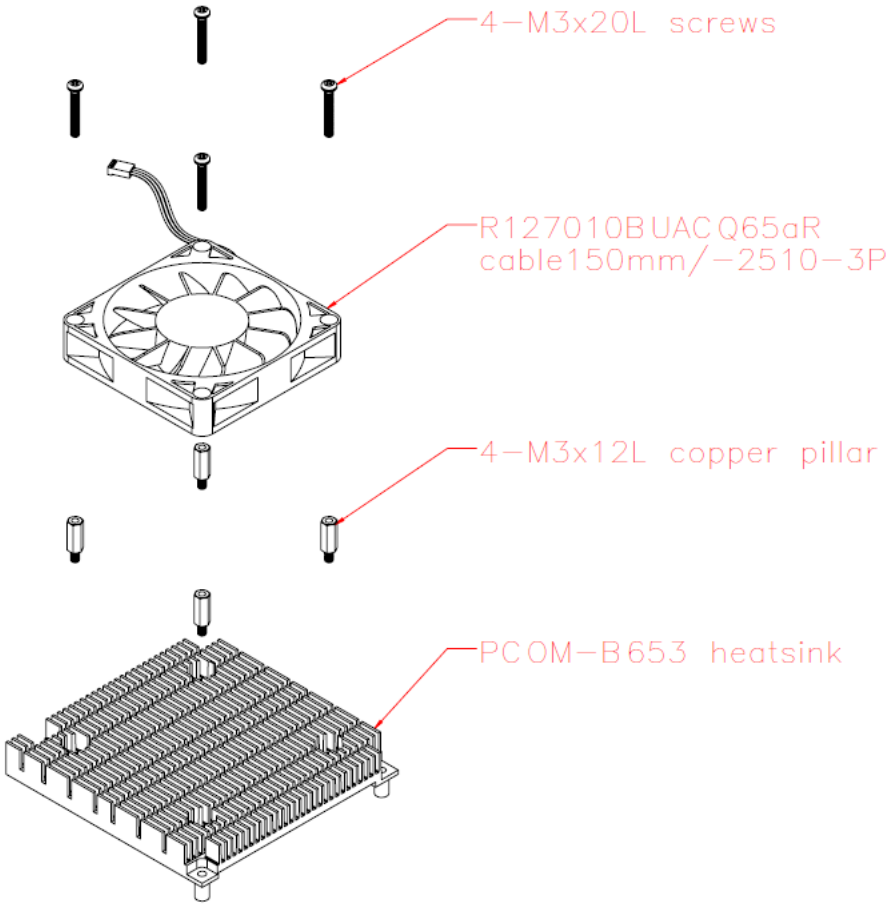


Figure 8 H/S Assembly guide

4.2 Packaging

Package	Appearance	Size
Anti-Static bubble bag		180x135mm
White Paper Box		210x151x40mm
Shipping Box (10 pcs White paper box)		595x300x195mm

Table 7 Packaging

4.3 Ordering Guide

PCOM-B653VGL

Product	Ordering P/N	Status
PCOM-B653VGL-8145UE	AB1-3K05	Available
PCOM-B653VGL-8365UE	AB1-3K04	Available
PCOM-B653VGL-8665UE	AB1-3K06	Available

Table 8 Ordering Guide - PCOM-B653VGL

Accessory

Product	Ordering P/N	Status
PCOM-B653VGL Cooler	B9971821	Available
PCOM-B653VGL Heat Spreader	B830A560	Available
PCOM-C605	AB1-3998	Available

Table 9 Ordering Guide - Accessory

5 Signal Descriptions and Pinout Tables

Below tables lists PCOM-B653VGL AB and CD Row connectors Type 6 pin name, un-connected pins are present as NC

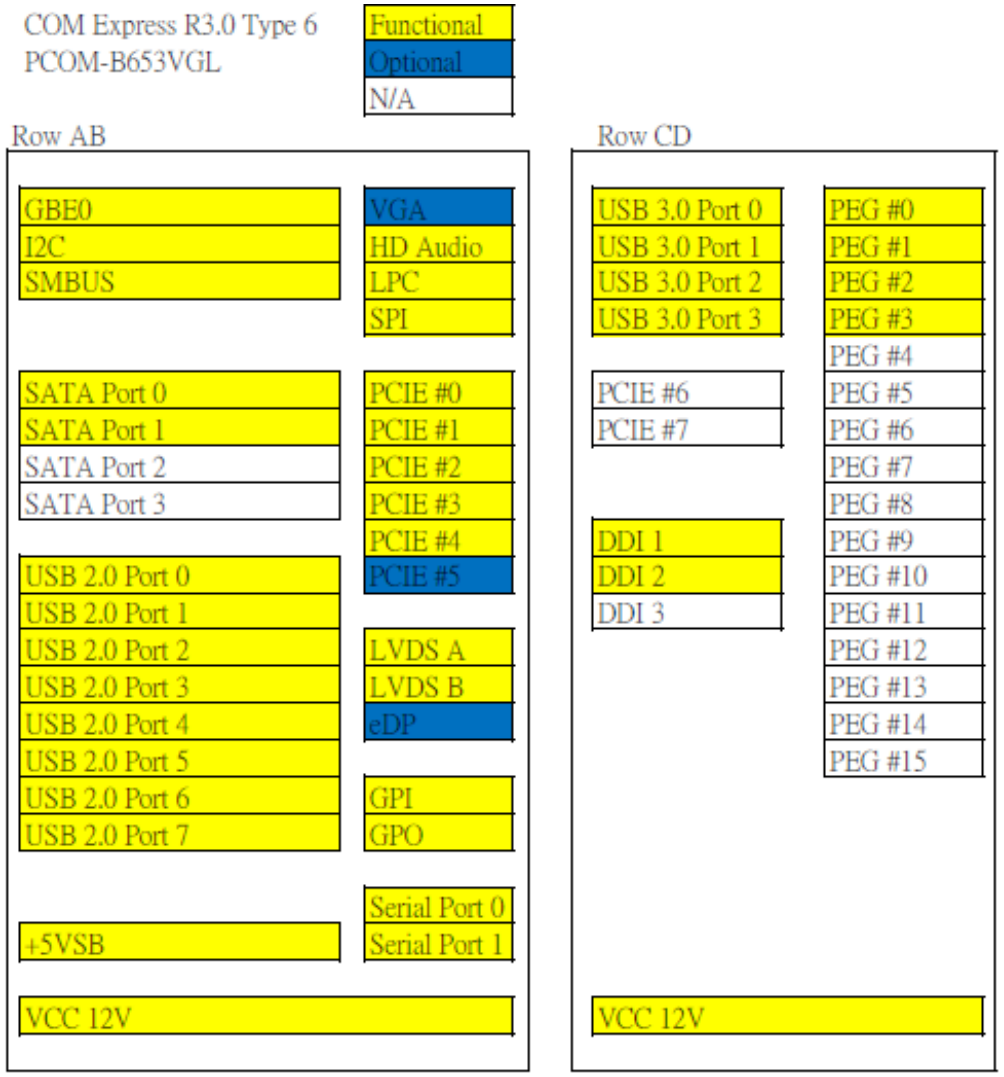


Figure 9 AB & CD Row connector signals

PCOM-B653VGL-ZR0 Pin out (Original Type 6 pin definition)							
Pin	**Row A**	**Pin**	**Row B**	**Pin**	**Row C**	**Pin**	**Row D**
A1	GND(FIXED)	**B1**	GND(FIXED)	**C1**	GND(FIXED)	**D1**	GND(FIXED)
A2	GBE0_MDI3-	**B2**	GBE0_ACT#	**C2**	GND	**D2**	GND
A3	GBE0_MDI3+	**B3**	LPC_FRAME#	**C3**	USB_SSRX0-	**D3**	USB_SSTX0-
A4	GBE0_LINK100#	**B4**	LPC_AD0	**C4**	USB_SSRX0+	**D4**	USB_SSTX0+
A5	GBE0_LINK1000#	**B5**	LPC_AD1	**C5**	GND	**D5**	GND
A6	GBE0_MDI2-	**B6**	LPC_AD2	**C6**	USB_SSRX1-	**D6**	USB_SSTX1-
A7	GBE0_MDI2+	**B7**	LPC_AD3	**C7**	USB_SSRX1+	**D7**	USB_SSTX1+
A8	GBE0_LINK#	**B8**	NC(LPC_DRQ0#)	**C8**	GND	**D8**	GND
A9	GBE0_MDI1-	**B9**	NC(LPC_DRQ1#)	**C9**	USB_SSRX2-	**D9**	USB_SSTX2-
A10	GBE0_MDI1+	**B10**	LPC_CLK	**C10**	USB_SSRX2+	**D10**	USB_SSTX2+
A11	GND(FIXED)	**B11**	GND(FIXED)	**C11**	GND(FIXED)	**D11**	GND(FIXED)
A12	GBE0_MDI0-	**B12**	PWRBTN#	**C12**	USB_SSRX3-	**D12**	USB_SSTX3-
A13	GBE0_MDI0+	**B13**	SMB_CK	**C13**	USB_SSRX3+	**D13**	USB_SSTX3+
A14	NC(GBE0_CTREF)	**B14**	SMB_DAT	**C14**	GND	**D14**	GND
A15	SUS_S3#	**B15**	SMB_ALERT#	**C15**	NC(DDI1_PAIR6+)	**D15**	DDI1_CTRLCLK_AUX+

Table 10 PCOM-B653VGL Pin-out 1-7

A16	SATA0_TX+	**B16**	SATA1_TX+	**C16**	NC(DDI1_PAIR6-)	**D16**	DDI1_CTRLCLK_AUX-
A17	SATA0_TX-	**B17**	SATA1_TX-	**C17**	NC(RSVD15)	**D17**	NC(RSVD15)
A18	SUS_S4#	**B18**	SUS_SATA	**C18**	NC(RSVD15)	**D18**	NC(RSVD15_
A19	SATA0_RX+	**B19**	SATA1_RX	**C19**	NC(PCIE_RX6+)	**D19**	NC(PCIE_TX6+)
A20	SATA0_RX-	**B20**	SATA1_RX	**C20**	NC(PCIE_RX6-)	**D20**	NC(PCIE_TX6)-
A21	GND(FIXED)	**B21**	GND(FIXED)	**C21**	GND(FIXED)	**D21**	GND(FIXED)
A22	NC(SATA2_TX+)	**B22**	NC(SATA3_TX+)	**C22**	NC(PCIE_RX7+)	**D22**	NC(PCIE_TX7+)
A23	NC(SATA2_TX-)	**B23**	NC(SATA3_TX-)	**C23**	NC(PCIE_RX7-)	**D23**	NC(PCIE_TX7-)
A24	SUS_S5#	**B24**	PWR_OK	**C24**	DDI1_HPD	**D24**	NC(RSVD20)
A25	NC(SATA2_RX+)	**B25**	NC(SATA3_RX+)	**C25**	NC(DDI1_PAIR4+)	**D25**	NC(RSVD21)
A26	NC(SATA2_RX-)	**B26**	NC(SATA3_RX-)	**C26**	NC(DDI1_PAIR4-)	**D26**	NC(DDI1_PAIR0+)
A27	BATLOW#	**B27**	WDT	**C27**	NC(RSVD15)	**D27**	NC(DDI1_PAIR0)-
A28	(S)ATA_ACT#	**B28**	NC(PCH_HDA_SDI1)	**C28**	NC(RSVD15)	**D28**	NC(RSVD21)
A29	AC/HDA_SYNC	**B29**	AC/HDA_SDIN1	**C29**	NC(DDI1_PAIR5+)	**D29**	DPB_TXP1
A30	AC/HDA_RST#	**B30**	AC/HDA_SDIN0	**C30**	NC(DDI1_PAIR5-)	**D30**	DPB_TXN1

Table 11 PCOM-B653VGL Pin-out 2-7

A31	GND(FIXED)	**B31**	GND(FIXED)	**C31**	GND(FIXED)	**D31**	GND(FIXED)
A32	AC/HDA_BITCLK	**B32**	SPKR	**C32**	DDI2_CTRLCLK_AUX+	**D32**	DDI1_PAIR2+
A33	AC/HDA_SDOUT	**B33**	I2C_CK	**C33**	DDI2_CTRLCLK_AUX-	**D33**	DDI1_PAIR2-
A34	BIOS_DIS0#	**B34**	I2C_DAT	**C34**	DDI2_DDC_AUX_SEL	**D34**	DDI1_DDC_AUX_SEL
A35	THRMTRIP#	**B35**	THRM#	**C35**	NC(RSVD15)	**D35**	NC(RSVD15)
A36	USB6-	**B36**	USB7-	**C36**	NC(DDI3_CTRLCLK_AUX+)	**D36**	DDI1_PAIR3+
A37	USB6+	**B37**	USB7+	**C37**	NC(DDI3_CTRLCLK_AUX-)	**D37**	DDI1_PAIR3-
A38	USB_6_7_OC#	**B38**	USB_4_5_OC#	**C38**	NC(DDI3_DDC_AUX_SEL)	**D38**	NC(RSVD15)
A39	USB4-	**B39**	USB5-	**C39**	NC(DDI3_PAIR0+)	**D39**	DDI2_PAIR0+
A40	USB4+	**B40**	USB5+	**C40**	NC(DDI3_PAIR0-)	**D40**	DDI2_PAIR0-
A41	GND(FIXED)	**B41**	GND(FIXED)	**C41**	GND(FIXED)	**D41**	GND(FIXED)
A42	USB2-	**B42**	USB3-	**C42**	NC(DDI3_PAIR1+)	**D42**	DDI2_PAIR1+
A43	USB2+	**B43**	USB3+	**C43**	NC(DDI3_PAIR1-)	**D43**	DDI2_PAIR1-
A44	USB_2_3_OC#	**B44**	USB_0_1_OC#	**C44**	NC(DDI3_HPD)	**D44**	DDI2_HPD
A45	USB0-	**B45**	USB1-	**C45**	NC(RSVD15)	**D45**	NC(RSVD15)

Table 12 PCOM-B653VGL Pin-out 3-7

A46	USB0+	**B46**	USB1+	**C46**	NC(DDI3_PAIR2+)	**D46**	DDI2_PAIR2+
A47	VCC_RTC	**B47**	EXCD1_PERST#	**C47**	NC(DDI3_PAIR2-)	**D47**	DDI2_PAIR2-
A48	EXCD0_PERST#	**B48**	EXCD1_CPPE#	**C48**	NC(RSVD15)	**D48**	NC(RSVD15)
A49	NC(EXCD0_CPPE#)	**B49**	SYS_RESET#	**C49**	NC(DDI3_PAIR3+)	**D49**	DDI2_PAIR3+
A50	LPC_SERIRQ	**B50**	CB_RESET#	**C50**	NC(DDI3_PAIR3-)	**D50**	DDI2_PAIR3-
A51	GND(FIXED)	**B51**	GND(FIXED)	**C51**	GND(FIXED)	**D51**	GND(FIXED)
A52	PCIE_TX5+	**B52**	PCIE_RX5+	**C52**	PEG_RX0+	**D52**	PEG_TX0+
A53	PCIE_TX5-	**B53**	PCIE_RX5-	**C53**	PEG_RX0-	**D53**	PEG_TX0-
A54	GP10	**B54**	GPO1	**C54**	NC(TYPE0#)	**D54**	PEG_LANE_RV#
A55	PCIE_TX4+	**B55**	PCIE_RX4+	**C55**	PEG_RX1+	**D55**	PEG_TX1+
A56	PCIE_TX4-	**B56**	PCIE_RX4-	**C56**	PEG_RX1-	**D56**	PEG_TX1-
A57	GND	**B57**	GPO2	**C57**	NC(TYPE1#)	**D57**	TYPE2#
A58	PCIE_TX3+	**B58**	PCIE_RX3+	**C58**	PEG_RX2+	**D58**	PEG_TX2+
A59	PCIE_TX3-	**B59**	PCIE_RX3-	**C59**	PEG_RX2-	**D59**	PEG_TX2-
A60	GND(FIXED)	**B60**	GND(FIXED)	**C60**	GND(FIXED)	**D60**	GND(FIXED)

Table 13 PCOM-B653VGL Pin-out 4-7

A61	PCIE_TX2+	**B61**	PCIE_RX2+	**C61**	PCIE_RX12+	**D61**	PCIE_TX12+
A62	PCIE_TX2-	**B62**	PCIE_RX2-	**C62**	PCIE_RX12-	**D62**	PCIE_TX12-
A63	GPI1	**B63**	GPO3	**C63**	NC(RSVD15)	**D63**	NC(RSVD15)
A64	PCIE_TX1+	**B64**	PCIE_RX1+	**C64**	NC(RSVD15)	**D64**	NC(RSVD15)
A65	PCIE_TX1-	**B65**	PCIE_RX1-	**C65**	NC(PEG_RX4+)	**D65**	NC(PEG_TX4+)
A66	GND	**B66**	WAKE0#	**C66**	NC(PEG_RX4-)	**D66**	NC(PEG_TX4-)
A67	GPI2	**B67**	N/A(WAKE1#)	**C67**	NC(RSVD15)	**D67**	GND
A68	PCIE_TX0+	**B68**	PCIE_RX0+	**C68**	NC(PEG_RX5+)	**D68**	NC(PEG_TX5+)
A69	PCIE_TX0-	**B69**	PCIE_RX0-	**C69**	NC(PEG_RX5-)	**D69**	NC(PEG_TX5-)
A70	GND(FIXED)	**B70**	GND(FIXED)	**C70**	GND(FIXED)	**D70**	GND(FIXED)
A71	LVDS_A0+ / eDP_TX2+	**B71**	LVDS_B0+	**C71**	NC(PEG_RX6+)	**D71**	NC(PEG_TX6+)
A72	LVDS_A0- / eDP_TX2-	**B72**	LVDS_B0-	**C72**	NC(PEG_RX6-)	**D72**	NC(PEG_TX6-)
A73	LVDS_A1+ / eDP_TX1+	**B73**	LVDS_B1+	**C73**	GND	**D73**	GND
A74	LVDS_A1- / eDP_TX1-	**B74**	LVDS_B1-	**C74**	NC(PEG_RX7+)	**D74**	NC(PEG_TX7+)
A75	LVDS_A2+ / eDP_TX0+	**B75**	LVDS_B2+	**C75**	NC(PEG_RX7-)	**D75**	NC(PEG_TX7-)

Table 14 PCOM-B653VGL Pin-out 5-7

A76	LVDS_A2- / eDP_TX0-	**B76**	LVDS_B2-	**C76**	GND	**D76**	GND
A77	LVDS_VDD_EN / eDP_VDD_EN	**B77**	LVDS_B3+	**C77**	NC(RSVD)	**D77**	D77(RSVD)
A78	LVDS_A3+	**B78**	LVDS_B3-	**C78**	NC(PEG_RX8+)	**D78**	NC(PEG_TX8+)
A79	LVDS_A3-	**B79**	LVDS_BKLT_EN / eDP_BKLT_EN	**C79**	NCPEG_RX8-)	**D79**	NC(PEG_TX8-)
A80	GND(FIXED)	**B80**	GND(FIXED)	**C80**	GND(FIXED)	**D80**	GND(FIXED)
A81	LVDS_A_CK+ / eDP_TX3+	**B81**	LVDS_B_CK+	**C81**	NC(PEG_RX9+)	**D81**	NC(PEG_TX9+)
A82	LVDS_A_CK- / eDP_TX3-	**B82**	LVDS_B_CK-	**C82**	NC(PEG_RX9-)	**D82**	NC(PEG_TX9-)
A83	LVDS_I2C_CK / eDP_AUX+	**B83**	LVDS_BKLT_CTRL / eDP_BKLT_CTRL	**C83**	NC(RSVD)	**D83**	NC(RSVD)
A84	LVDS_I2C_DAT / eDP_AUX-	**B84**	VCC_5V_SBY	**C84**	GND	**D84**	GND
A85	GPI3	**B85**	VCC_5V_SBY	**C85**	NC(PEG_RX10+)	**D85**	NC(PEG_TX10+)
A86	NC(RSVD15)	**B86**	VCC_5V_SBY	**C86**	NC(PEG_RX10-)	**D86**	NC(PEG_TX10-)
A87	eDP_HDP	**B87**	VCC_5V_SBY	**C87**	GND	**D87**	GND
A88	PCIE_CLK_REF+	**B88**	BIOS_DIS1#	**C88**	NC(PEG_RX11+)	**D88**	NC(PEG_TX11+)
A89	PCIE_CLK_REF-	**B89**	VGA_RED	**C89**	NC(PEG_RX11-)	**D89**	NC(PEG_TX11-)
A90	GND(FIXED)	**B90**	GND(FIXED)	**C90**	GND(FIXED)	**D90**	GND(FIXED)

Table 15 PCOM-B653VGL Pin-out 6-7

A91	SPI_POWER	**B91**	VGA_GRN	**C91**	NC(PEG_RX12+)	**D91**	NC(PEG_TX12+)
A92	SPI_MISO	**B92**	VGA_BLU	**C92**	NC(PEG_RX12-)	**D92**	NC(PEG_TX12-)
A93	GPO0	**B93**	VGA_HSYNC	**C93**	GND	**D93**	GND
A94	SPI_CLK	**B94**	VGA_VSYNC	**C94**	NC(PEG_RX13+)	**D94**	NC(PEG_TX13+)
A95	SPI_MOSI	**B95**	VGA_I2C_CK	**C95**	NC(PEG_RX13-)	**D95**	NC(PEG_TX13-)
A96	NC(TPM_PP)	**B96**	VGA_I2C_DAT	**C96**	GND	**D96**	GND
A97	NC(TYPE10#)	**B97**	SPI_CS#	**C97**	NC(RSVD17)	**D97**	NC(RSVD)
A98	SER0_TX	**B98**	RSVD15	**C98**	NC(PEG_RX14+)	**D98**	NC(PEG_TX14+)
A99	SER0_RX	**B99**	RSVD15	**C99**	NC(PEG_RX14-)	**D99**	NC(PEG_TX14-)
A100	GND(FIXED)	**B100**	GND(FIXED)	**C100**	GND(FIXED)	**D100**	GND(FIXED)
A101	SER1_TX	**B101**	FAN_PWNOUT	**C101**	NC(PEG_RX15+)	**D101**	NC(PEG_TX15+)
A102	SER1_RX	**B102**	FAN_TACHIN	**C102**	NC(PEG_RX15-)	**D102**	NC(PEG_TX15-)
A103	LID#	**B103**	SLEEP#	**C103**	GND	**D103**	GND
A104	VCC_12V	**B104**	VCC_12V	**C104**	VCC_12V	**D104**	VCC_12V
A105	VCC_12V	**B105**	VCC_12V	**C105**	VCC_12V	**D105**	VCC_12V
A106	VCC_12V	**B106**	VCC_12V	**C106**	VCC_12V	**D106**	VCC_12V
A107	VCC_12V	**B107**	VCC_12V	**C107**	VCC_12V	**D107**	VCC_12V
A108	VCC_12V	**B108**	VCC_12V	**C108**	VCC_12V	**D108**	VCC_12V
A109	VCC_12V	**B109**	VCC_12V	**C109**	VCC_12V	**D109**	VCC_12V
A110	GND(FIXED)	**B110**	GND(FIXED)	**C110**	GND(FIXED)	**D110**	GND(FIXED)

Table 16 PCOM-B653VGL Pin-out 7-7

6 BIOS Setup Items

PCOM-B653VGL is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, PCOM-B653VGL communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

6.1 Entering Setup - Launch System Setup

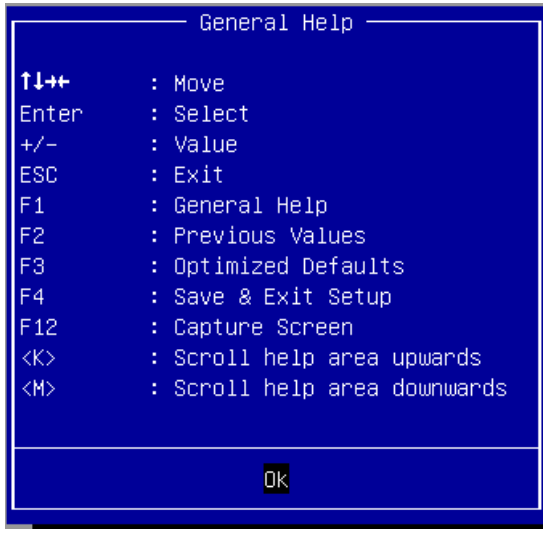
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run General Help or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



6.2 Main

Use this menu for basic system configurations, such as time, date etc.

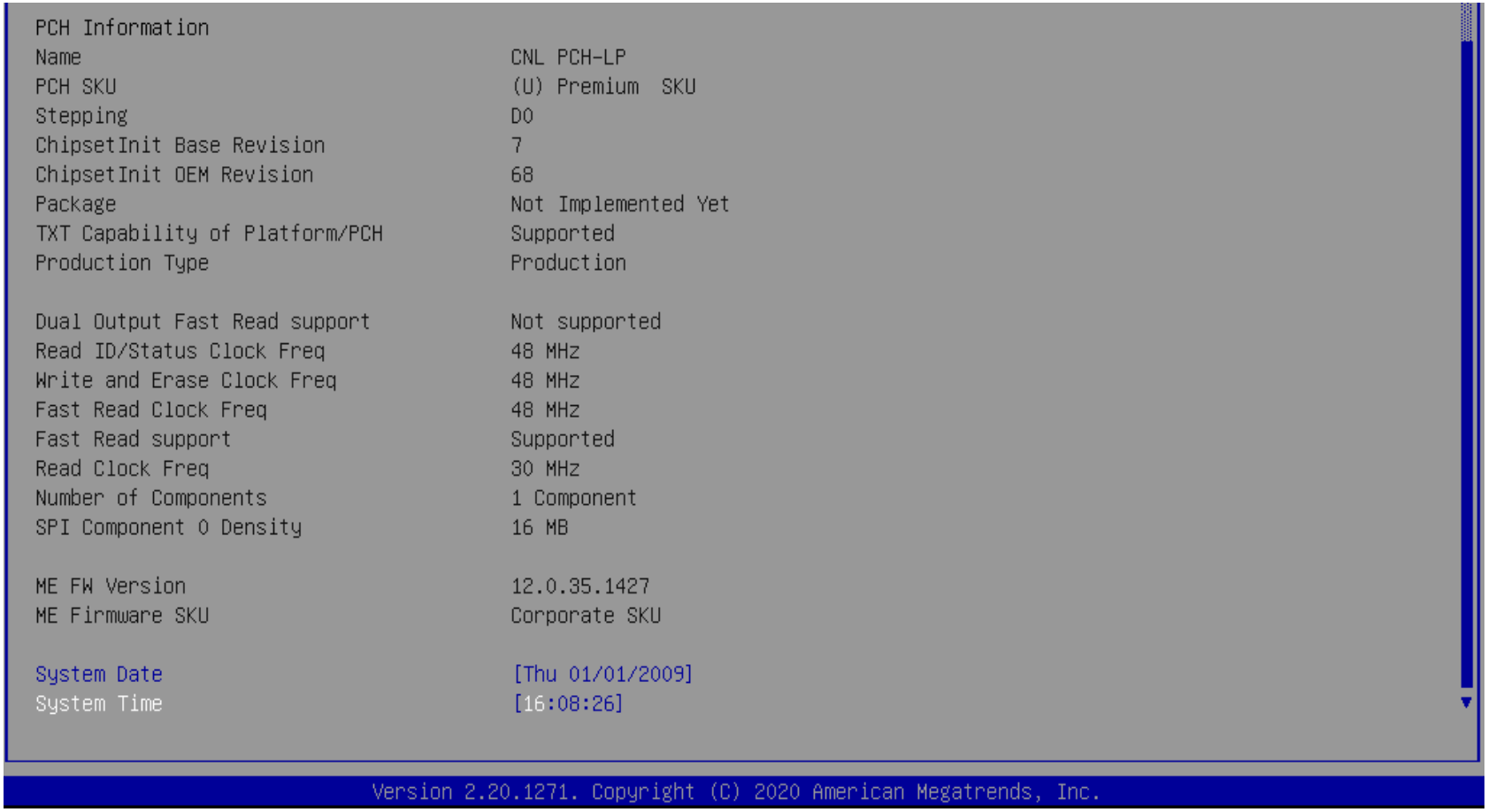


Figure 10 BIOS MAIN

Feature	Description	Options
System Date	The date format is <Day>, <Month><Date><Year>. Use [+] or [—] to configure system Date.	
System Time	The time format is <Hour><Minute><Second>. Use [+] or [—] to configure system Time.	

Table 17BIOS System Description

6.3 Configuration

Use this menu to set up the items of special enhanced features.

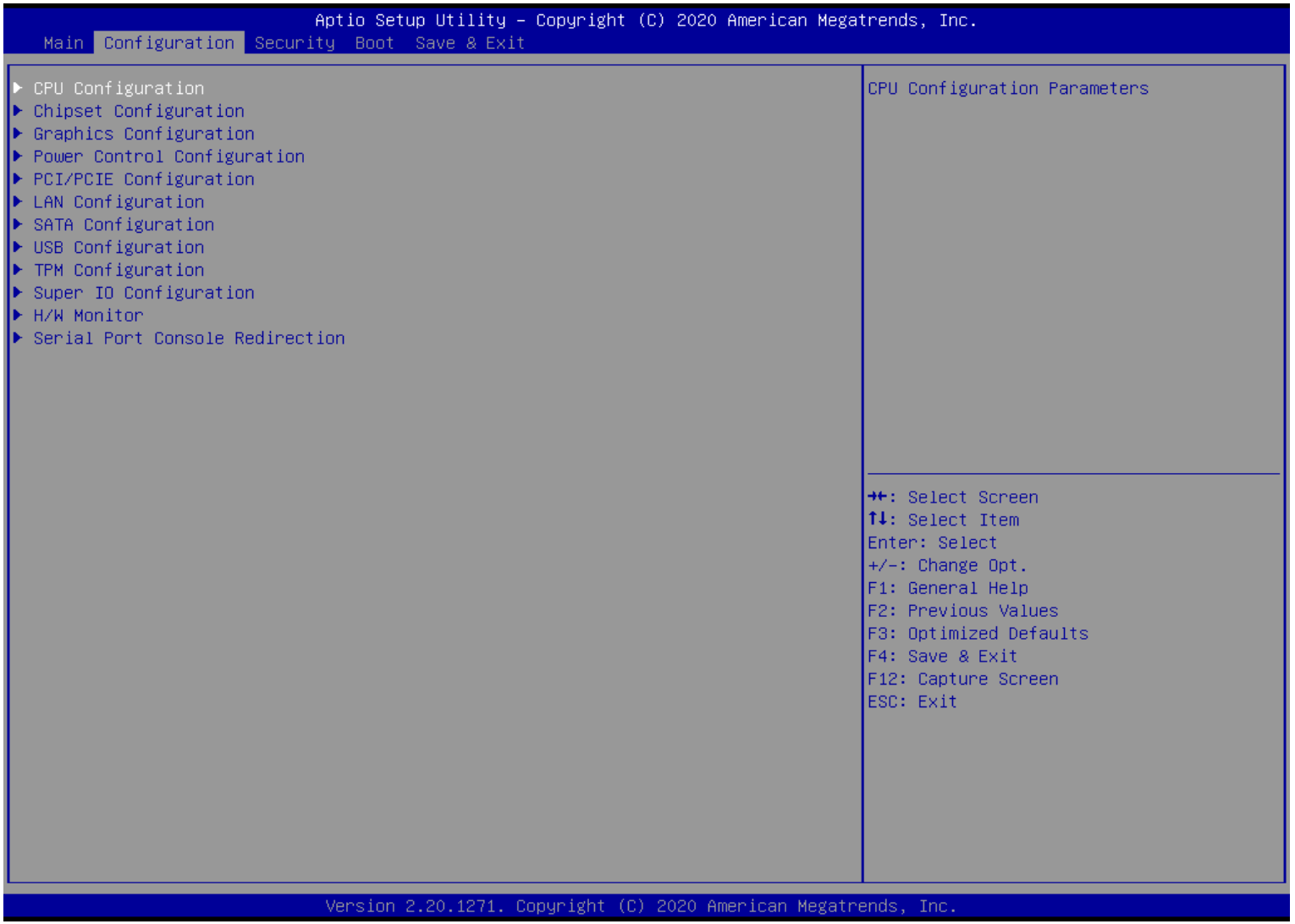


Figure 11 BIOS CONFIGURATION

6.4 CPU

CPU Configuration Parameters

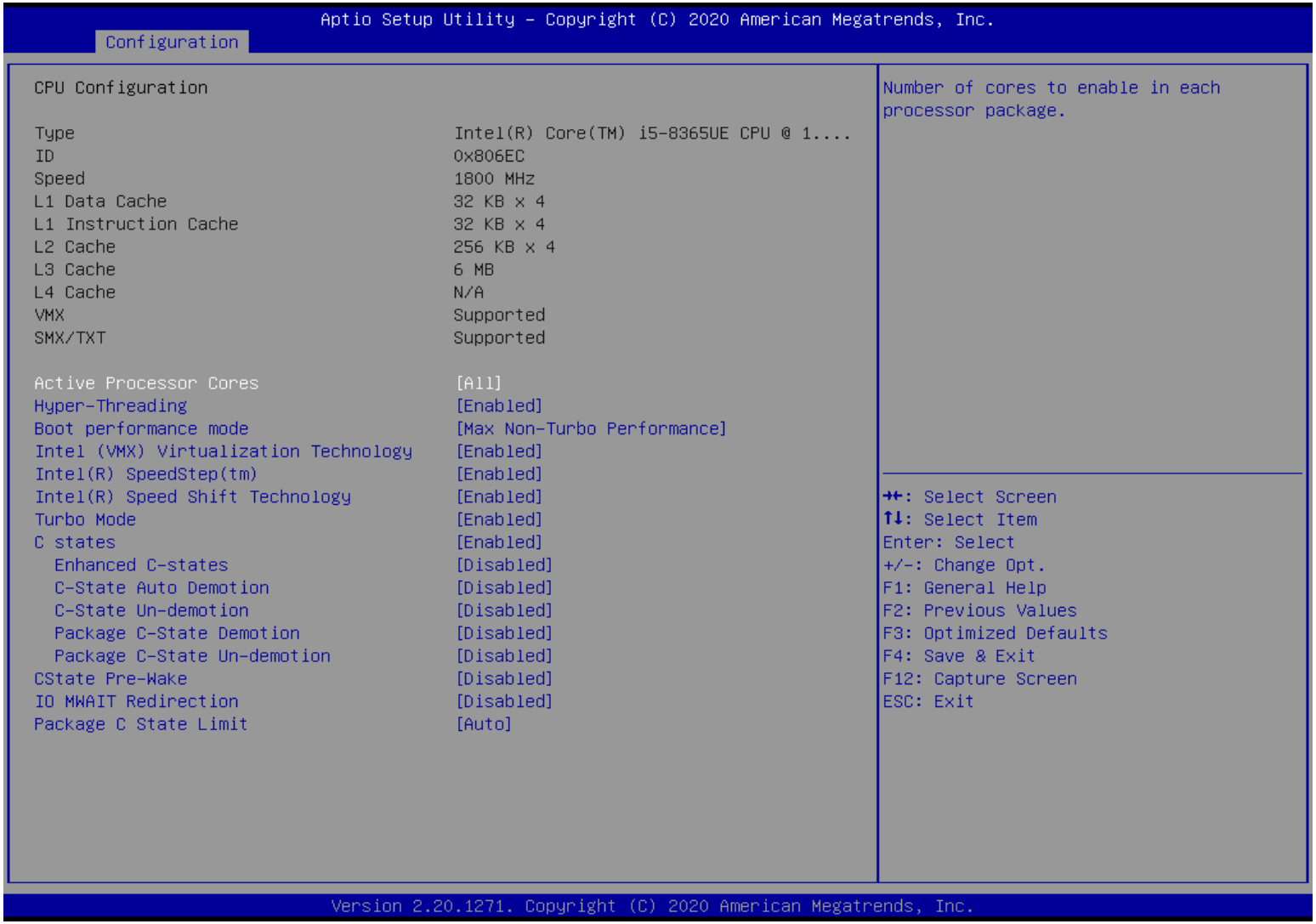


Figure 12 BIOS CPU

Feature	Description	Options
Active Processor Cores	Number of cores to enable in each processor package.	★All, 1, 2, 3,
Hyper-Threading	Enabled or Disabled Hyper-Threading Technology.	★Enabled, Disabled
Boot performance mode	Select the performance state that the BIOS will set starting from reset vector.	★Max Non-Turbo Performance, Turbo Performance, Max Battery ,
Intel (VMX) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vander pool Technology.	★Enabled, Disabled
Intel® Speed Step™	Allows more than two frequency ranges to be supported.	★Enabled, Disabled
Intel® Speed Shift Technology	Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states	★Enabled, Disabled
Turbo Mode	Enable/Disable processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled)	★Enabled, Disabled
C states	Enable/disable CPU Power Management. Allows CPU to go to C states It's not 100% utilized	★Disabled, Enabled
C states[Enabled]		
Enhanced C-states	Enable/Disable C1E.When enabled, CPU will switch to minimum speed when all cores enter C-state	★Disabled, Enabled
C-State Auto Demotion	Configure C-State Auto Demotion	★Disable, C1 ,C3 ,C1 and C3
C-State Un-demotion	Configure C-State Un-demotion	★Disable, C1 ,C3,C1 and C3
Package C State Demotion	Package C-State Demotion	★Disabled, Enabled
Package C State Un-demotion	Package C-State Un-demotion	★Disabled, Enabled
CState Pre-Wake	Disable – Sets bit 30 of POWER_CTL MSR(0x1FC) to 1 to disable the Cstate Pre-Wake	★Disabled, Enabled
IO MWAIT Redirection	When set, will map IO_read instructions sent to IO registers PMG_IO_BASE_ADDRBASE+offset to MWAIT(offset)	★Disabled, Enabled
Package C State Limit	Maximum Package C State Limit Setting. Cpu Default: Leaves to Factory default value. Auto: Initializes to deepest available Package C States Limit	★Auto,C0/C1,C2,C3,C6,C7, C7S,C8,C9,C10,Cpu Default,

Table 18BIOS CPU Description

6.5 ChipsetConfiguration

Configuration Chipset feature

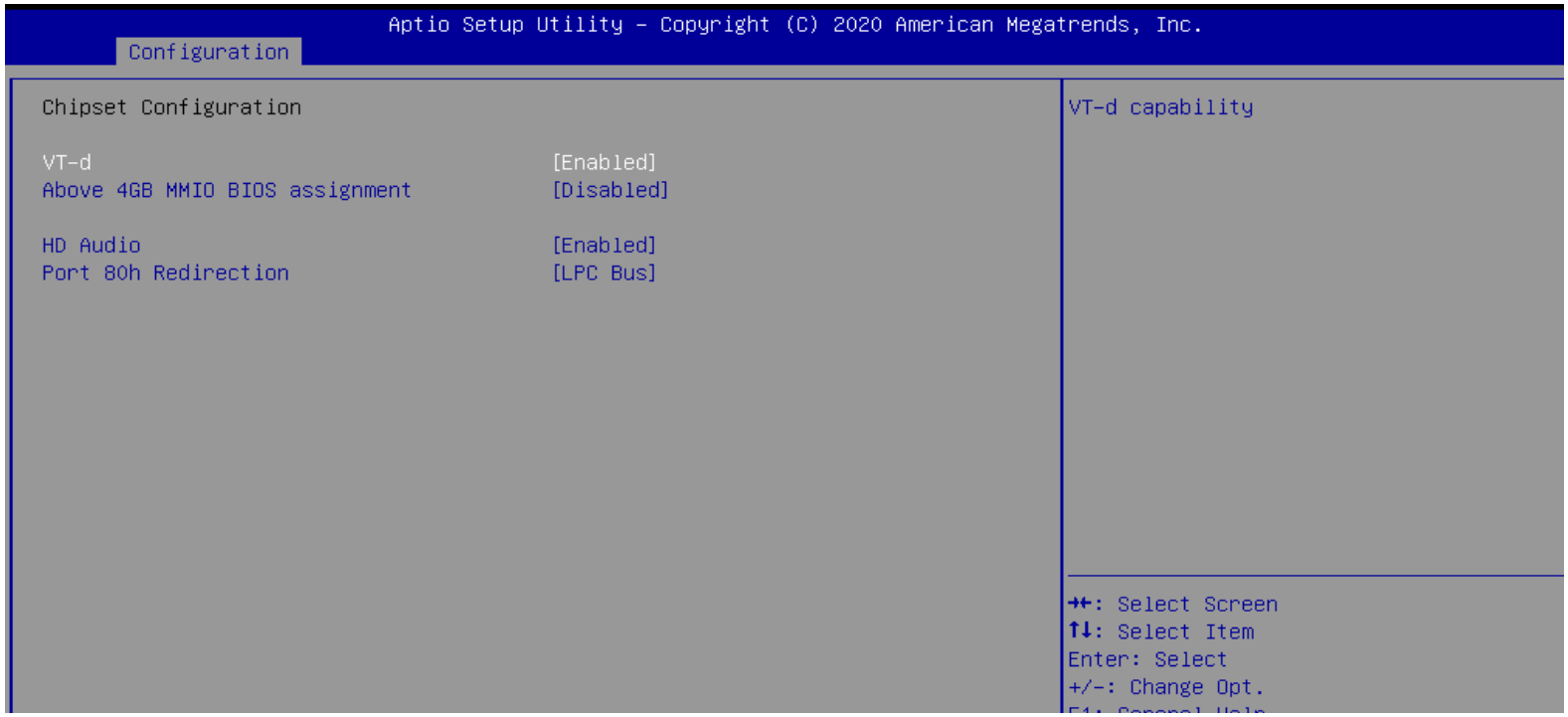


Figure 13 BIOS CHIPSET

Feature	Description	Options
VT-d	VT-d Capability	★Enabled ,Disabled
Above 4GB MMIO BIOS assignment	Enable/Disable above 4GB MemoryMappedIO BIOS assignment This is enabled automatically when Aperture Size is set to 2048MB	★Disabled, Enabled
HD Audio	Control Detection of the HD-Audio device. Disabled= HAD will be unconditionally disabled Enabled= HAD will be unconditionally enabled.	★Enabled ,Disabled
Port 80h Redirection	Control where the Port 80h cycles are sent	★LPC Bus, PCIE Bus

Table 19BIOS Chipset Description

6.6 Graphics Configuration

Configuration Graphics Settings

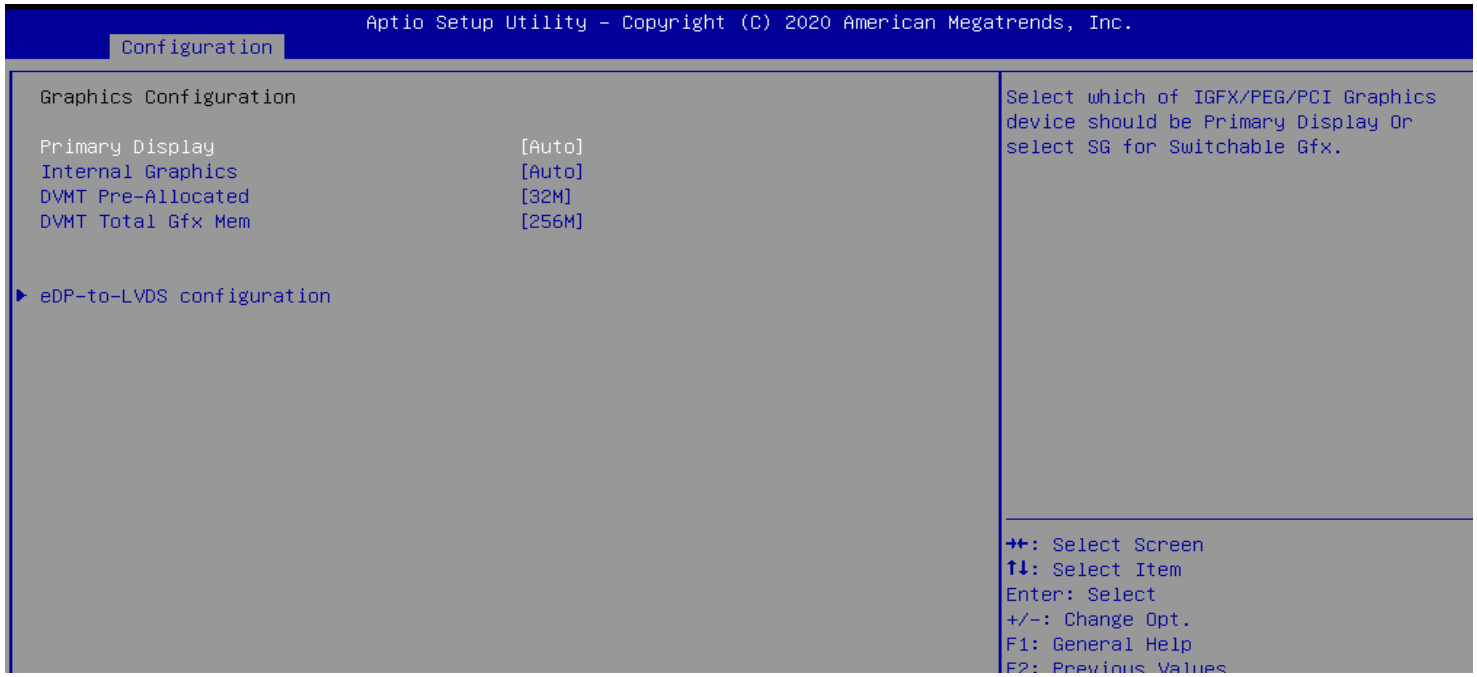


Figure 14 BIOS LAN

Feature	Description	Options
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.	★Auto, IGFX, PEG, PCIE
Internal Graphics	Keep IGFX enable based on the setup options.	★Auto, Disable, Enable
DVMT Pre-Allocated	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.	★32M,0M,64M,4M,8M,12M,16M,20M,24M, 28M,32M/F7,36M,40M,44M,48M,52M,56M, 60M
DVMT Total Gfx Mem	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device	★256M, 128M, MAX

Table 20BIOS LAN Description

eDP-to-LVDS configuration

eDP-to-LVDS(PTN3460)

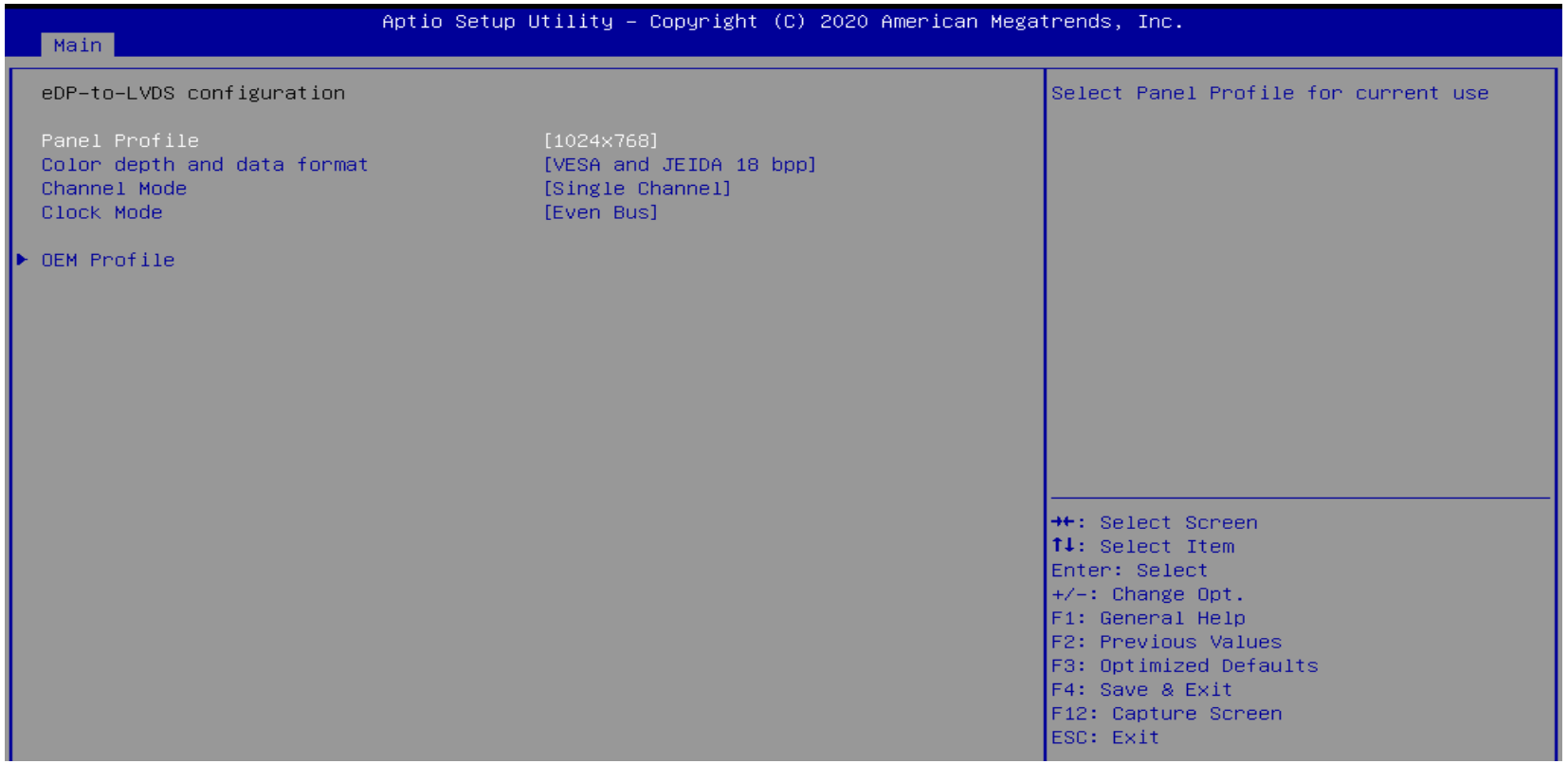


Figure 15 BIOS eDP-to-LVDS

Feature	Description	Options
Panel Profile	Select Panel Profile for current use.	★1024x768,640x480,800x480,800x600,1280x800 1280x1024,1366x768,1440x900,1920x1080,OEM Profile
Color depth and data format	Select Color depth and data format	★VESA and JEIDA 18 bpp, VESA 24 bpp, JEIDA 24 bpp
Channel Mode	Select LVDS Channel Mode	★Single Channel, Dual Channel
Clock Mode	Select clock output for LVDS.	★Even Bus, Odd Bus, Both Buses

Table 21BIOS eDP to LVDS Description

OEM Profile

PANEL 1 Help

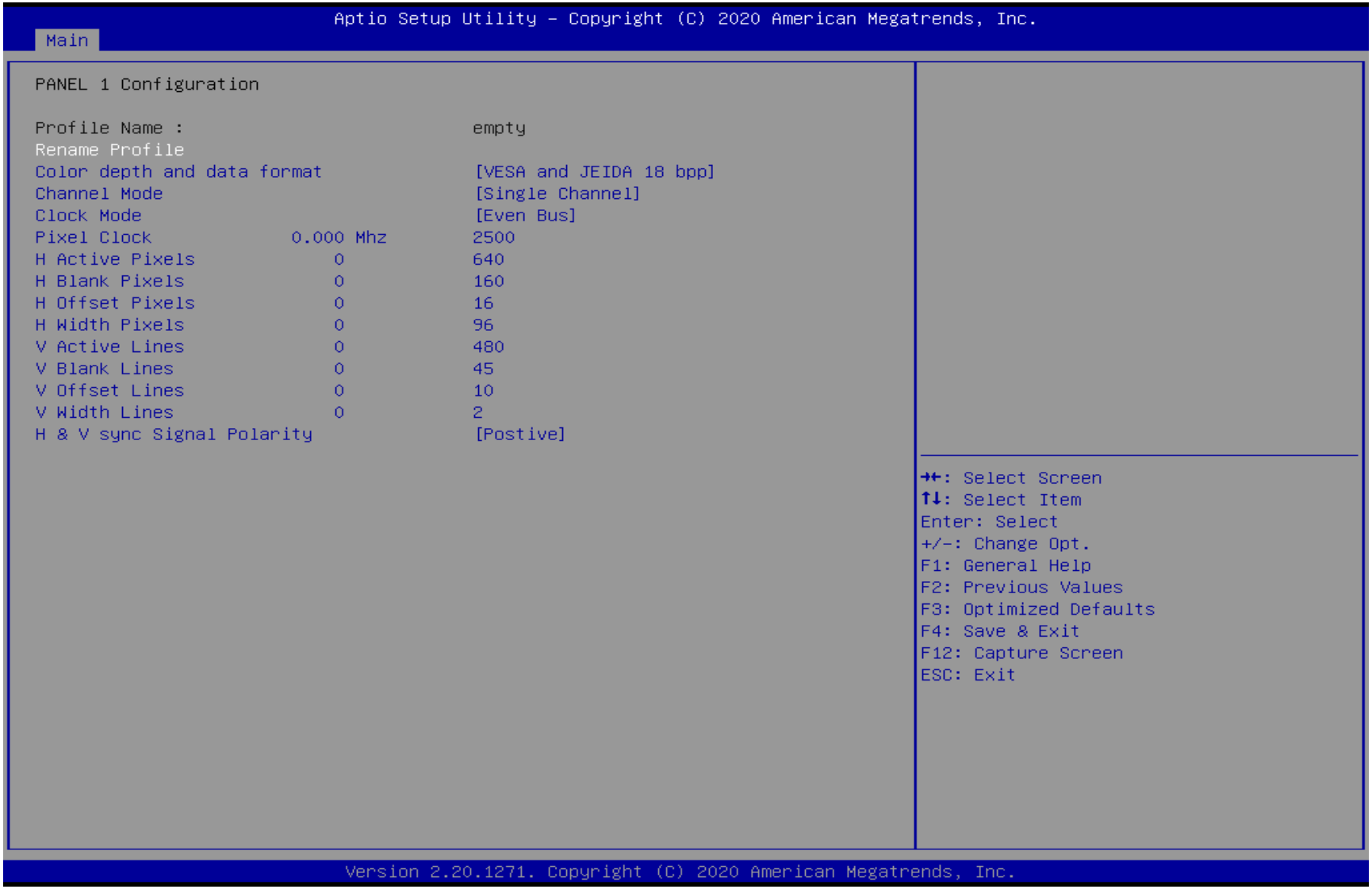


Figure 16 BIOS OEM Profile

Feature	Description	Options
Color depth and data format	Select Color depth and data format	★VESA and JEIDA 18 bpp, VESA 24 bpp, JEIDA 24 bpp
Channel Mode	Select LVDS Channel Mode	★Single Channel, Dual Channel
Clock Mode	Select clock output for LVDS.	★Even Bus, Odd Bus, Both Buses
Pixel Clock	Pixel Clock(10Khz)	★2500
H Active Pixels	H Active Pixels (Pixel)	★640
H Blank Pixels	H Blank Pixels (Pixel)	★160
H Offset Pixels	H Offset Pixels (Pixel)	★16
H Width Pixels	H Width Pixels (Pixel)	★96
V Active Lines	V Active Lines (Line)	★480
V Blank Lines	V Blank Lines (Line)	★45
V Offset Lines	V Offset Lines (Line)	★10
V Width Lines	V Width Lines (Line)	★2
H&V sync Signal Polarity	Flag: 0x1E Signal Polarity is Postive 0x18 Signal Polarity is Non-Postive	★Postive, Non-Postive

Table 22BIOS OEM Description

6.7 Power Control Configuration

System Power Control Configuration Parameters

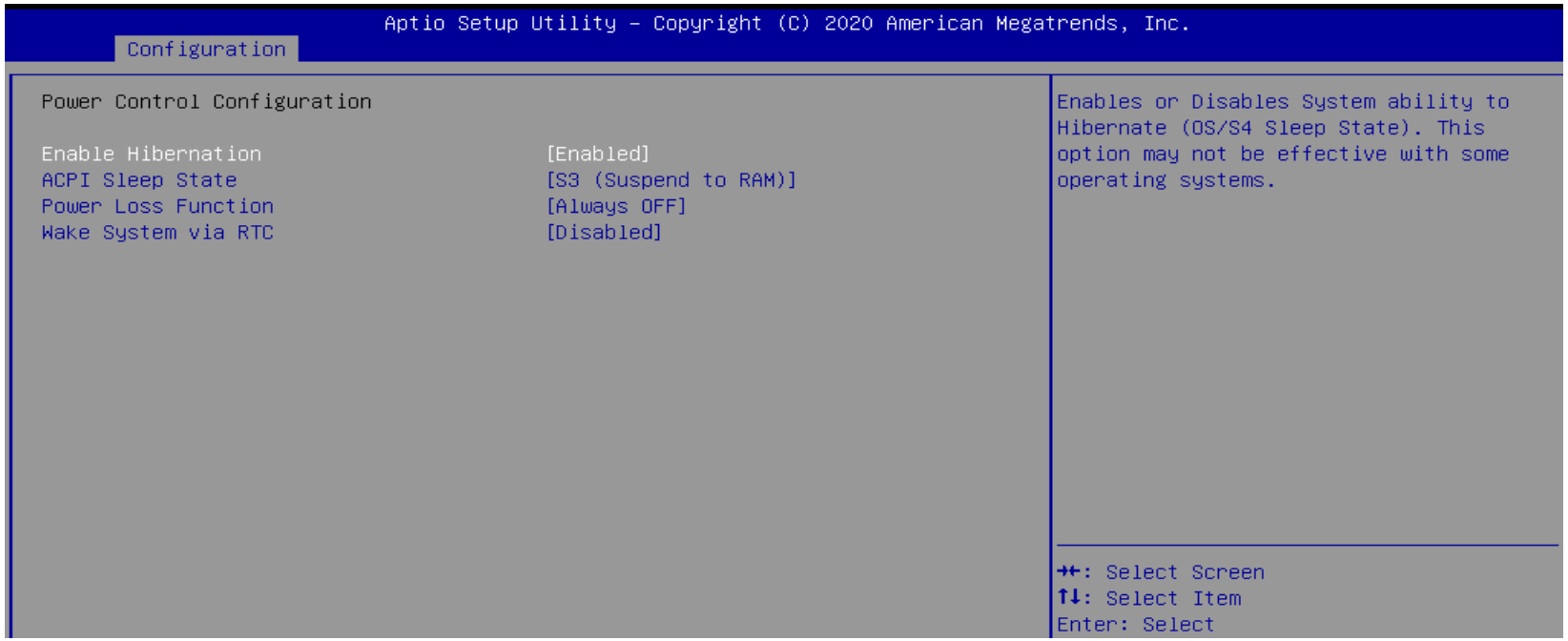


Figure 17BIOS Power Control Configuration

Feature	Description	Options
Enable Hibernation	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some operation systems.	★Enabled ,Disabled
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.	★S3 (Suspend to RAM) ,Suspend Disabled
Power Loss Function	Control SIO Power Loss Function, ON is always ON, OFF is always OFF, Last state will depends on last power state.	★Always OFF, Always ON, Last State
Wake System from S5 via RTC	Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec Specified/programmed by the Tools from OS	★Disabled, Enabled

Table 23BIOS Power Control Description

6.8 PCI/PCIE Configuration

PCI/PCI Express Settings

Figure 18BIOS PCI/PCIE Configuration

PCI Express Root Port5/6/7/8/10/13

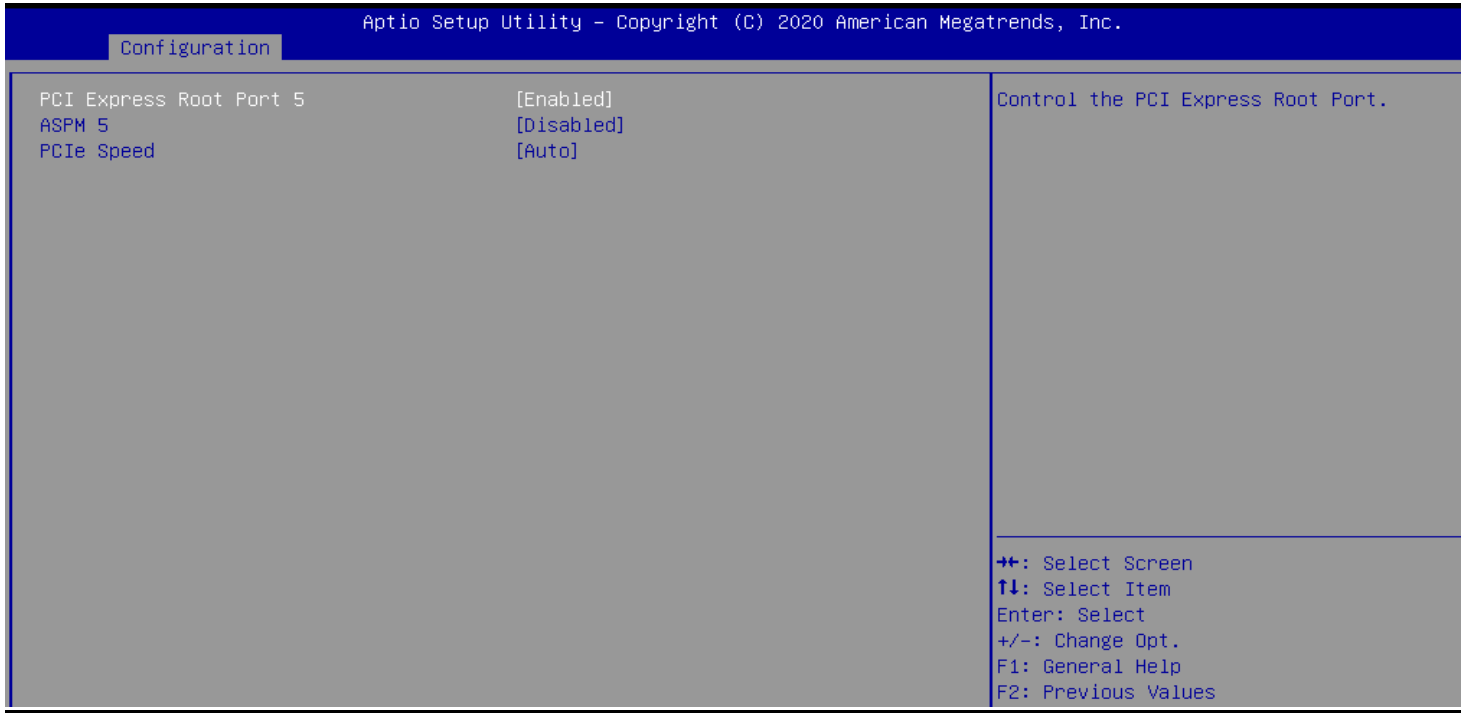


Figure 19 BIOS PCI Express Root Port

Feature	Description	Options
PCI Express Root Port 5/6/7/8/10/13	Control the PCI Express Root Port.	★Enabled , Disabled
ASPM 5/6/7/8/10/13	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO-BIOS auto configure DISABLE – Disables ASPM	★Disabled, L0s, L1, L0sL1, Auto
PCIe Speed	Configure PCIe Speed.	★Auto, Gen1, Gen2, Gen3

Table 24BIOS PCI Express Root Port Description

6.9 LAN Configuration

Configuration On Board LAN device.

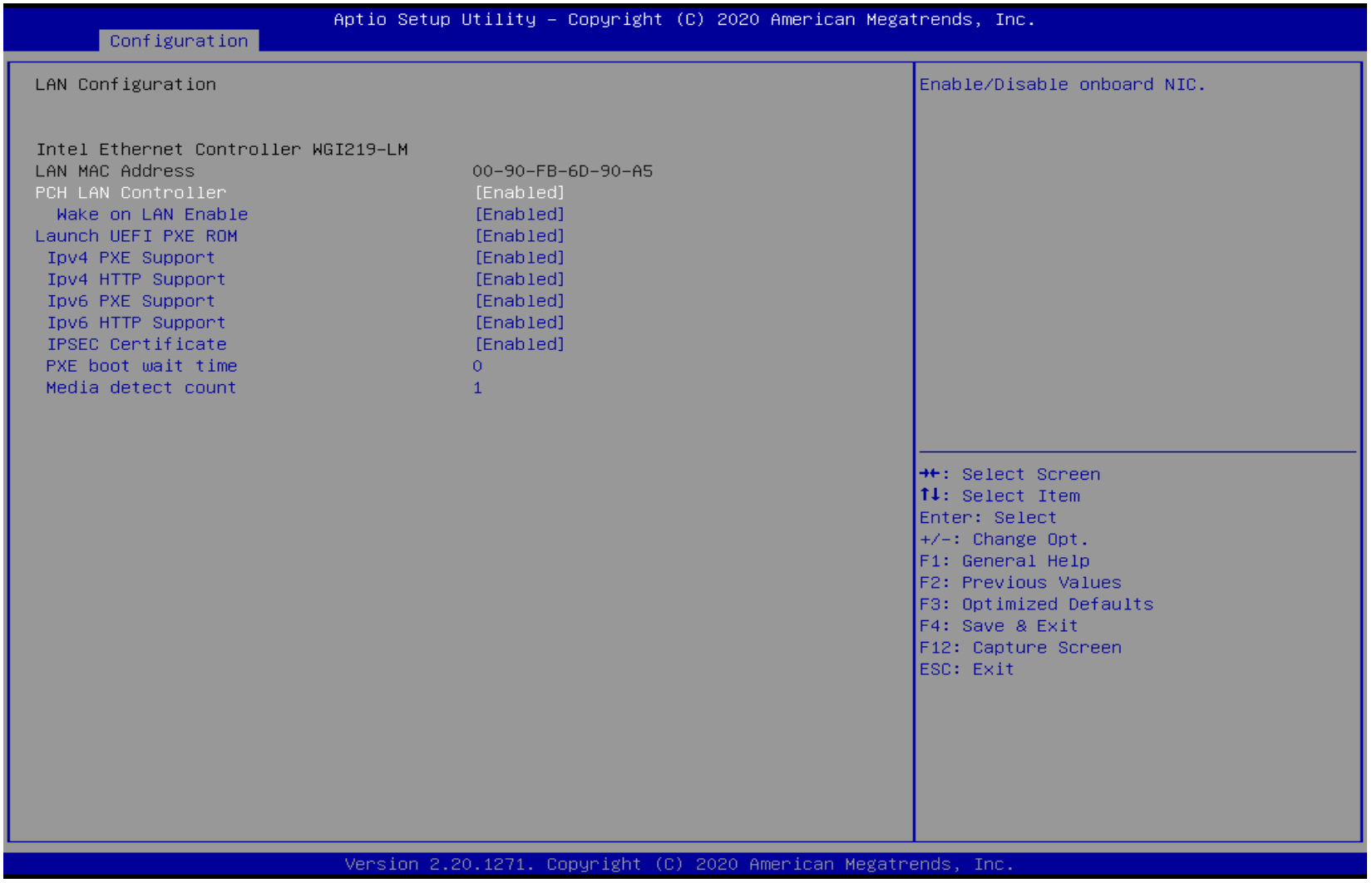


Figure 20 BIOS LAN Configuration

Feature	Description	Options
PCH LAN Controller	Enable/Disable onboard NIC	★Enabled , Disabled
Wake on LAN Enable	Enable/Disable integrated LAN to wake the system.	★Enabled , Disabled
Launch UEFI PXE ROM	Enable/Disable UEFI Network Stack	★Disabled, Enabled
Launch UEFI PXE ROM[Enable]		
Ipv4 PXE Support	Enable/Disable Ipv4 PXE boot support. If disable, IPv4 PXE boot support will not be available.	★Enabled, Disabled
Ipv4 HTTP Support	Enable/Disable Ipv4 HTTP boot support. If disable, IPv4 HTTP boot support will not be available.	★Enabled, Disabled
Ipv6 PXE Support	Enable/Disable Ipv6 PXE boot support. If disable, IPv6 PXE boot support will not be available.	★Enabled, Disabled
Ipv6 HTTP Support	Enable/Disable Ipv6 HTTP boot support. If disable, IPv6 HTTP boot support will not be available.	★Enabled, Disabled
IPSEC Certificate	Support to Enable/Disable IPSEC certificate for Ikev	★Enabled, Disabled
PXE boot wait time	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the values	★0
Media detect count	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the values.	★1

Table 25BIOS LANDescription

6.10 SATA Configuration

SATA Device Options Settings

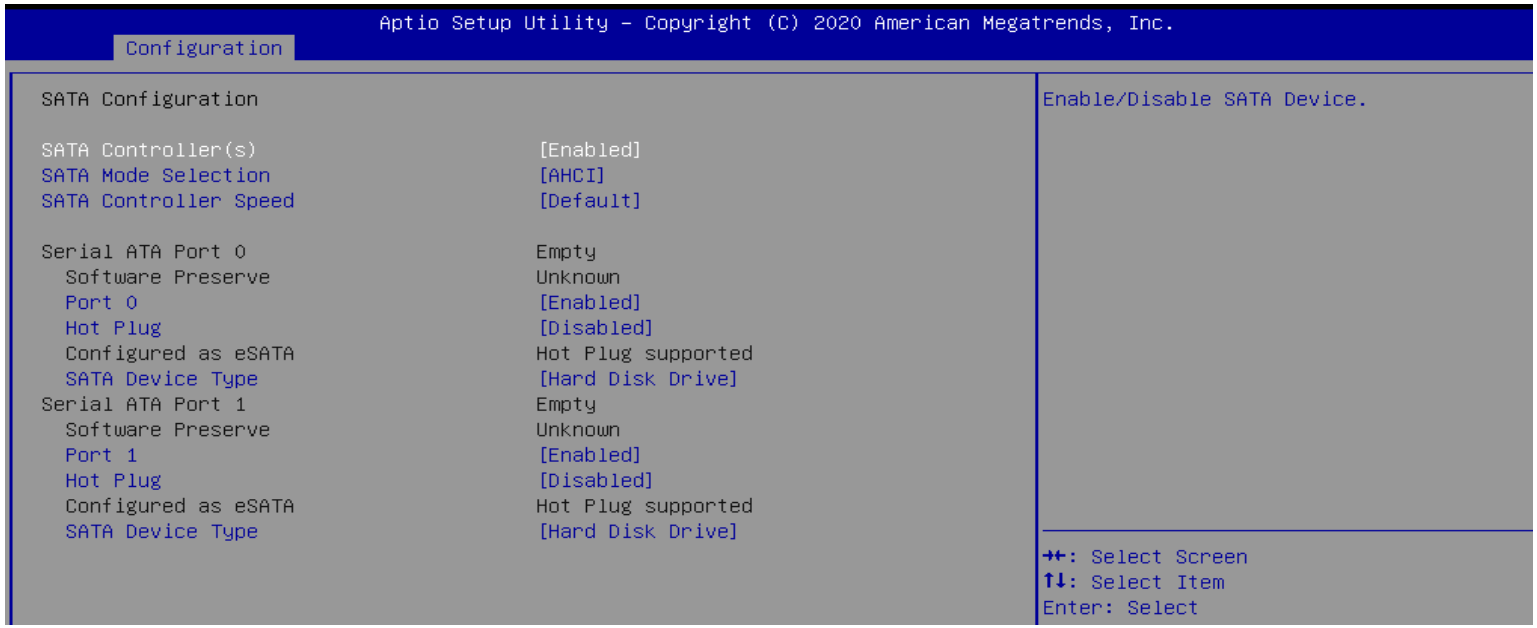


Figure 21BIOS SATA Configuration

Feature	Description	Options
SATA Controller(s)	Enable/Disable SATA Device	★Enabled , Disabled
SATA Mode Selection	Determines how SATA controller(s) operate.	★AHCI,RAID
SATA Controller Speed	Indicates the maximum speed the SATA controller can support	★Default,Gen1,Gen2,Gen3
Serial ATA Port 0/1		
Port 0/1	Enable or Disable SATA Port	★Enabled ,Disabled
Hot Plug	Designates this port as Hot Pluggable	★Disabled, Enabled
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive	★Hard Disk Drive, Solid State Drive

Table 26BIOS SATADescription

6.11 USB Configuration

USB Configuration Parameters

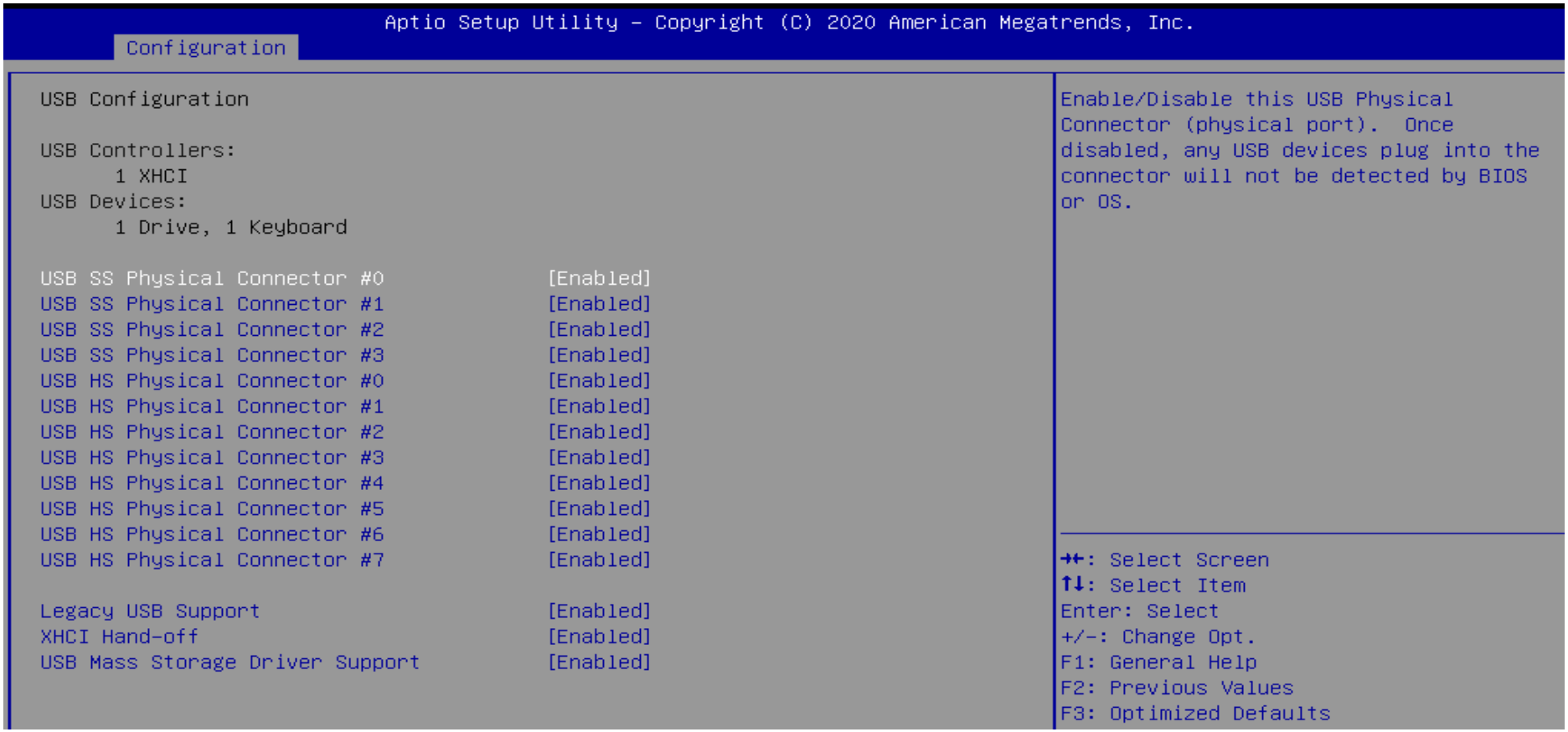


Figure 22BIOS USB Configuration

Feature	Description	Options
USB SS/HS Physical Connector #0~7	Enable/Disable this USB Physical Connector (physical port). Once disable, any USB devices plug into the connector will not be detected by BIOS or OS.	★Enabled ,Disabled
Legacy USB Support	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI application	★Enabled , Disabled, Auto
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver	★Enabled , Disabled
USB Mass Storage Driver Support	Enable/Disable USB Mass Storage Driver Support	★Enabled , Disabled

Table 27BIOS USB Description

6.12 TPM Configuration

Trusted Computing Setting

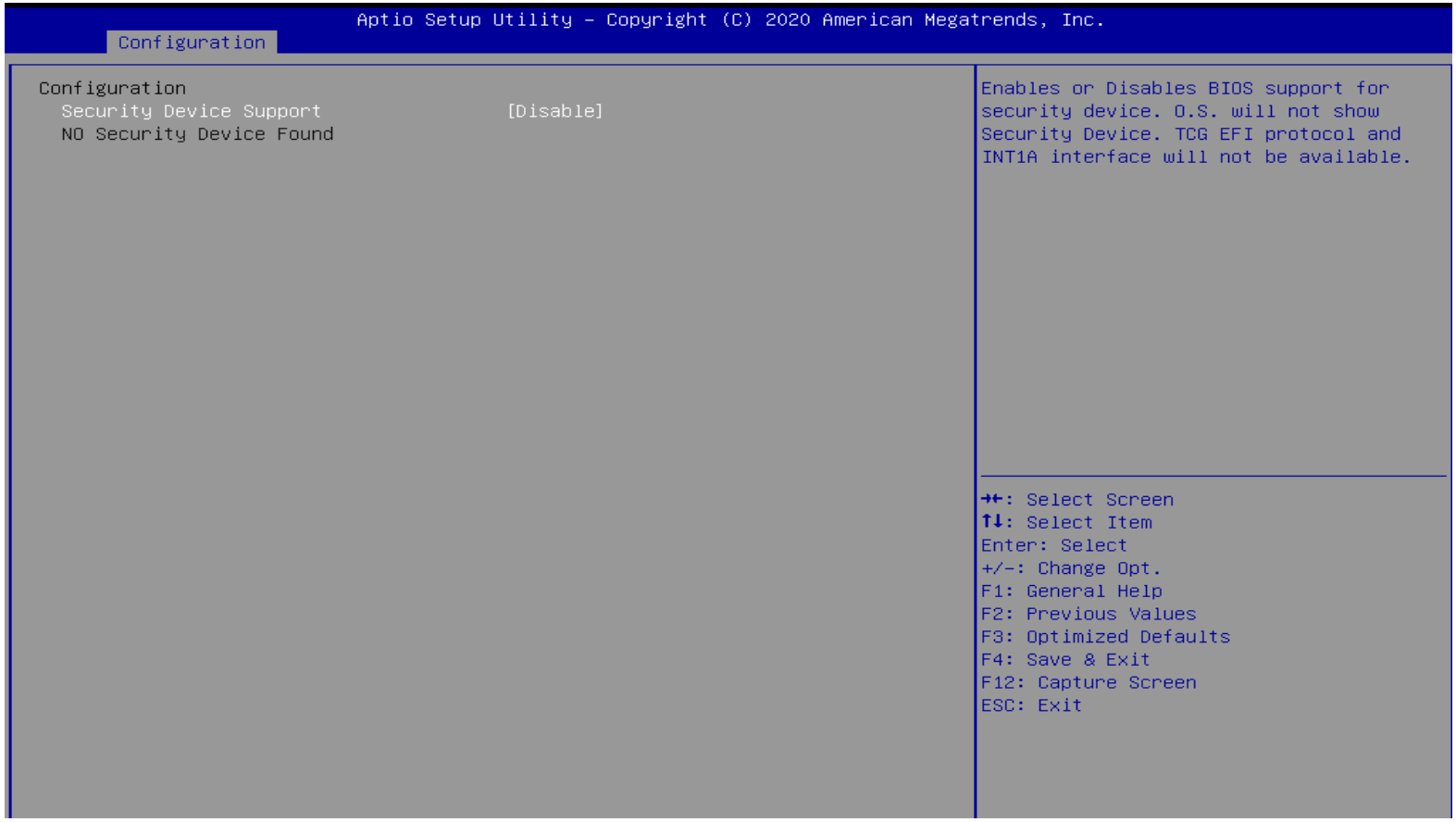


Figure 23 BIOS TPM Configuration

Feature	Description	Options
Security Device Support	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A Interface will not be available.	★Disabled, Enabled

Table 28 BIOS TPM Description

6.13 Super IO Configuration

System Super IO Chip Parameters.

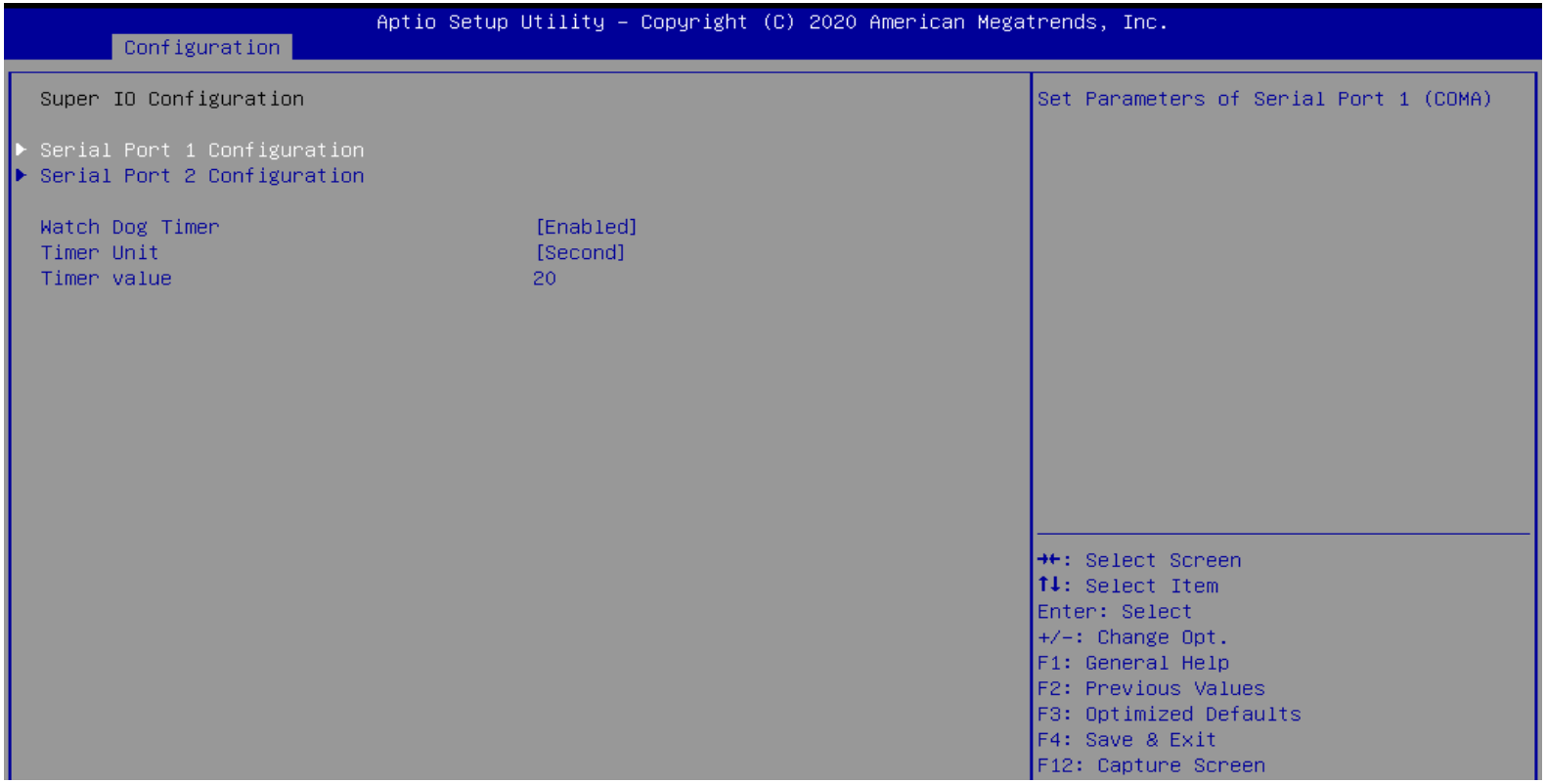


Figure 24 BIOS Super IO Configuration

Feature	Description	Options
Watch Dog Timer	Enable/Disable Watch Dog Timer	★Disabled, Enabled
Watch Dog Timer[Enable]		
Timer Unit	Select Timer count unit of WDT	★Second, Minute
Timer value	Set WDT Timer value seconds/minutes	★20

Table 29 BIOS Super IO Description

Serial Port 1 Configuration

Set Parameters of Serial Port 1 (COM A)

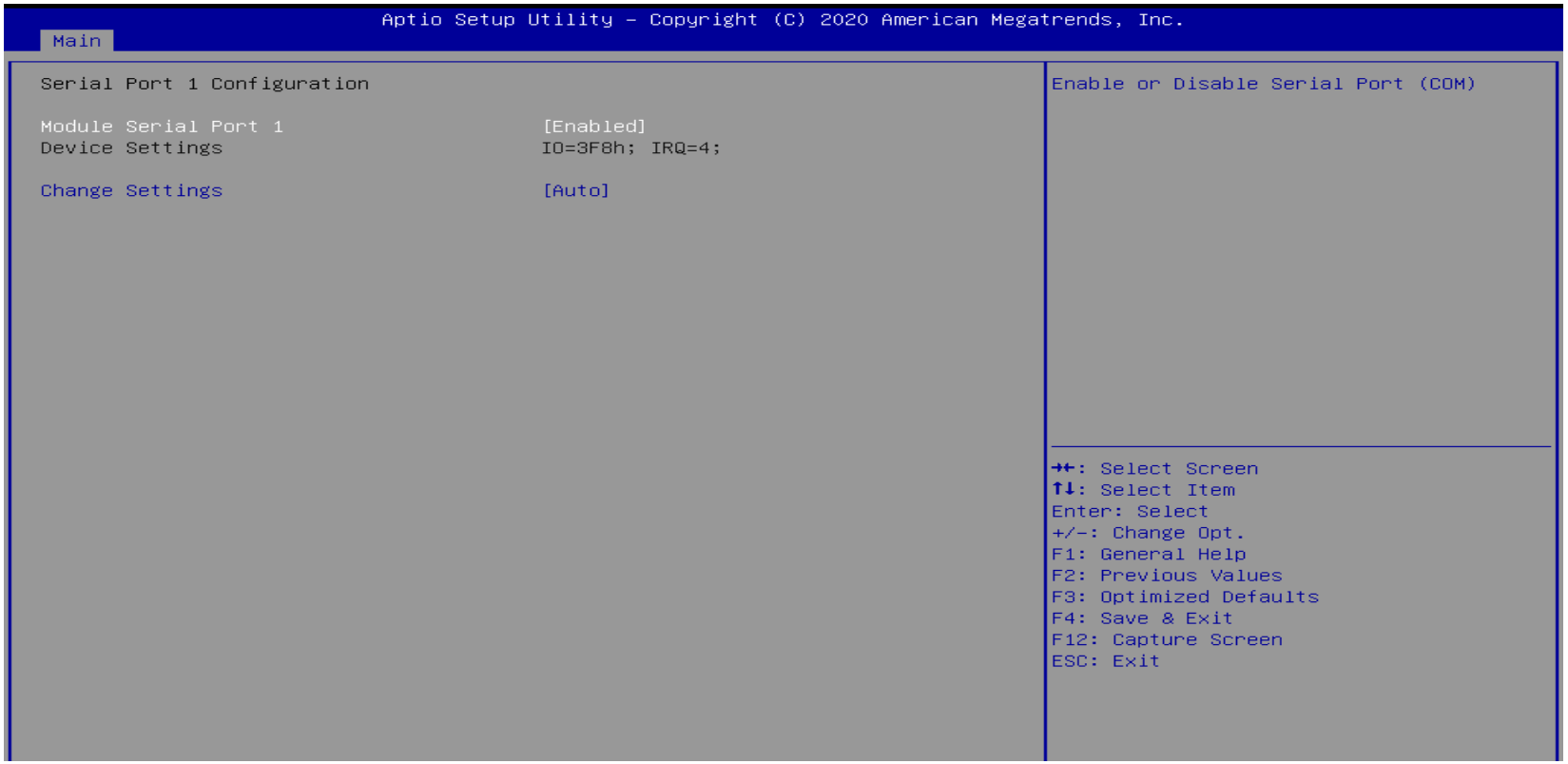


Figure 25 BIOS Serial Port 1 Configuration

Feature	Description	Options
Module Serial Port 1	Enable or Disable Serial Port (COM)	★Enabled, Disabled
Change Settings	Select an optimal settings for Super IO Device	★Auto ,IO=3F8h; IRQ=4, IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12

Table 30 BIOS Serial Port 1 Description

Serial Port 2 Configuration

Set Parameters of Serial Port 2 (COM B)

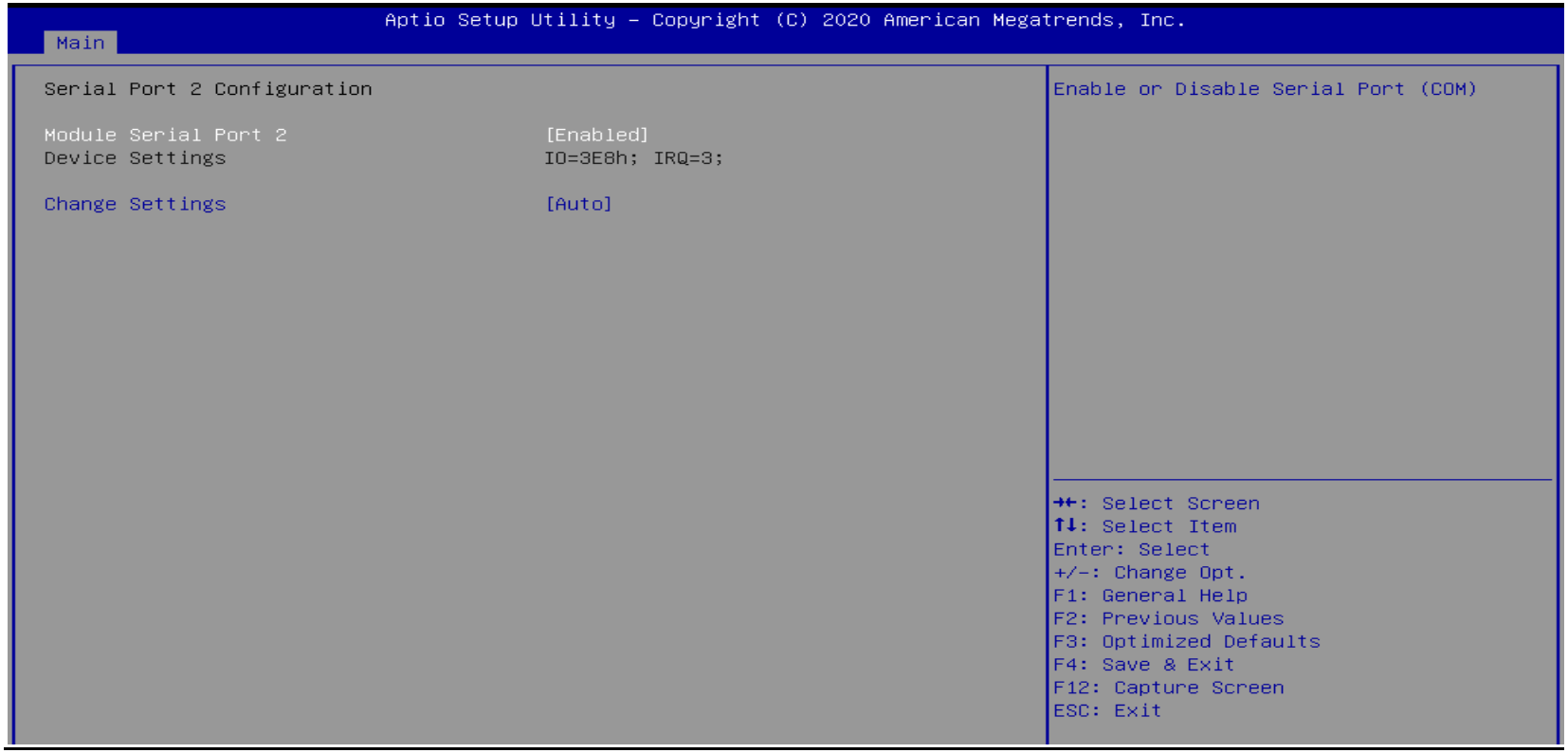


Figure 26BIOS Serial Port 2 Configuration

Feature	Description	Options
Serial Port	Enable or Disable Serial Port (COM)	★Enabled, Disabled
Change Settings	Select an optimal settings for Super IO Device	★Auto,IO=3E8h; IRQ=3, IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12 IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12 IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12

Table 31 BIOS Serial Port 2 Description

6.14 H/W Monitor

Monitor hardware status

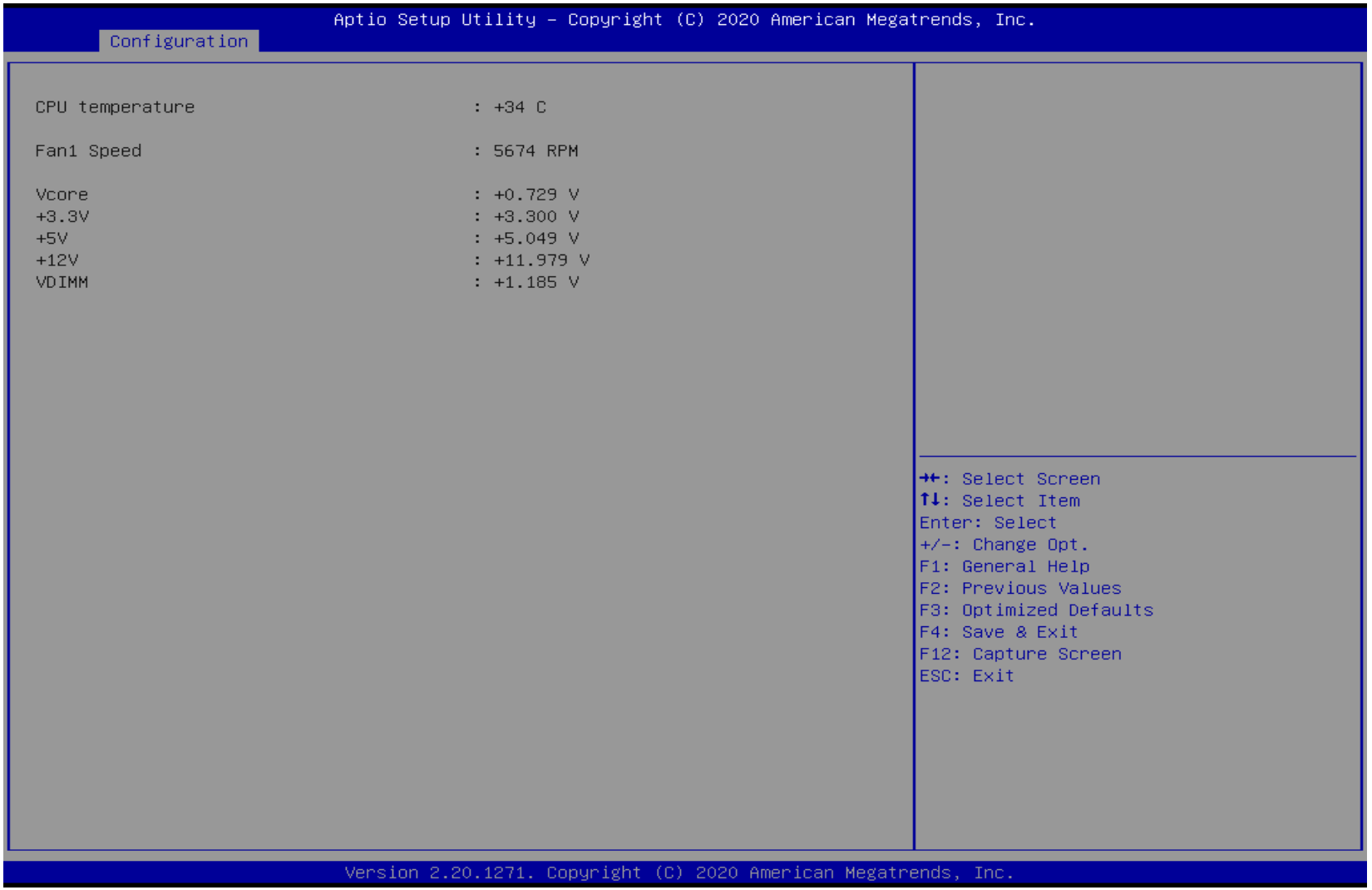


Figure 27 BIOS H/W MONITOR

6.15 Serial Port Console Redirection

Serial Port Console Redirection

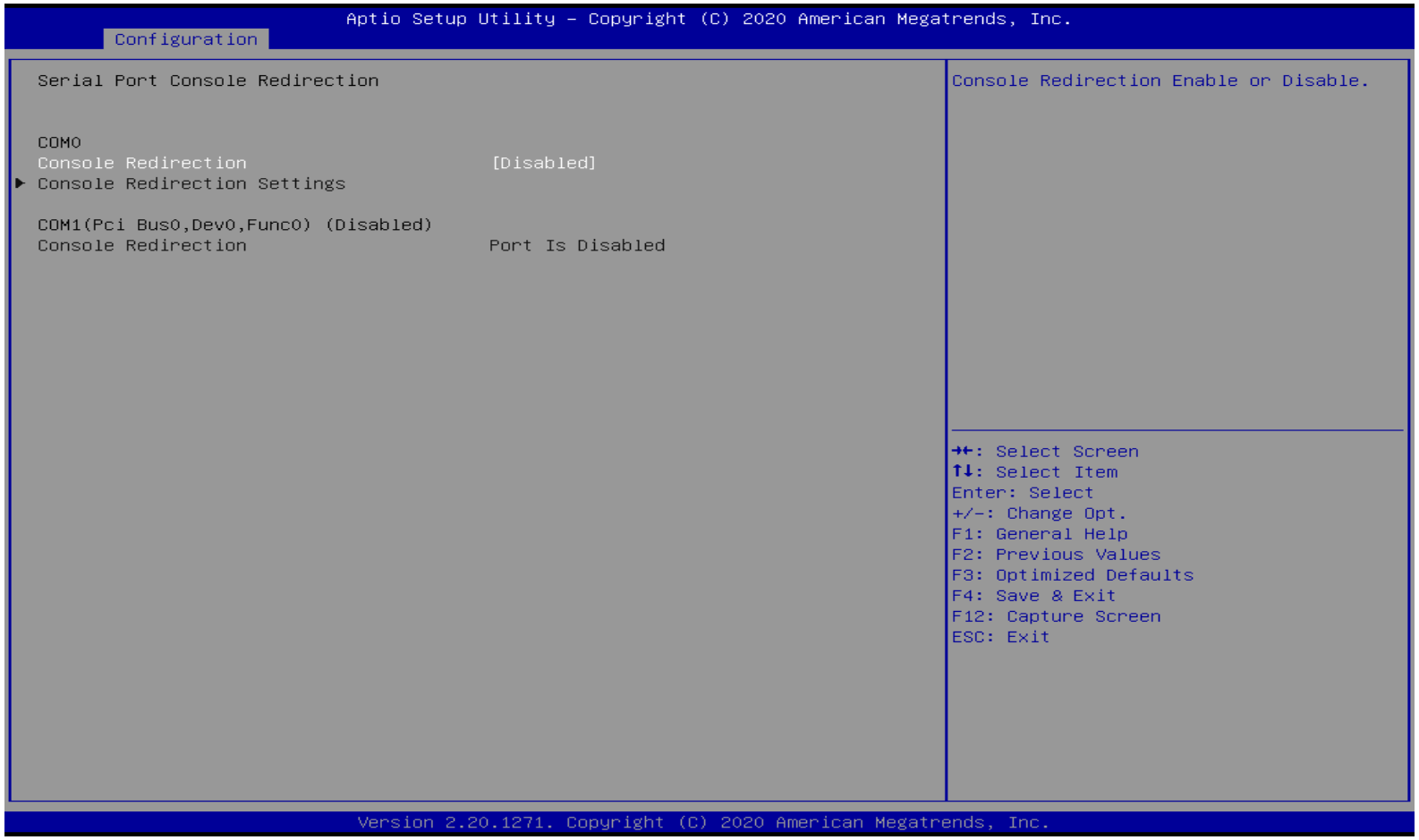


Figure 28BIOS Serial Port Console Redirection

Feature	Description	Options
Console Redirection	Console Redirection Enable or Disable	★Disabled, Enabled

Table 32 BIOS Serial Port Console Description

Console Redirection Settings

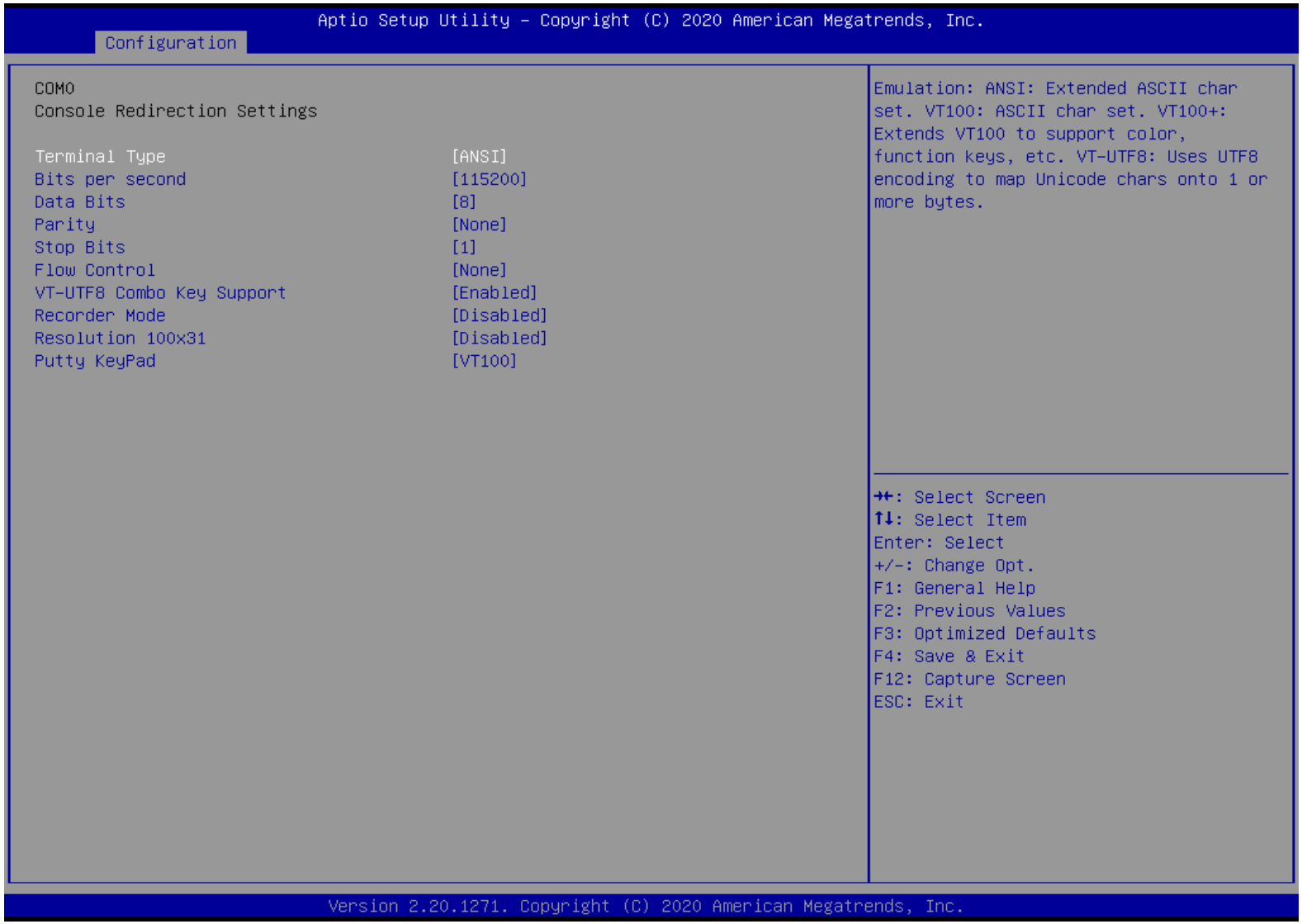


Figure 29BIOS Console Redirection Settings

Feature	Description	Options
Terminal Type	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	★ANSI, VT100, VT100+, VT-UTF8
Bits per second	Select Serial port transmission speed. The speed must be matched on other side. Long or noisy lines may require lower speeds.	★115200, 9600, 19200, 38400, 57600
Data Bits	Data Bits	★8, 7
Parity	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.	★None, Even, Odd, Mark, Space
Stop Bits	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	★1,2
Flow Control	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	★None, Hardware RTS/CTS
VT-UTFB Combo Key Support	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	★Enabled, Disabled
Recorder Mode	With this mode enabled only text will be sent. This is to capture Terminal data.	★Disabled, Enabled
Resolution 100x31	Enables or disables extended terminal resolution	★Disabled, Enabled
Putty KeyPad	Select FunctionKey and KeyPad on Putty	★VT100, LINUX,XTERMR6, SCO,ESCN,VT400

Table 33BIOS Console Redirection Description

6.16 Security

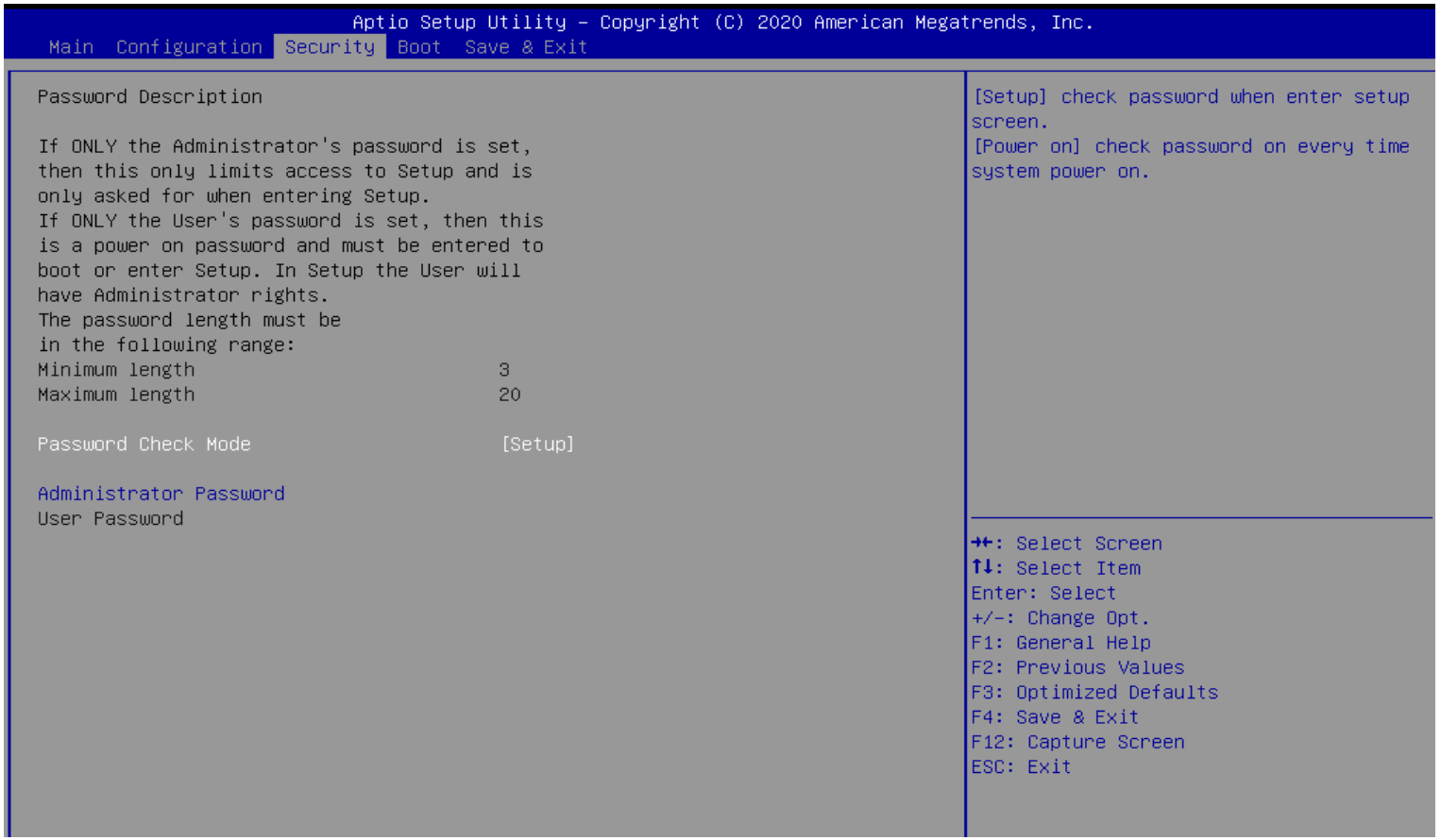


Figure 30BIOS Security

Feature	Description	Options
Password Check Mode	[Setup] check password when enter setup screen. [Power on] check password on every time system power on.	★Setup, Power on
Administrator Password	Set Administrator Password	

Table 34BIOS Security Description

6.17 Boot

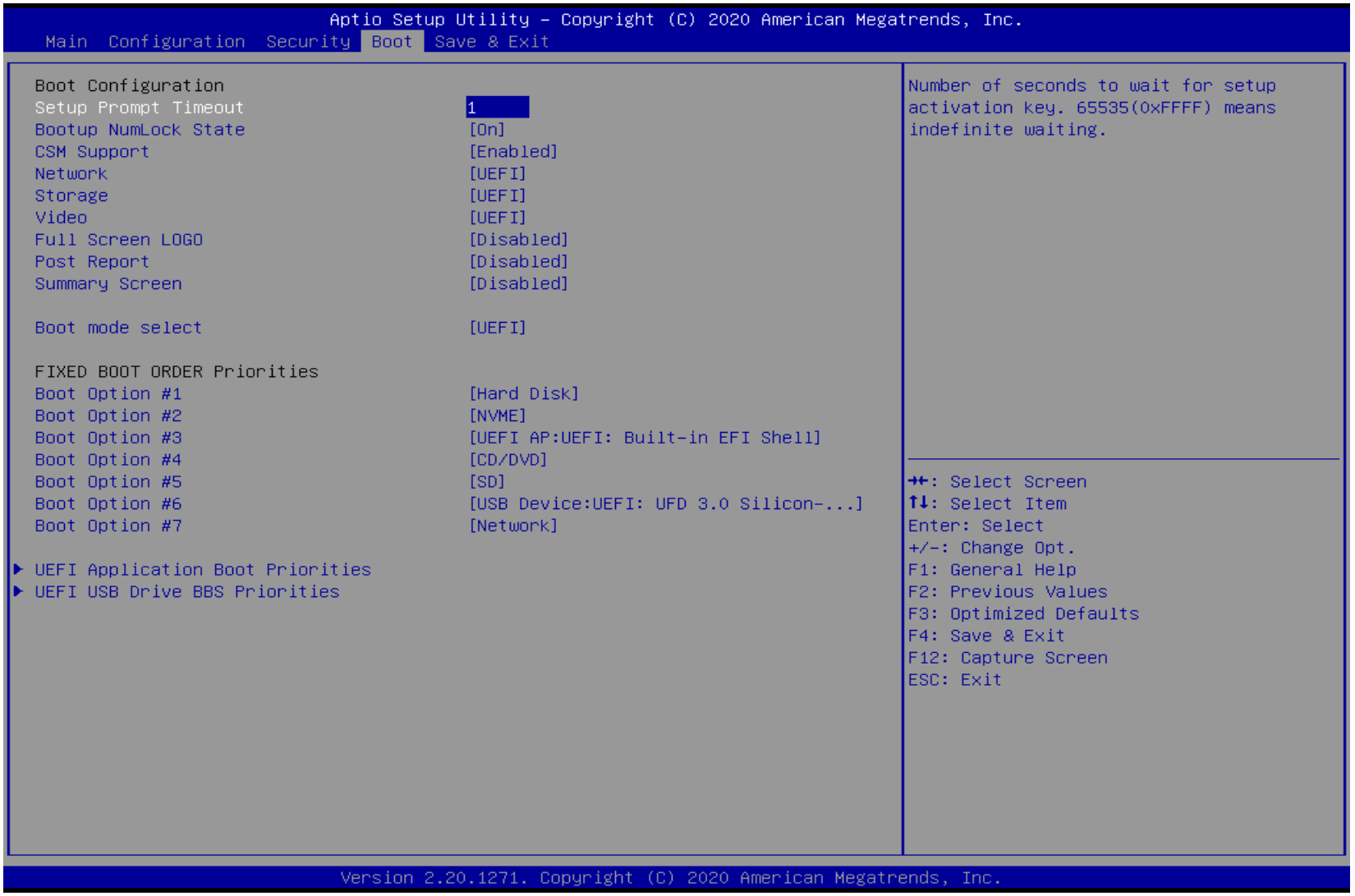


Figure 31 BIOS Boot

Feature	Description	Options
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.	★1
Bootup NumLock State	Select the keyboard NumLock state	★On, Off
CSM Support	Enable/Disable CSM support	★Disabled, Enabled
CSM Support[Enable]		
Network	Controls the execution of UEFI and Legacy Network OpROM	★UEFI, Do not launch, Legacy
Storage	Controls the execution of UEFI and Legacy Storage OpROM	★UEFI, Do not launch, Legacy
Video	Controls the execution of UEFI and Legacy Video OpROM	★UEFI, Do not launch, Legacy
Full Screen LOGO	Enables or disables Quiet Boot option and Full Screen LOGO.	★Disabled, Enabled
Post Report	Post Report Support Enabled/Disabled	★Disabled, Enabled
Summary Screen	Summary Screen Support Enabled/Disabled	★Disabled, Enabled
Boot mode select	Select boot mode LEGACY/UEFI	★UEFI ,Legacy
Boot Option #1~7	Sets the system boot order	★Hard Disk, NVME,UEFI AP, CD/DVD,SD,USB Device, Network, Disabled
UEFI Application Boot Priorities	Specifies the Boot Device Priority sequence from available UEFI Application	

Table 35BIOS Boot Description

6.18 Save & Exit

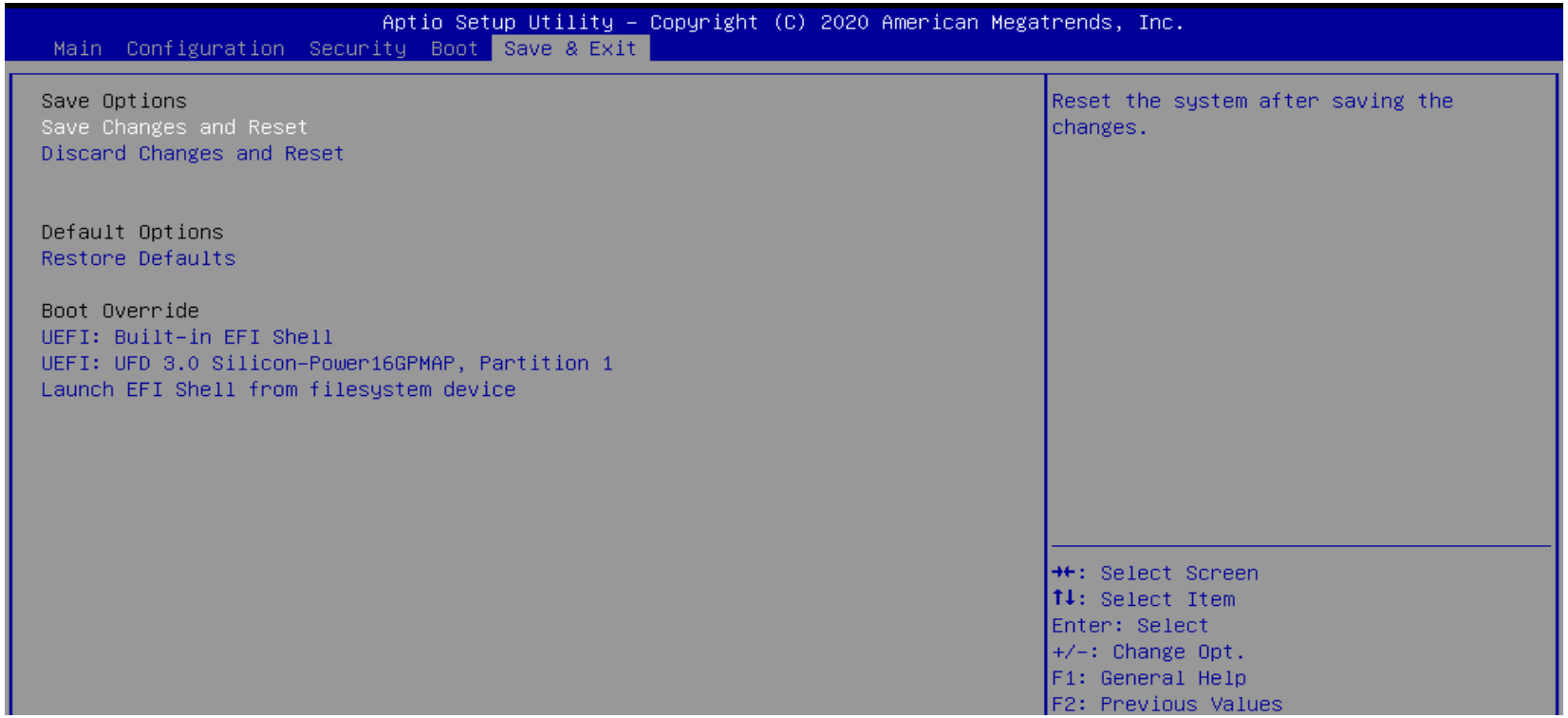


Figure 32 BIOS Save & Exit

Feature	Description	Options
Save Changes and Reset	Reset the system after saving the changes.	
Discard Changes and Reset	Reset system setup without saving any changes.	
Restore Defaults	Restore/Load Default values for all the setup options.	
UEFI: Built-in EFI Shell	Reset the system after saving the changes. (Boot option filter: UEFI only)	
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shell.efi) from one of the available filesystem devices.	

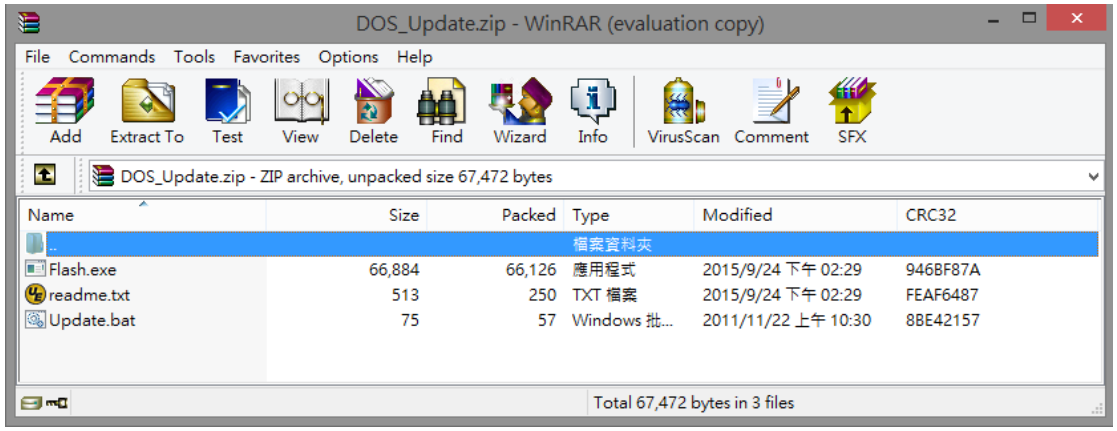
Table 36BIOS Save & Exit Description

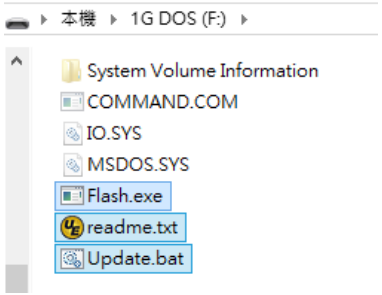
7 BIOS Update

BIOS/EC DOS Update SOP process

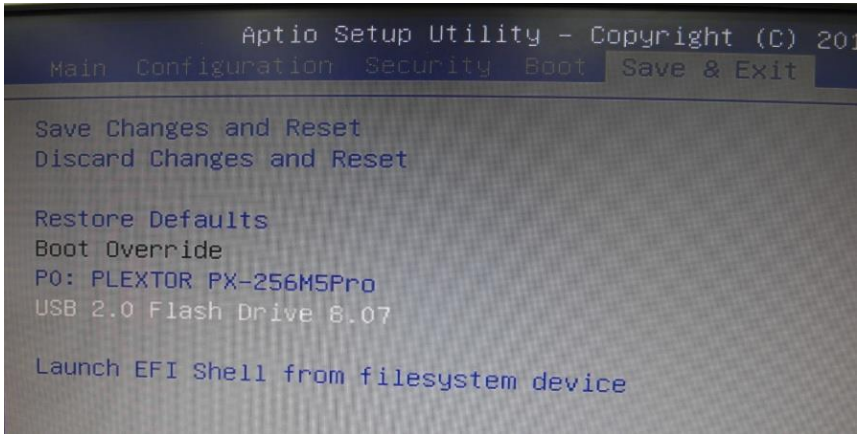
Step 1. Create a DOS USB DOK (Caution : Must be FAT or FAT32 format).

Step 2. Unzip update file to the DOS USB DOK.

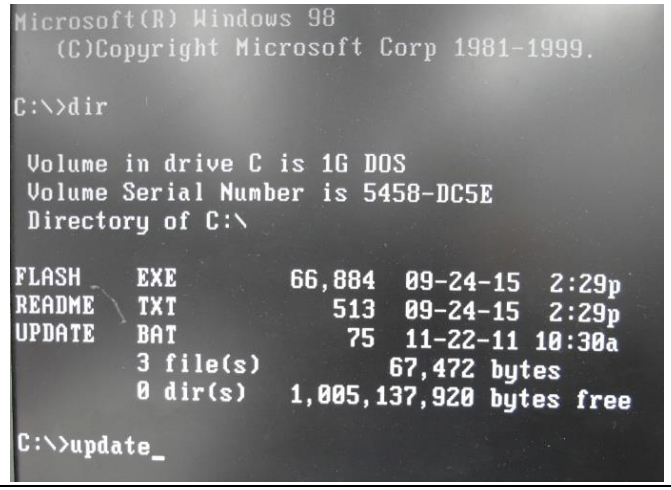




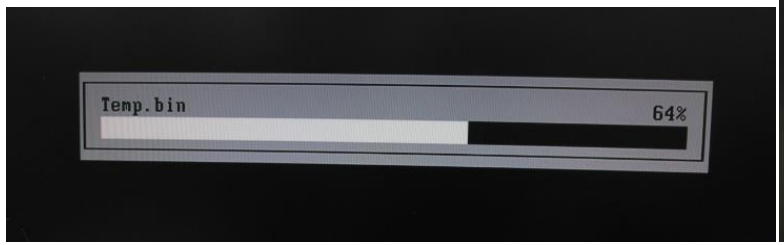
Step 3. Plug the DOS USB DOK to the target system and boot from the DOS USB DOK.

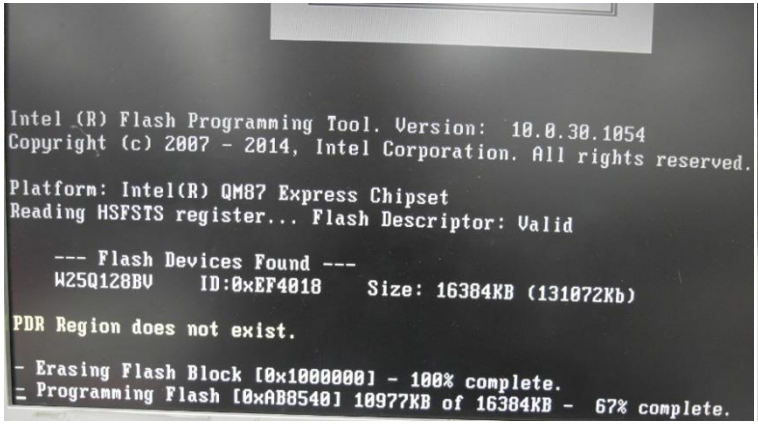


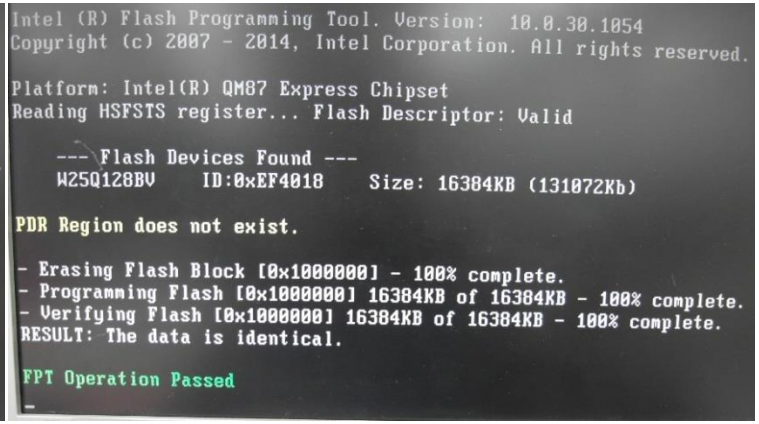
Step 4. Under the update file folder, type command : "update" and press enter.



Step 5. The update process will start and you can see the update progress. Once finished, please power off and restart the system.





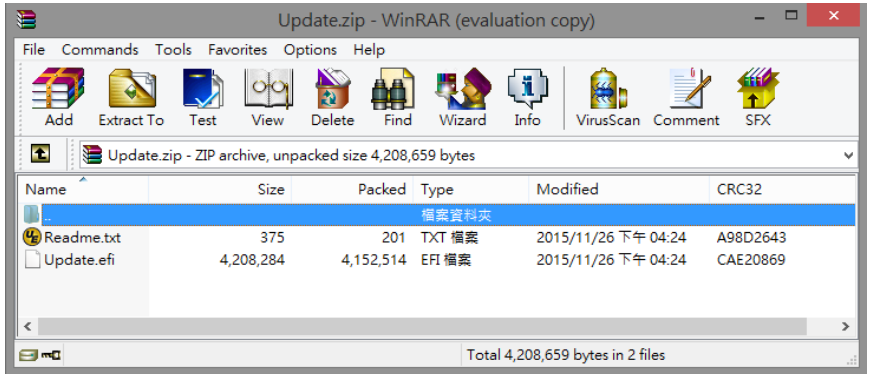


<End of BIOS/EC DOS update process>

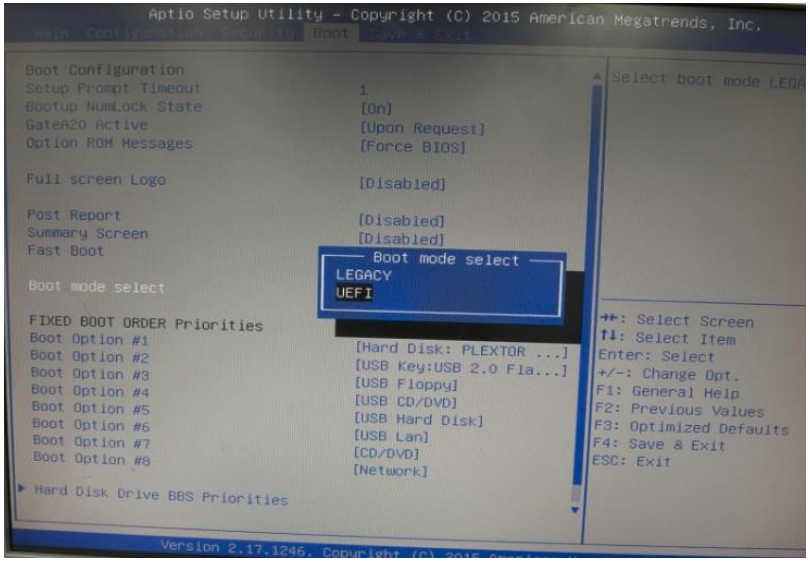
BIOS/EC UEFI Update SOP process

Step 1. Prepare a USB DOK (Caution : Must be FAT or FAT32 format).

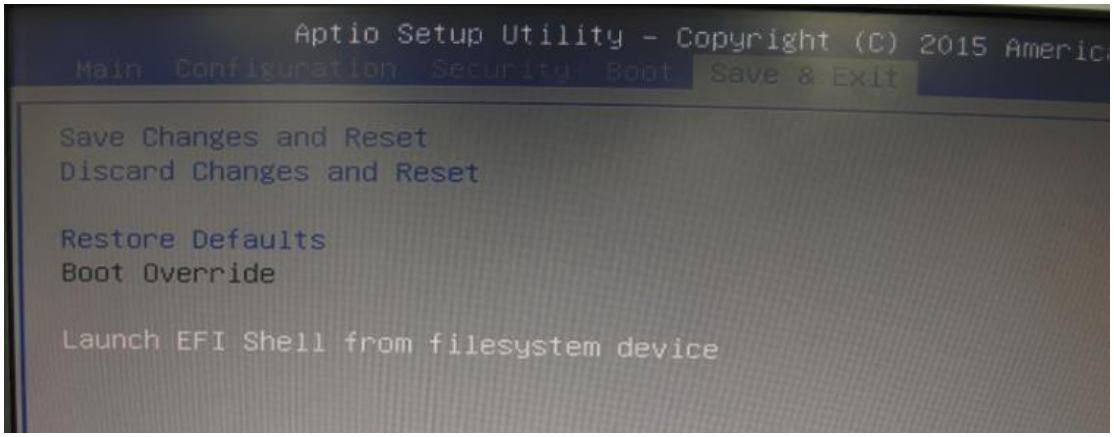
Step 2. Unzip update file to the USB DOK.



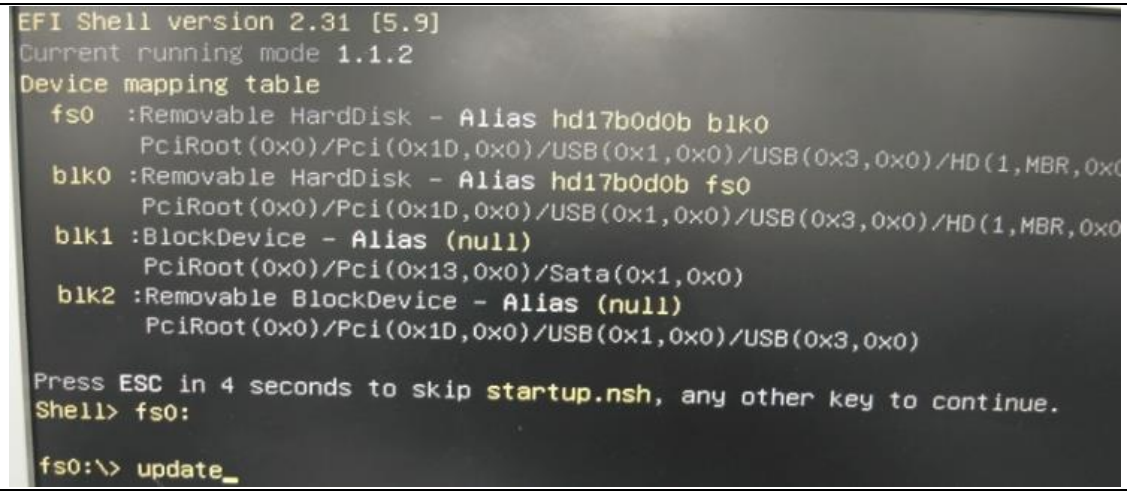
Step 3. Select UEFI boot mode in the BIOS boot menu and save, then restart the system.



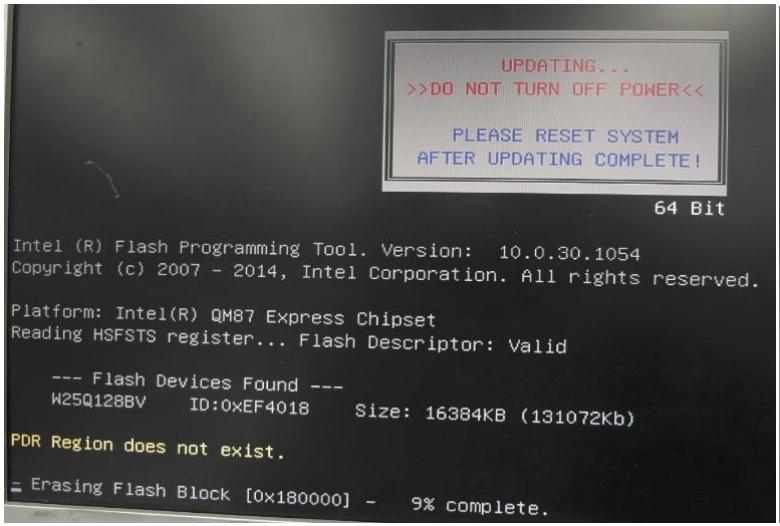
Step 4. Plug the USB DOK to the target system and boot from UEFI Shell.

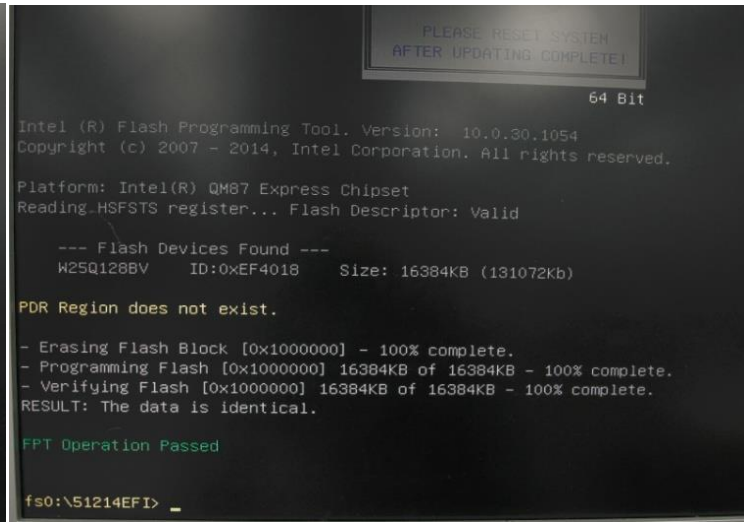


Step 5. Under the UEFI shell, direct to your USB DOK, below example fs0 and type command : "update" and press enter.



Step 6. The update process will start and you can see the update progress. Once finished, please power off and restart the system.





<End of BIOS/EC UEFI update process>

8 PORTWELL Software Tool

PORTWELL Evaluation Tool (PET)

The PORTWELL Evaluation Tool (PET) is an API which PORTWELL's customers can access the GPIO, I2C, SMBus, etc under Windows and Linux OS. For more information please contact PORTWELL.

PORTWELL BIOS web Tool (PBT)

The PORTWELL BIOS web Tool (PBT) is a brand new on-line utility which innovated by PORTWELL. PBT now is available for PORTWELL's premiere customers who are able to add customized BIOS logo andchange BIOS default settings on American Megatrends (AMI) BIOS. Please contact PORTWELL for more information.

PORTWELL EC Auto Test Tool (PECAT)

The PORTWELL EC Auto Test Tool (PECAT) is a brand new utility which innovated by PORTWELL. PECAT now is available for PORTWELL's premiere customers, who are able to Test Embedded Controller Function in UEFI Mode. Please contact PORTWELL for more information.

9 Industry Specifications

The list below provides links to industry specifications that apply to PORTWELL modules.

Low Pin Count Interface Specification, Revision 1.0 (LPC)http://www.intel.com/design/chipsets/industry/lpc.htm
Universal Serial Bus (USB) Specification, Revision 2.0http://www.usb.org/home
Serial ATA Specification, Revision 3.0 http://www.serialata.org/
PICMG® COM Express Module™ Base Specification http://www.picmg.org/
PCI Express Base Specification, Revision 2.0 https://www.pcisig.com/specifications

10 Quick Start Guide

The PCOM-B653VGL Quick Start Guide illustrates the Module and accessories assemble processes, and also guides users how to power on the product and enter BIOS menu. The contents include heat sink / cooler and Module introduction, assembling of heat sink / cooler and Carrier, and debug message.

10.1 PCOM-B653VGL Introduction

This section introduces the Top and Bottom side of PCOM-B653VGL.

Top side of PCOM-B653VGL

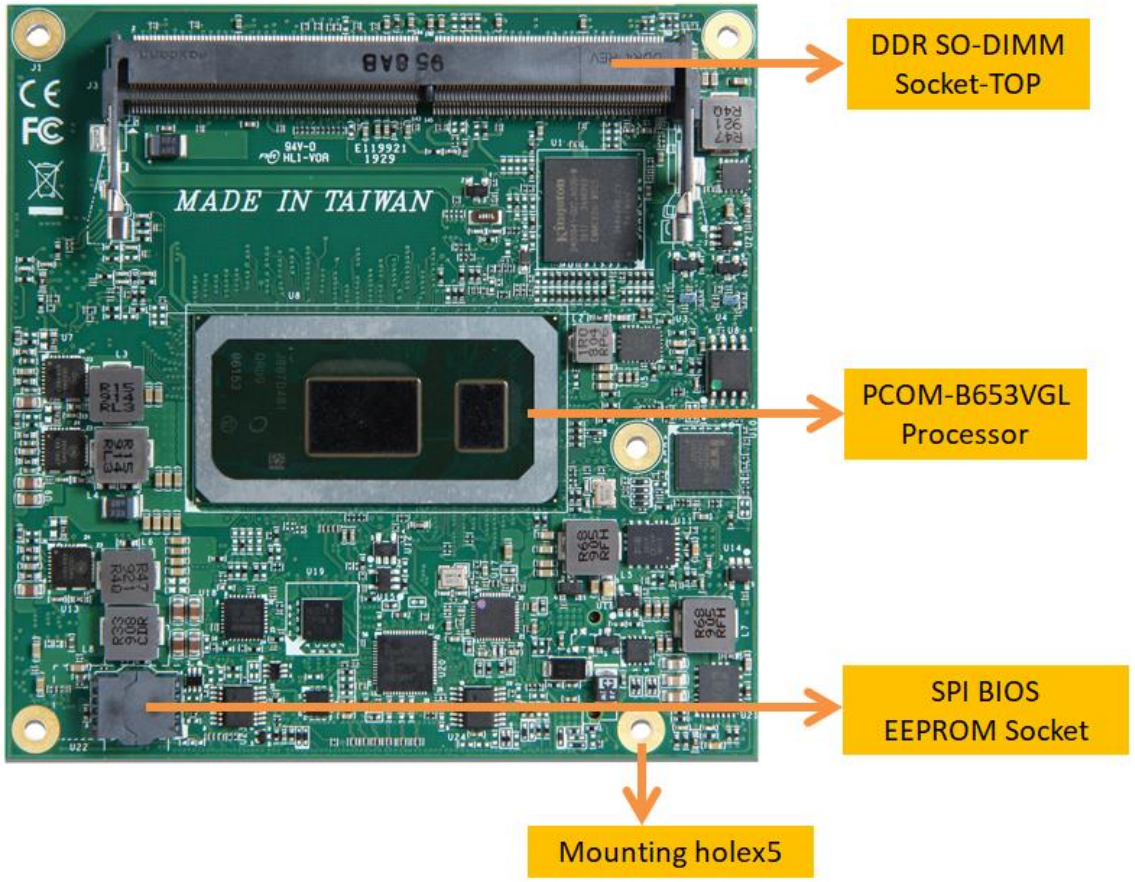


Figure 33 PCOM-B653VGL - Top

Bottom side of PCOM-B653VGL

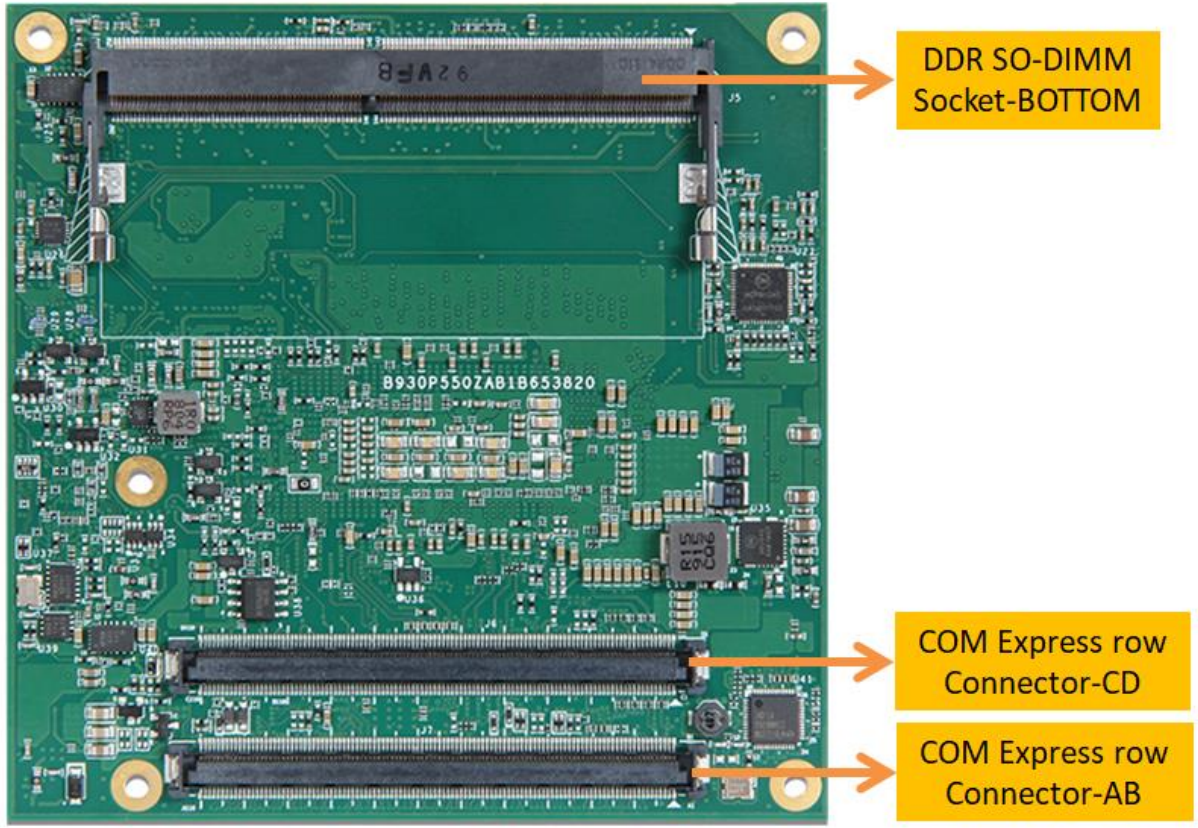


Figure 34 PCOM-B653VGL - Bottom

10.2 Cooler

The section introduces PCOM-B653VGL cooler.

Top view of PCOM-B653VGL cooler

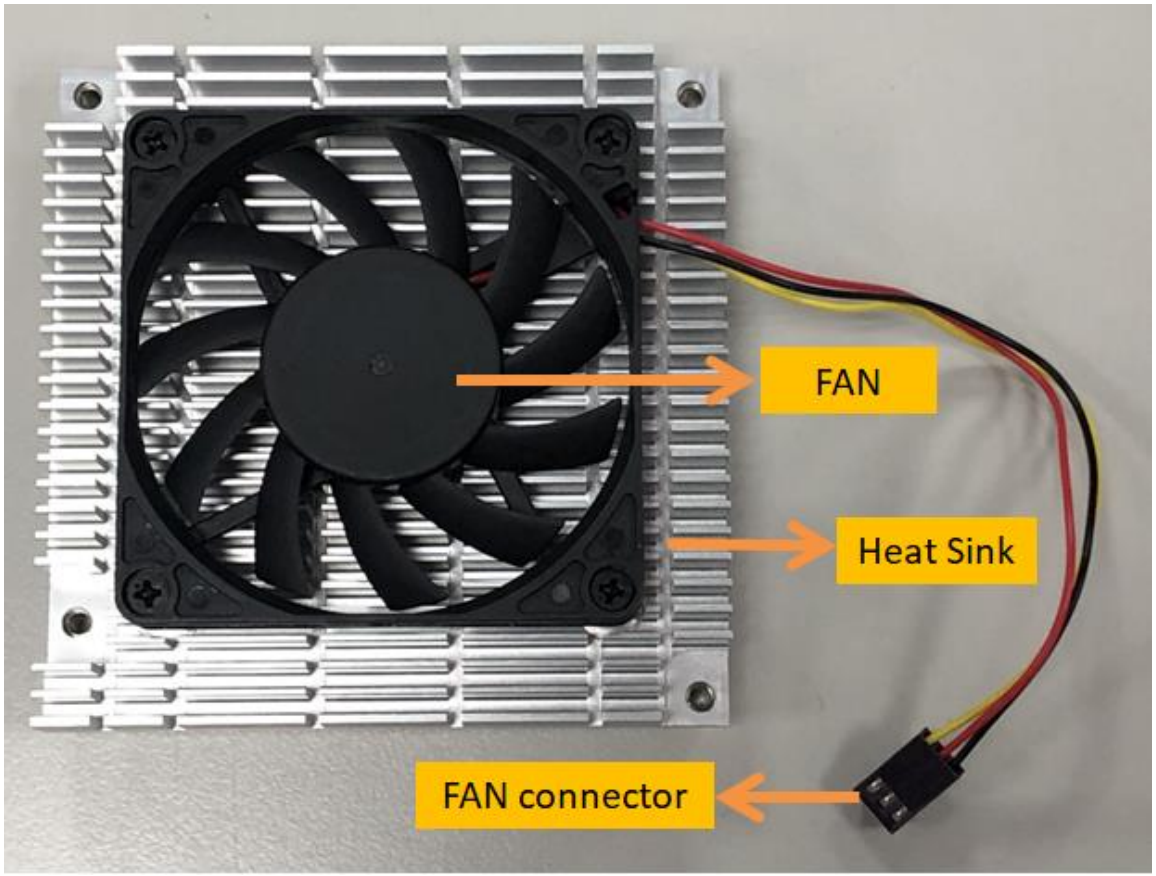


Figure 35 Cooler - Top

Bottom view of PCOM-B653VGL cooler

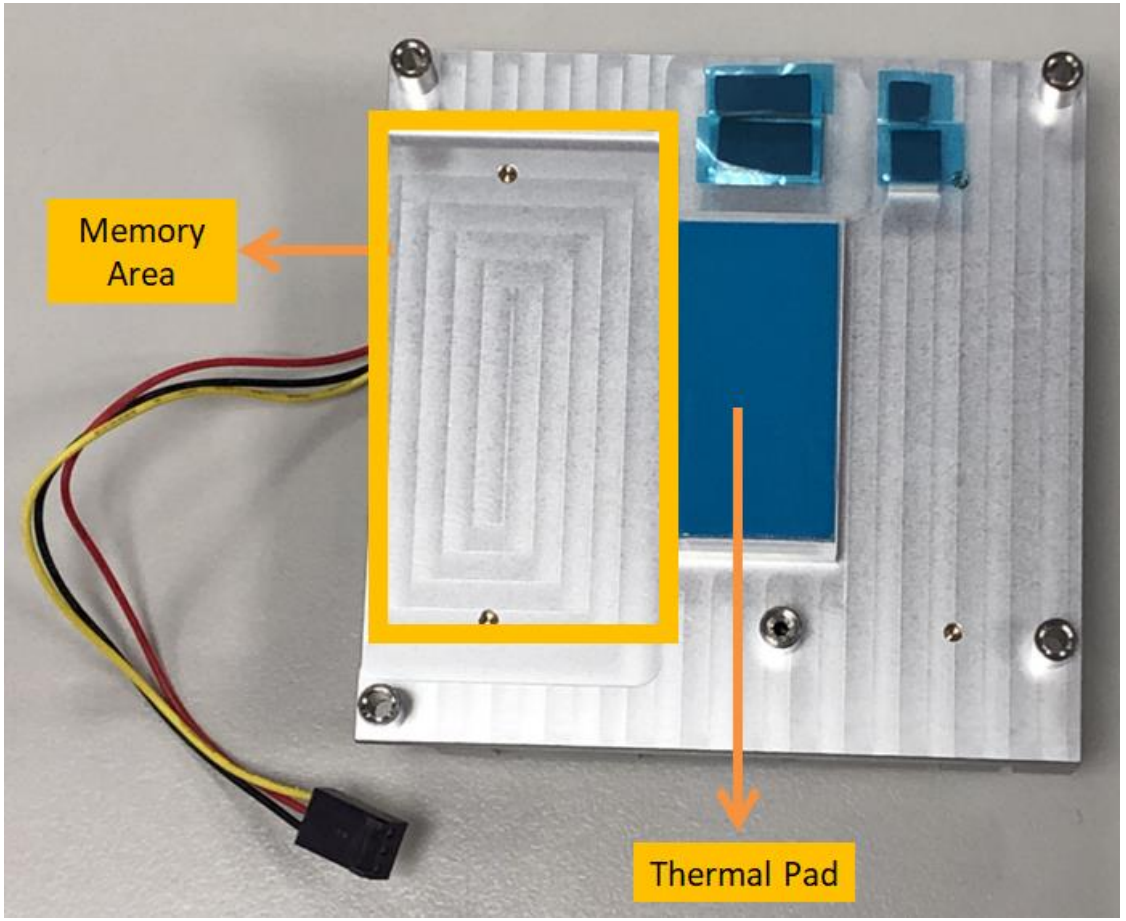


Figure 36 Cooler - Bottom

10.3 Accessory

This section presents PCOM-B653VGL cooler accessories.

1. Copper pillar M2.5 (Female) x5 pcs
2. Copper pillar M2.5 (Male) x5 pcs
3. Screws M2.5 x5 pcs

Figure 37M2.5 Female Copper pillar

Figure 38M2.5 Male Copper pillar M2.5

Figure 39M2.5 Screws

10.4 Assembly SOP

This section presents the step by step procedures for assembling PCOM-B653VGL, cooler and PCOM-C605 carrier.

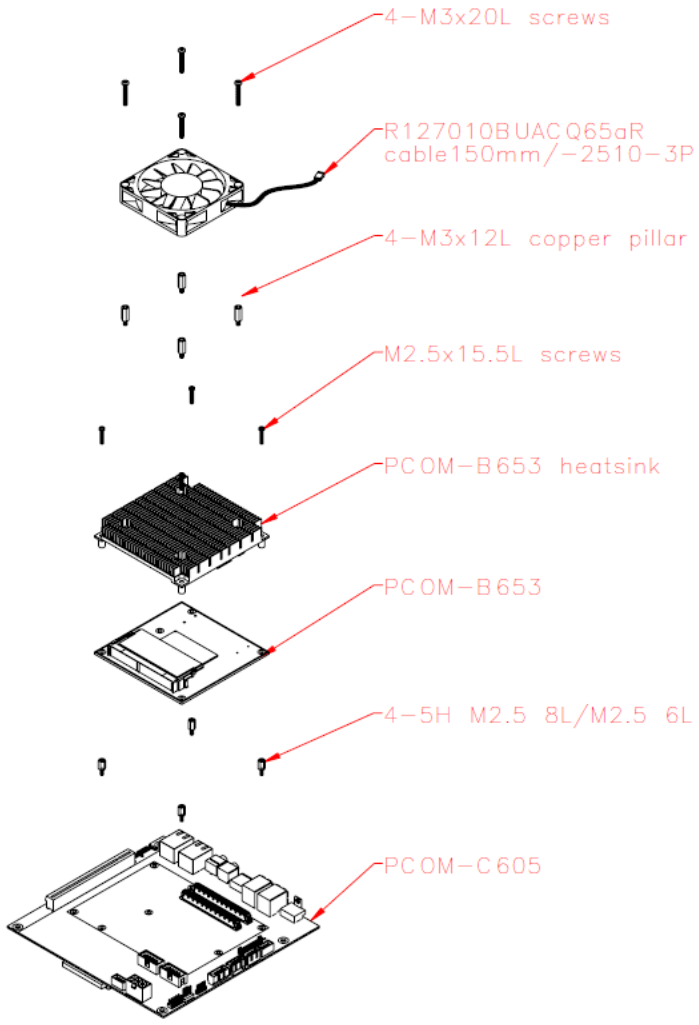


Figure 40 Assembly

Step 1

Accessories required :

1. PCOM-C605
2. Copper pillar M2.5 (Female) x4 pcs
3. Copper pillar M2.5 (Male) x4 pcs

Screws the 4 pcs Copper pillar M2.5 (Female) and 4 pcs Copper pillar M2.5 (Female) on the compact size position of PCOM-C605.

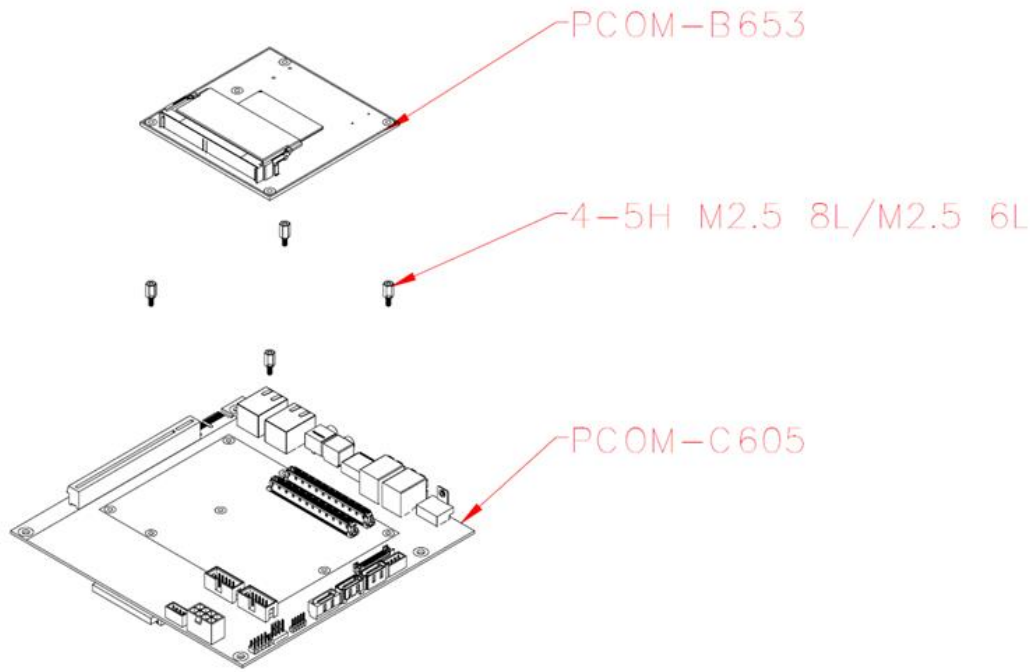


Figure 41 Assembly Step 1

Step 2

Accessories required :

1. PCOM-B653VGL x1
2. DDR4 Memory x1
3. Screws x4 pcs
4. PCOM-C605 x1

Screwing the PCOM-B653VGL(with DDR4 Memory connected) on PCOM-C605 from Step1 with 4 male M2.5 copper pillar.

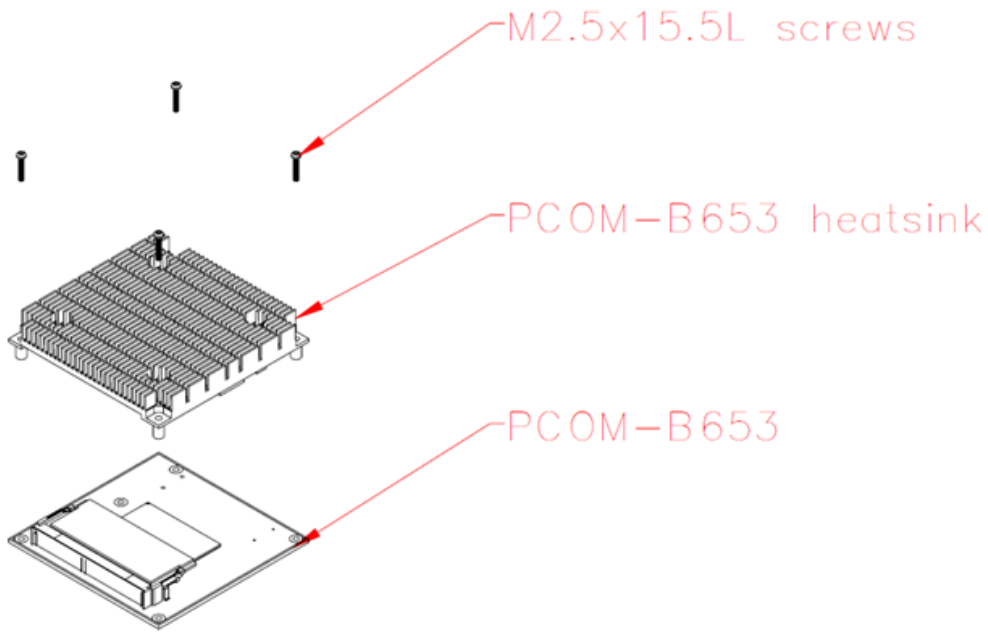


Figure 42 Assembly Step 2

10.5 Power ON

This section presents the required input voltage and how to power on PCOM-B653VGL.

The nominal DC input voltage is +12V, for powering on PCOM-B653VGL on PCOM-C605 Carrier with ATX power, make sure the PSON is low level, and connect the +12V cable to PCOM-C605 J21.

Auto Power ON

Every time PSU power on, PCOM-B653VGL will automatically boot.

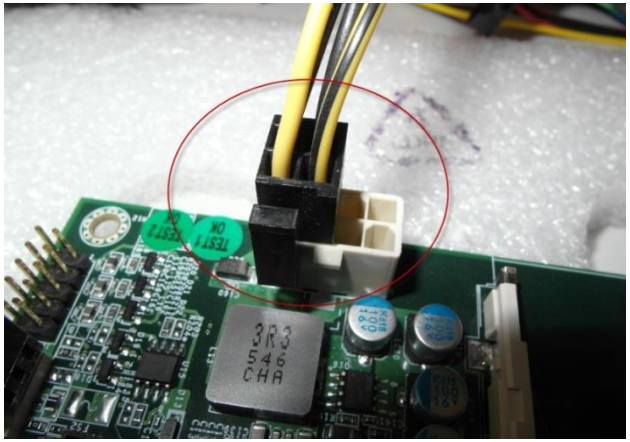


Figure 43PCOM-C605 +12V

BIOS Menu

After powering on, press Del on keyboard to enter BIOS menu, the BIOS version and EC version can be found.

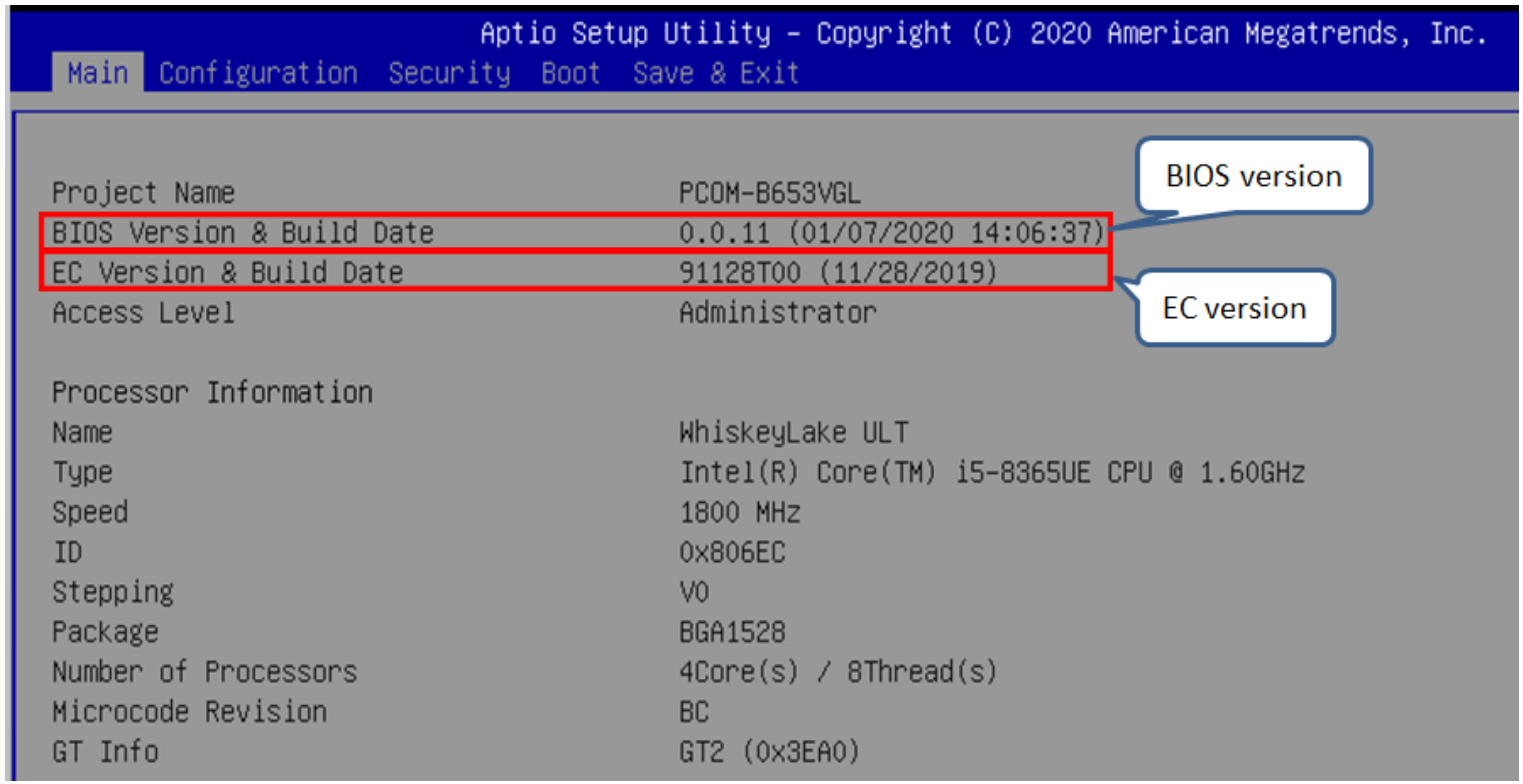


Figure 44 BIOS Menu

10.6 Debug message

This section presents the POST code of PCOM-B653VGL, users can check the POST code for boot procedure diagnostic.

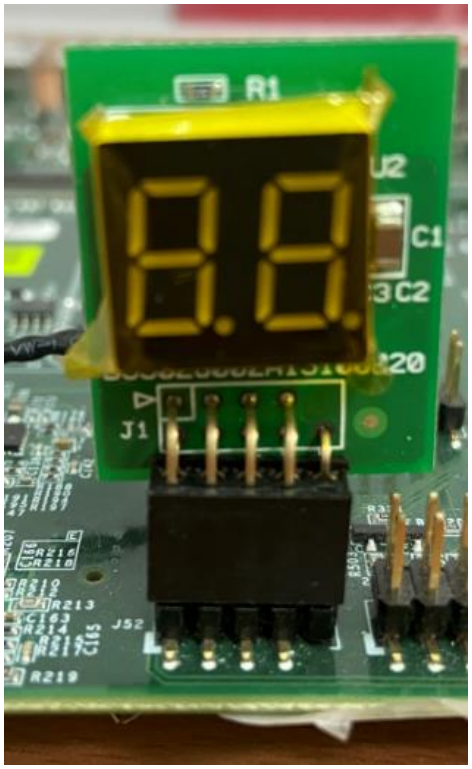


Figure 45 PCOM-B653VGL Header

PCOM-B653VGL POST code table can be found below for reference.

POST code	Description
0x10	PEI_CORE_STARTED
0x11	CPU Initialization

0x15	North Bridge Initialization
0x19	South Bridge Initialization
0x2B	Memory SPD
0x2C	MEMORY DETECT
0x2D	MEMORY TIMING
0x2E	MEMORY CONFIG
0x2F	MEMORY Initialization
0x31	MEMORY INSTALLED
0x32	CPU Initialization
0x33	CPU CACHE Initialization
0x34	CPU AP Initialization
0x35	CPU BSP Initialization
0x36	CPU SMM Initialization
0x37	MEMORY North Bridge Initialization
0x3B	MEMORY South Bridge Initialization
0x4F	DXE IPL
0x60	DXE CORE
0x61	DXE NVRAM
0x62	DXE South BridgeRUN
0x63	DXE CPU Initialization
0x68	DXE North Bridge HB Initialization
0x69	DXE North Bridge Initialization
0x6A	DXE North Bridge SMM Initialization
0x70	DXE South Bridge Initialization
0x71	DXE South Bridge SMM Initialization
0x72	DXE South Bridge DEVICES Initialization

0x78	DXE ACPI
0x79	DXE CSM
0x90	DXE BDS
0x91	DXE BDS CONNECT DRIVRES
0x92	DXE PCI BUS
0x93	DXE PCI BUS HPC
0x94	DXE PCI BUS ENUM
0x95	DXE PCI BUS REQUEST RESOURCES
0x96	DXE PCI BUS ASSIGN RESOURCES
0x97	DXE_CON_OUT_CONNECT
0x98	DXE_CON_IN_CONNECT
0x99	DXE_SIO_Initialization
0x9A	DXE_USouth Bridge_BEGIN
0x9B	DXE_USouth Bridge_RESET
0x9C	DXE_USouth Bridge_DETECT
0x9D	DXE_USouth Bridge_ENABLE
0xA0	DXE_IDE_BEGIN
0xA1	DXE_IDE_RESET
0xA2	DXE_IDE_DETECT
0xA3	DXE_IDE_ENABLE
0xA4	DXE_SCSI_BEGIN
0xA5	DXE_SCSI_RESET
0xA6	DXE_SCSI_DETECT
0xA7	DXE_SCSI_ENABLE
0xA8	DXE_SETUP_VERIFYING_PASSWORD
0xA9	DXE_SETUP_START

0xAB	DXE_SETUP_INPUT_WAIT
0xAD	DXE_READY_TO_BOOT
0xAE	DXE_LEGACY_BOOT
0xAF	DXE_EXIT_BOOT_SERVICES
0xB0	RT_SET_VIRTUAL_ADDRESS_MAP_BEGIN
0xB1	RT_SET_VIRTUAL_ADDRESS_MAP_END
0xB2	DXE_LEGACY_OPROM_Initialization
0xB3	DXE_RESET_SYSTEM
0xB4	DXE_USouth Bridge_HOTPLUG
0xB5	DXE_PCI_BUS_HOTPLUG
0xB6	DXE_NVRAM_CLEANUP
0xB7	DXE_CONFIGURATION_RESET
0xD0	DXE_CPU_ERROR
0xD1	DXE_North Bridge_ERROR
0xD2	DXE_South Bridge_ERROR,
0xD3	DXE_ARCH_PROTOCOL_NOT_AVAILABLE
0xD4	DXE_PCI_BUS_OUT_OF_RESOURCES
0xD5	DXE_LEGACY_OPROM_NO_SPACE
0xD6	DXE_NO_CON_OUT
0xD7	DXE_NO_CON_IN
0xD8	DXE_INVALID_PASSWORD
0xD9	DXE_BOOT_OPTION_LOAD_ERROR
0xDA	DXE_BOOT_OPTION_FAILED
0xDB	DXE_FLASH_UPDATE_FAILED
0xDC	DXE_RESET_NOT_AVAILABLE
0xE0	PEI_S3_STARTED

0xE1	PEI_S3_BOOT_SCRIPT
0xE2	PEI_S3_VIDEO_REPOST
0xE3	PEI_S3_OS_WAKE
0xF0	PEI_RECOVERY_AUTO
0xF1	PEI_RECOVERY_USER
0xF2	PEI_RECOVERY_STARTED
0xF3	PEI_RECOVERY_CAPSULE_FOUND
0xF4	PEI_RECOVERY_CAPSULE_LOADED
0xFF	Boot process not start

Table 37 PCOM-B653VGL Debug message